Power Density and Performance Improvement of New Automotive Power Semiconductor Packages

Steadily but surely automobile manufacturers are looking to design out the engine-driven auxiliary loads such as fuel, water, brake and power steering pumps with electric driven ones. Here MOSFETs are the devices of choice to power such applications. Improved fuel efficiency, reliability and reduced CO_2 emissions are the main drivers, and variable speed electric drives rise to this challenge, but the dominance of the existing technology is strong. With Automotive DirectFET 2, the lead frame, wire bonding and molding are eliminated all together leading to further performance and reliability improvements.

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In March 2009 the Ford Motor Company announced that by 2012 it was targeting to have up to 90% the vehicles it produces equipped with Electric Power Steering. Ford cited the improved performance and a possible 5% fuel economy as driving factors for this rapid adoption.

Power density is a phrase often used in describing servers, but less often associated with cars, but it is indeed important; the vehicle needs to be a finite size and increasingly to meet emissions and fuel consumption regulations limits are put on weight. A typical lead acid battery has an energy density of around 0.1MJ/kg compared with around 45MJ/kg for gasoline; this is one reason why such advanced battery technology is needed to make hybrid and electric vehicles a practical reality - the traditional technology offers great energy density. Similarly the existing engine and hydraulic driven pumps on a car offer very good power density compared with a typical electrical motor, so replacing these traditional solutions with electric drives requires advanced motor design and highly efficient and compact power electronics.

Semiconductor switching losses

No semiconductor today is an 'ideal' switch with an infinitely low on resistance so heating occurs, and how this energy is managed and extracted from the switch, greatly affects power density. Consider thermal resistances and electrical resistances to be alike, temperature difference like electrical potential difference and power transfer the equivalent of current flow. Thus the power dissipation in the steady state of a semiconductor can be expressed according to equation 1 [1],

$$(1) \quad Pd = \frac{T_j - T_A}{R_{thJA}}$$

where Pd is the power dissipated in the semiconductor switch, T_j is the junction temperature, T_A the ambient temperature and R_{thJA} is the total thermal resistance from junction to ambient.

Linking power dissipation to current through the MOSFET allows a current density comparison between packages to be made, taking equation 2 into account:

$$(2) \quad P_d = I_D^{\,2} R_{DS(on)}$$

Substituting 1 and 2 together we arrive at equation 3:

$$(3) \quad I_D = \sqrt{\left(\frac{T_j - T_A}{R_{thJA}}\right) / R_{DS(on)}}$$

Finally dividing by the area of the MOSFET's PCB footprint we can arrive at the current density of a particular switch (equation 4):

$$(4) \quad CurrentDensity = \frac{I_D = \sqrt{\left(\frac{T_j - T_A}{R_{thJA}}\right) / R_{DS(on)}}}{A_{FP}}$$

We will now use equation 4 to see how we can increase current density and compare and contrast how different power semiconductor packages maximise this metric. Essentially there are three routes to getting good current power density in MOSFETs:

1) Minimal junction heating through using the lowest possible $R_{DS(on)}$
2) Extract the heat as efficiently as possible
3) Make the MOSFET as small as possible without sacrificing 1 and 2.

Keeping it small

Ultimately the smaller the footprint the MOSFET greater the power density, however such a reduction in package footprint area must not be done at the expense of $R_{DS(on)}$ or current carrying ability. Ultimately the designer wants to get the lowest $R_{DS(on)}$ possible in a given space. As die size and $R_{DS(on)}$ are inversely proportional, calculating the ratio of package footprint area to maximum die size area for the given package is an indication of the $R_{DS(on)}$ performance that a given package can offer in a given space. Figure 1 plots the ratio of package footprint to maximum die size area.

In Figure 1, the ideal ratio would tend towards 1, giving the least mm^2 of PCB footprint for a given $R_{DS(on)}$. However it clearly shows the area overhead that the more traditional packages such as the DPak and D2Pak place on the die size area, and ultimately the reduction in current density. The D2Pak has a package footprint to maximum die size area of 5; the package area is five times the size of the largest die size. Large Can DirectFET however offers a ratio of about 1.7 - so ultimately on the PCB a given $R_{DS(on)}$ in a smaller space can be achieved.

The technology and basic design of the D2Pak and DPak have changed little over the years, the leadframe, wrie bonds and molding take up area and volume while at the same time impeding performance;

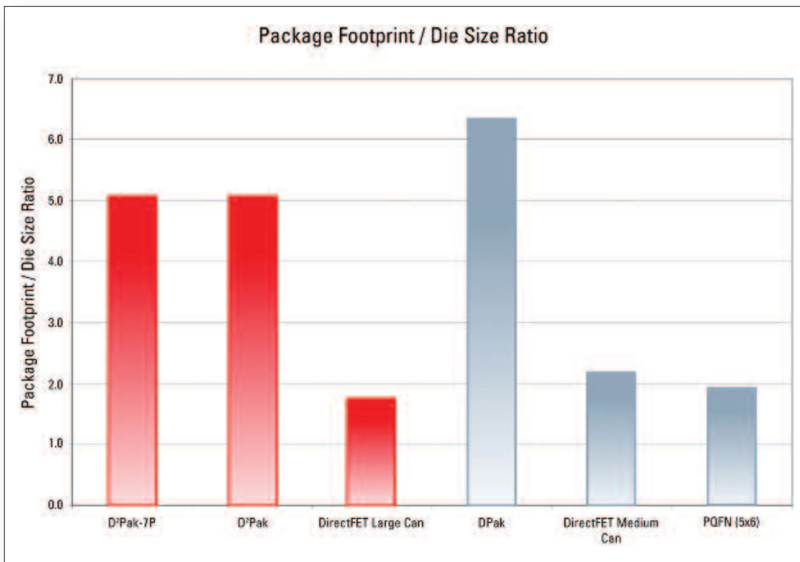


Figure 1: Package footprint to maximum die size area

they are an increasingly bothersome overhead as semiconductor technology improves. The latest power packages like the 5x6 PQFN fit far more silicon in a given space and in the case of Automotive DirectFET 2, the lead frame, wire bonding and molding are eliminated all together leading to further performance and reliability improvements.

Limiting heating

There have been dramatic advances in semiconductor technology over the years to achieve the lowest possible $R_{DS(on)}$ for a given area of silicon. Now with the very best trench technology and smallest geometries semiconductor designers are coming close to the fundamental performance limits of silicon, so not surprisingly new substrates like Silicon Carbide (SiC) and Gallium Nitride (GaN) are becoming popular as they can offer up to 10 times lower $R_{DS(on)}$ per area than a silicon based technology.

But before getting absorbed in new materials it's important to realise that there is still room for improvement on the packaging which will house the semiconductor, regardless of whether it's a Silicon or Silicon Carbide switch.

MOSFETs with an on-resistance of around $<2m\Omega$ are common place in the market today and increasingly on such devices around half of the $R_{DS(on)}$ stated on the datasheet is not attributed to the semiconductor die, but due to the packaging, or the Die Free Package Resistance (DFPR). Figure 2 shows the DFPR values for different types of packages, the lead frame and wire bonds used in the package add a significant distance to the path that the electrical current has to flow along and therefore make a large contribution to the $R_{DS(on)}$. When the wire bonds and leadframe removed (in the case of DirectFET) the DFPR is reduced to a value of less than half of equivalent plastic power package. The removal of this barrier ultimately means that a lower area of silicon is needed for a given $R_{DS(on)}$, and opening up the possibility of a system level cost saving.

Cooling down

From equation 4 its can be seen that as RthJA tends to zero the current density will increase as the heat generated in the junction is extracted and dissipated into the ambient more easily. Figure 3 shows the two thermal routes that make up the R_{thJA} for different package types, $R_{th(J-C)}$ top the thermal route through the top of the package, and $R_{th(J-PCB)}$ through the bottom of the package to the PCB. Power packages like the D2Pak and copper strap PQFN have excellent junction to PCB thermal paths, but like all the other traditional packages they are far less effective at allowing the heat generated to flow out through the top of the package, indeed they were not designed with top side cooling in mind. However when both top and bottom thermal paths are utilised drastic reductions in R_{thJA} can be made, as can be seen on the

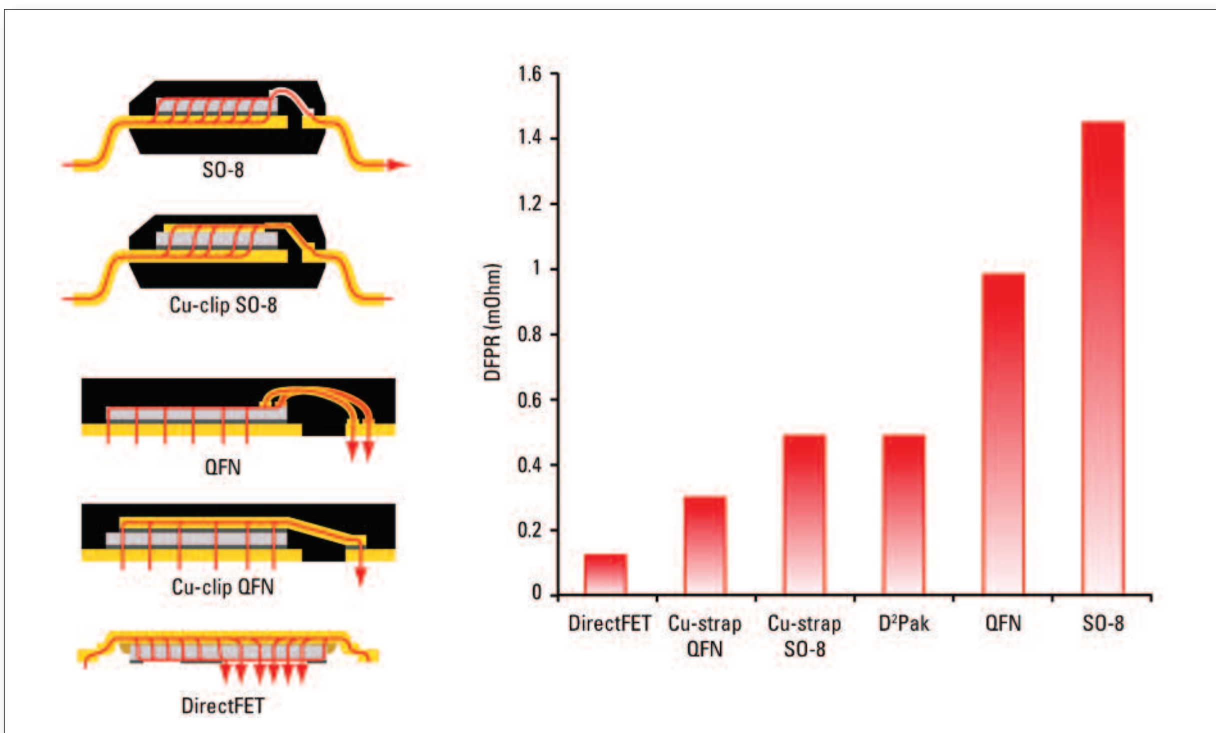


Figure 2: Comparison of Die Free Package Resistance (DFPR) for different semiconductor power packages

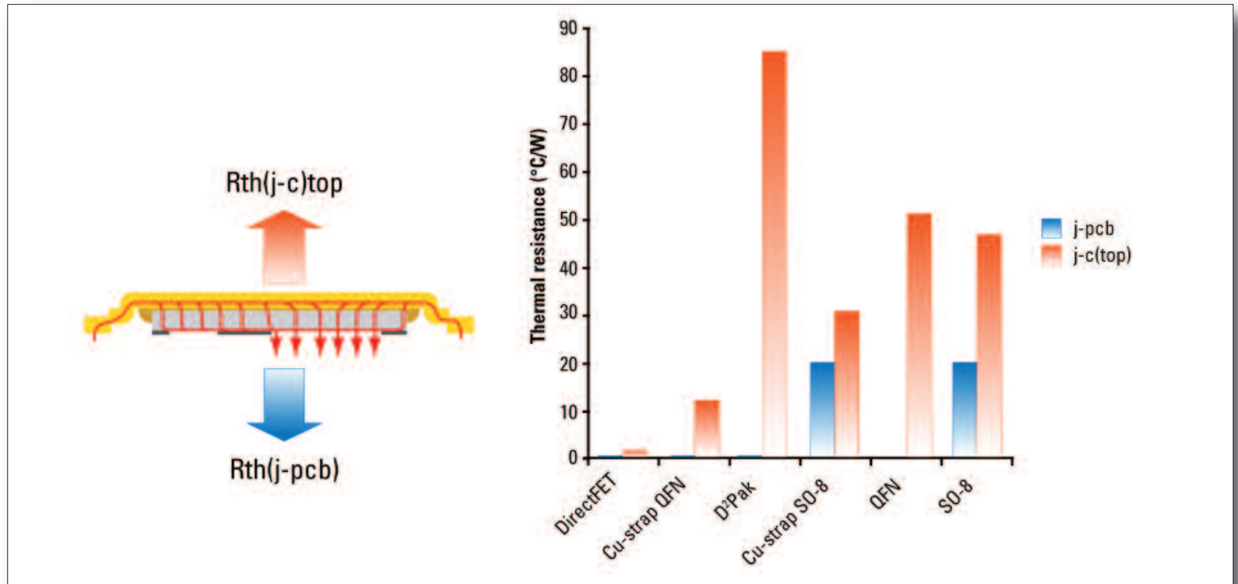


Figure 3. Comparison of thermal resistances for different semiconductor power packages

DirectFET package type.

Drawing the factors or space, $R_{DS(on)}$ and R_{thJA} together, Table 1 makes a side by side comparison of a large die, low $R_{DS(on)}$ D2pak product with a counterpart Automotive DirectFET product using equation 4. The table summarises the improvement in current density.

By taking two high performance 40V power MOSFETs which are typically used in automotive applications Table 1 shows how the simple construction of package like DirectFET, the elimination of wire bonds and leadframe allows $R_{DS(on)}$ PCB footprint and R_{thJA} to be minimised. This results in current density to be increased by over 3 times when compared with a traditional plastic D2Pak-7P, even in an application where dual sided cooling is not used.

Table 1: Comparison of Current Density for a D2Pak-7P and a Large Can DirectFET with different cooling arrangements

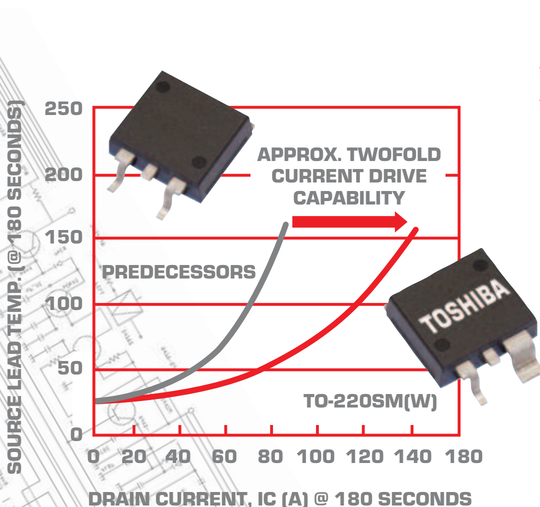
Part	AUIRFS3004-7P	AUIRF7739L2
Package	D2Pak-7P	Large Can DirectFET
PCB Footprint	170 mm²	64 mm²
Single Side Cooled on FR4		
R_{thJA} (Single side cooling)	40 °C/W	40 °C/W
$R_{DC(on)}$ @ T_j = 105°C, T_A = 25 °C	1.24 mΩ	0.9 mΩ
I_D	40.13 A	46.29 A
Current Density	0.24 A/mm²	0.73 A/mm²
Ratio of current density	**1**	**3.1**
Dual Sided Cooled		
R_{thJA} (Dual side cooling DF only)	12.5 °C/W	40 °C/W
$R_{DC(on)}$ @ T_j = 105°C, T_A = 25 °C	1.24 mΩ	0.9 mΩ
I_D	40.13 A	82.81 A
Current Density	0.24 A/mm²	1.3 A/mm²
Ratio of current density	**1**	**5.5**

Conclusion

The ability to drive more current through a smaller space, at higher efficiency and increase power density is going to become of greater importance as the electrification of the automobile unfolds. The replacement of fuel tanks and spark plugs of the past with batteries, IGBTs and MOSFETs of today will not happen by default. The new power electronic drive trains will not only have to meet but exceed the performance of the traditional internal combustion engine powered solution. With such demanding goals the use of next generation power semiconductor power packages which interfere less with the operation of the semiconductor will be key to ensure next generation efficiency, power density and performance goals are met.

Literature

[1] Power MOSFETs, Theory and Applications, Duncan Grant, John Gower



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