Application Considerations for Silicon Carbide MOSFETs

The SiC DMOSFET has definite system advantages over Silicon switching devices. However, its unique operating characteristics need to be carefully considered to fully realise these advantages. The gate driver needs to be capable of providing 20V drive with minimum output impedance and high current capability. The parasitics between the gate driver and SiC DMOSFET need to be minimised to assure that the gate pulse has a fast rise and fall time with good fidelity. The fast switching speed of the SiC DMOSFET can result in higher ringing and voltage overshoots. The effects of parasitics in the high current paths need to be carefully assessed. **Bob Callanan, Cree Inc., Research Triangle Park, USA**

The Silicon Carbide (SiC) DMOSFET has unique capabilities that make it a superiour switch when compared to its Silicon counterparts. The advantages of SiC DMOSFETs have been documented extensively in the literature [1]. However, there are some unique operating characteristics that need to be understood so that the device can be used to its full potential.

In this article, the characteristics of a typical 1.2 kV, 20 A SiC DMOSFET will be discussed. Comparisons will be made with other similar Silicon devices along with application implications. The intention of this comparison is to illustrate the differences in operating characteristics, not to pick the best device.

The devices selected for comparison are representative of commercially available Si IGBTs and MOSFETs with voltage and current ratings similar to the SiC DMOSFET. The TFS IGBT [3] is representative of a low on-voltage device and the NPT IGBT [4] is representative of a low turn-off loss device. The Si MOSFET [5] is representative of a commercially available 1.2kV Si MOSFET. Lastly, although not a 1.2kV device, the 900V SJMOSFET data [2] was included for comparison purposes. All comparisons were made with measured data except in the case of the SJMOSFET. Data sheet values were used.

Switching characteristics Silicon vs SiC

Consider the output characteristics of a typical 1.2 kV 20 A SiC DMOSFET as and the Si TFS IGBT shown in Figure 1. For the SiC DMOSFET, transition from triode (ohmic) to saturation (constant current) regions is not clearly defined as it is for the Si TFS IGBT. This is a result of the modest transconductance of the device. The modest amount of transconductance causes the transition from triode to saturation to be spread over a wider range of drain current. The result is that the SiC DMOSFET behaves more like a voltage controlled resistance than a voltage controlled current source.

The modest transconductance and short-channel effects are important to consider when applying the device. SiC DMOSFET needs to be driven with a higher gate voltage swing than what is customary with SJMOSFETS or IGBTs. Presently, 20V gate drive is recommended. The rate of rise of gate voltage will have a greater effect on the rate of rise of the drain current due to the lower transconductance. Therefore, the gate drive needs to supply a fast rise and fall time gate pulse to maximise switching speed. The SiC DMOSFET also has a threshold voltage similar to the Si SJMOSFET (2V nominal). Like the Si SJMOSFET, considerations need to be made for the lower threshold voltage, especially at high temperatures. Negative gate bias of up to -5V can be used if needed.

The rather large triode region can have impacts on certain types of fault detection schemes, chiefly the active de-saturation circuits. Some of these designs assume that the switching device enters a fairly high impedance constant current and/or transconductance saturation region during over-current faults. In the SiC DMOSFET case, the output impedance is lower and the device does not go into a clean constant current region during this type of over-current fault, especially under moderate over-currents. Therefore, the drain to source voltage will not increase as much. These characteristics of the SiC DMOSFET need to be carefully considered in fault protection schemes.

The forward conduction characteristics of the SiC DMOSFET along with the Si SJMOSFET, TFS, and NPT IGBTs are presented in Figure 2. The Si SJMOSFET's relatively high temperature coefficient of $R_{DS(on)}$ has considerable effect on its conduction losses. At 25°C, Si SJMOSFET and SiC DMOSFET were somewhat similar. At 150°C, $R_{DS(on)}$ of the SiC DMOSFET increases only about 20% from 25°C to 150°C whereas both the Si SJMOSFET and the Si MOSFET devices increases by 250%. This has a significant effect on system thermal design. The obvious advantage is that a smaller device can be used at higher

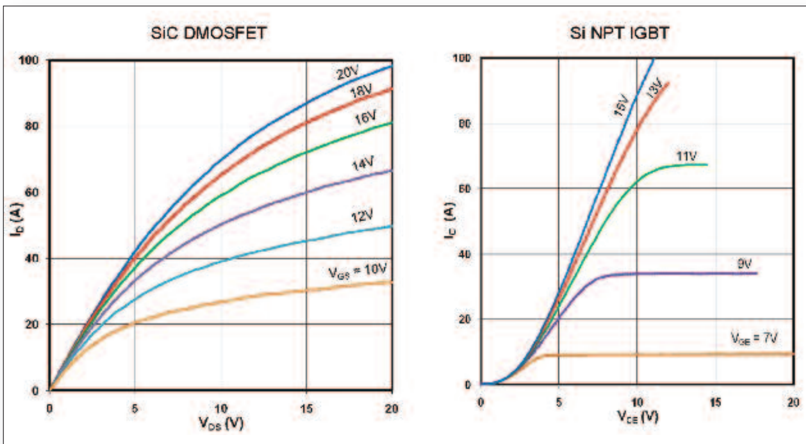

Figure 1: Output characteristics comparison (T_J = 150°C)

operating temperatures, higher than what is possible with Silicon.

One of the key advantages to SiC is the high temperature capability afforded by the wide bandgap. This is clearly reflected in the leakage current comparison at elevated temperature shown in Figure 3. The SiC DMOSFET has about 20x lower leakage current at 150°C. At 200°C, the Si comparison parts leakage current increases drastically, to the point where the device fails due to excess power dissipation. The SiC DMOSFET leakage current is still acceptable and over 100x lower than the Si devices.

As previously mentioned, the recommended gate drive voltage for the SiC DMOSFET is 20V. However, the amount of gate charge required to switch the device is low. The ramifications of the modestly higher gate voltage and lower gate charge can be reconciled by using the product of gate charge and gate voltage as a metric of gate energy. The gate charge and gate energy comparison is shown in Figure 4.

Even though the operating conditions are not exactly matched, the results of this comparison show that the SiC DMOSFET gate energy are comparable to or lower than the other devices. Therefore, the higher voltage swing does not adversely affect gate drive power requirements. The SiC DMOSFET V_{GS} versus gate charge characteristics are somewhat different from what is usually experienced with other gate controlled Silicon devices. The Miller plateau is not as flat as observed in typical Silicon MOSFETs and IGBTs. Once again, this is primarily due the modest amount of transconductance.

A popular figure of merit when comparing MOSFETs is the product of $R_{DS(on)}$ and total gate charge Q_g [6]. Minimisation of the figure of merit is an indicator of the superiour part. A comparison between the SiC DMOSFET and the other Si MOSFTs is shown in Figure 5. The Si SJMOSFET has a figure of merit of 32.4Ω*nC. The figure of merit of the SiC DMOSFET is 7.12Ω*nC. Furthermore, the SiC DMOSFET is a 1.2 kV part whereas the Si SJMOSFET is rated at 900V.

The inductive turn-off losses versus temperature of the SiC DMOSFET compared with the TFS and NPT IGBTs are shown in Figure 6. The freewheeling diode used with all devices was a 1.2 kV, 10A SiC Schottky diode. The turn-off losses of the IGBTs are significantly higher than the SiC DMOSFET and strongly increase with temperature. This is due to the tail loss inherent with IGBTs. The NPT IGBT is significantly better than the TFS IGBT. However, the NPT IGBT conduction losses are much higher than the SiC DMOSFET.

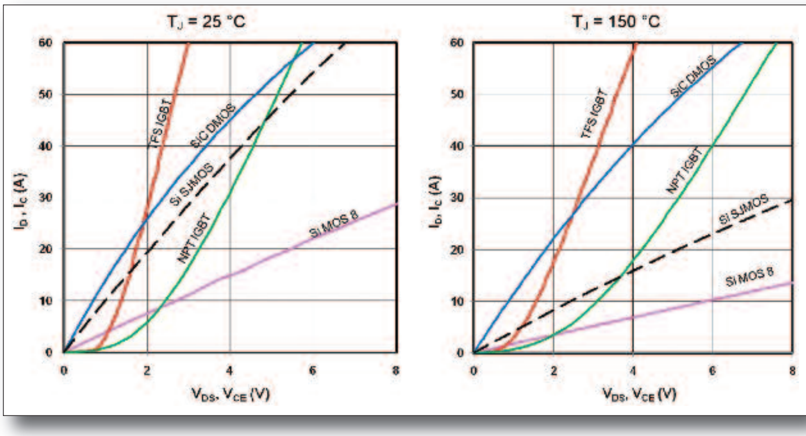

Figure 2: **Forward conduction characteristics comparison (V_{GS} = 20V, V_{GE} = 15V)**

The TFS IGBT conduction loss is lower than the NPT IGBT, but the switching loss is the highest of the three.

Gate driver requirements

To achieve fast switching time, the gate drive interconnections need to have minimum parasitics, especially inductance. This requires the gate driver to be located as close as possible to the SiC DMOSFET. Care should be exercised to minimise or eliminate ringing in the gate drive circuit. This can be achieved by selecting an appropriate external gate resistor. The silicon IGBT current tail provides a certain amount of turn-off snubbing that reduces voltage overshoot and ringing. As with any majority carrier device, the SiC DMOSFET has no tail, so the amount of drain voltage overshoot and parasitic ringing is noticeably higher. The higher ringing is of concern because of the SiC DMOSFET's lower transconductance and low threshold voltage reduces gate noise immunity. The high level of drain current di/dt can couple back to the gate circuit through any common gate/source inductance. A Kelvin connection for the gate drive

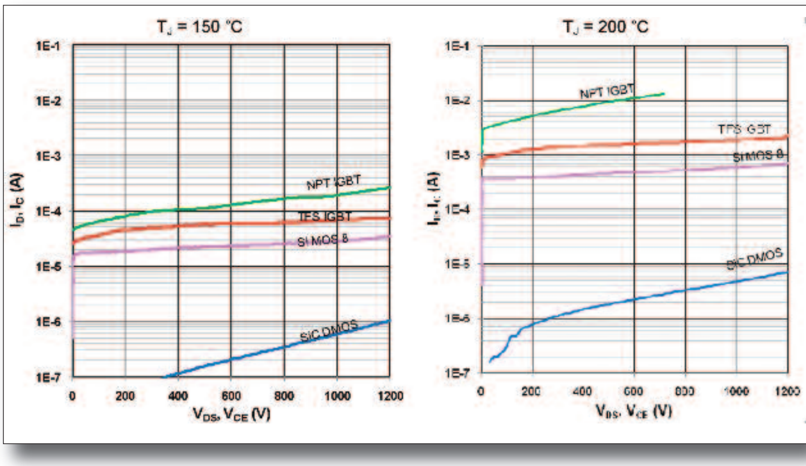

Figure 3: **High temperature leakage current comparison**

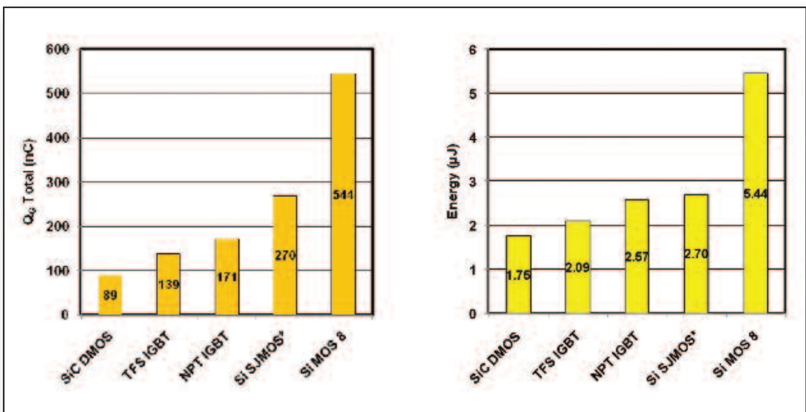

Figure 4: **Gate charge and energy comparison**

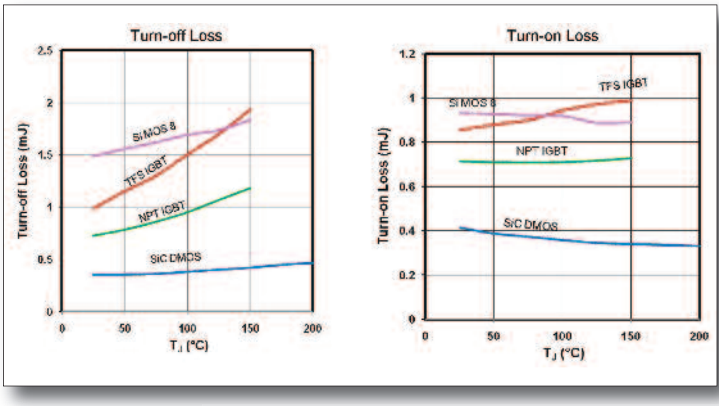

Figure 5: Figure of Merit comparison (Q_g * $R_{DS(on)}$)

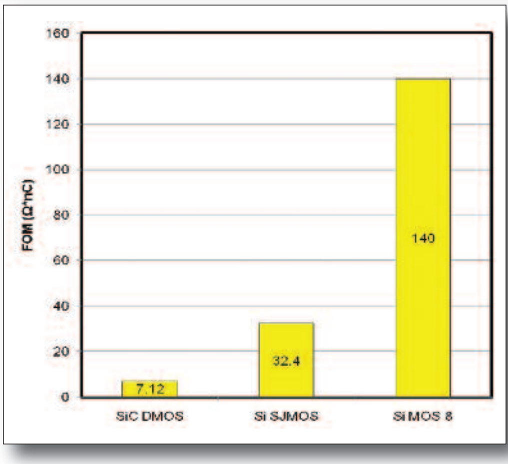

Figure 6: Switching loss vs. temperature comparison (V_{DD} = V_{CC} = 800V, I_D = I_C = 20A, R_G = 10Ω)

recommended, especially if the gate driver cannot be located close to the SiC DMOSFET. Ferrite beads (nickel-zinc recommended) in lieu of or in addition to an external gate resistor are helpful to minimise ringing while maintaining fast switching time.

Like any other power MOSFET, the SiC DMOSFET has a body diode. The body diode is a SiC PN diode that has a 2.5V - 2.7V built-in voltage, but a substantially lower reverse recovery charge when compared to a Si SJMOSFET. Use of this diode is not recommended due to its high forward drop. An external SiC Schottky diode is suggested.

Literature

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