

# Trench Field-Stop IGBT3 Turn-Off

The new Trench-Field-stop devices show significant differences in control characteristics compared to Power MOSFETs. The reason is the large amount of stored charge, which builds up in the conduction mode. This storage effect can be described by an additional element in an equivalent circuit, a capacitance at the output. **Daniel Heer, Reinhold Bayerer, Thomas Schütze, Infineon Technologies AG, Warstein, Germany**

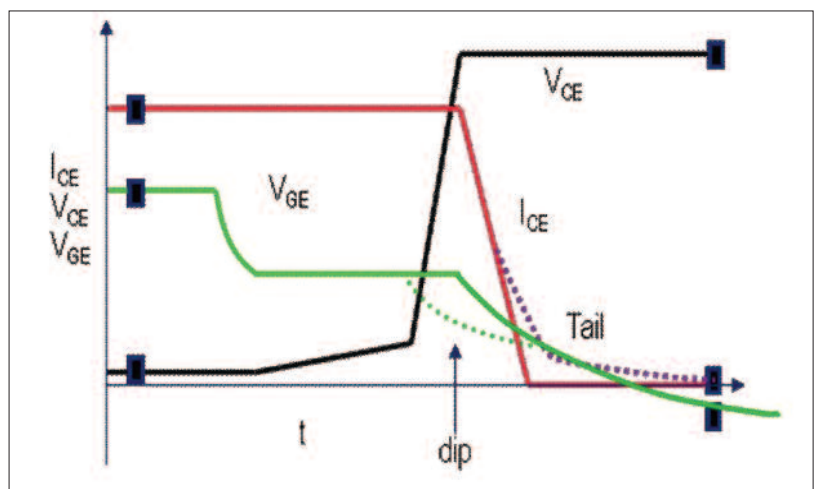
A simple equivalent circuit contains the output characteristics,  $C_{GC}$ ,  $C_{GE}$ , and the new  $C_{CE}$ -capacitance. This circuit describes principal switching and control characteristics. Characterization of these elements is done by special test configurations, which allow excluding parasitic capacitance of the package. As an additional outcome of the work the stored charge of a 3.3 kV IGBT3 and its dependence on conduction time is received.

## Turn-off description of trench field stop IGBT

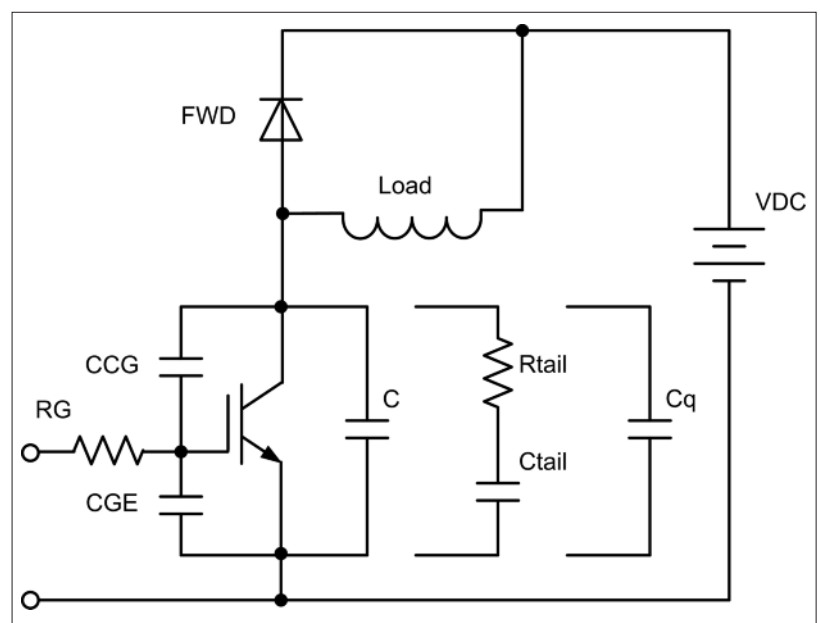
The turn-off of a standard power MOSFET under inductive load starts with a drop of gate voltage to the threshold for the actual load current. Then the gate voltage stays at that level while the drain voltage is rising and the drain current continues to flow. When the drain voltage reaches the DC-bus voltage the drain current starts to fall controlled by the gate voltage, now drop from the threshold level (Miller plateau) to the off state. The turn-off is completely controlled by the gate voltage - see solid traces of Figure 1. Super-Junction MOSFETs can differ from this behavior.

The Trench-Field-stop IGBT is well suited for inverter circuits, which benefit from low conduction losses. These low losses are achieved by significantly increased carrier density compared to former generations. During turn-off against inductive load, such devices don't require an open MOS-channel all the time to carry the load current. For a short period of time the stored charge is feeding the load current. This behavior occurs at the end of the Miller plateau, where the gate voltage shows a dip in, i.e. the MOS-channel closes while the load current is still running. During this period the collector voltage is rising according to the decay of stored charge. Figure 3 illustrates the turn-off under different load currents.

The  $dV/dt$  of the collector voltage varies with the amount of load current in a way



**Figure 1:** Turn-off of a MOS-device. Solid traces apply to standard MOSFET, dashed deviations apply for IGBTs. The dip in the gate voltage indicates, that the collector current is carried on by stored charges



**Figure 2:** Equivalent circuit describing the turn-off of a Trench-Fieldstop IGBT under inductive load. The IGBT symbol stands for the static output characteristics  $I_{CE}(V_{CE}, V_{GE})$ .  $C_{CC}(V_{CE})$ ,  $C_{CE}$  and  $C$  are well known elements for MOSFETs and IGBTs.  $C_q$ ,  $C_{tail}$  and  $R_{tail}$  are introduced here to describe the bipolar behavior of the IGBT

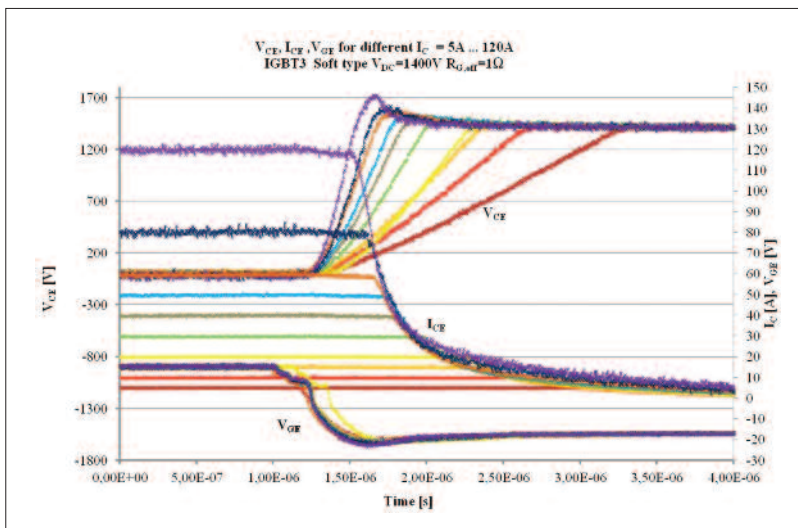


Figure 3: Turn-off of a 3.3kV IGBT3, single chip under different load currents. See the variation in  $dV/dt$  with changing collector/load current. At a low gate resistance the gate voltage drops before collector voltage has risen to  $V_{ce}=V_{DC}$

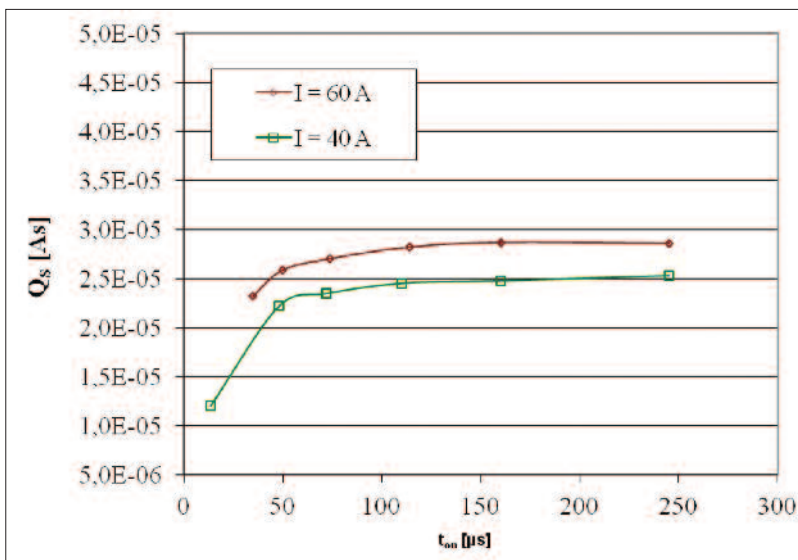


Figure 4: Charge stored in a single 3.3kV IGBT3 as a function of on-time -  $Q_s=f(t_{on})$  ( $I_c=40$  A,  $t_{on}=14...245$   $\mu$ s and  $I_c=60$  A  $t_{on}=35...245$   $\mu$ s,  $V_{DC}=1400$  V,  $R_g=1$   $\Omega$ )

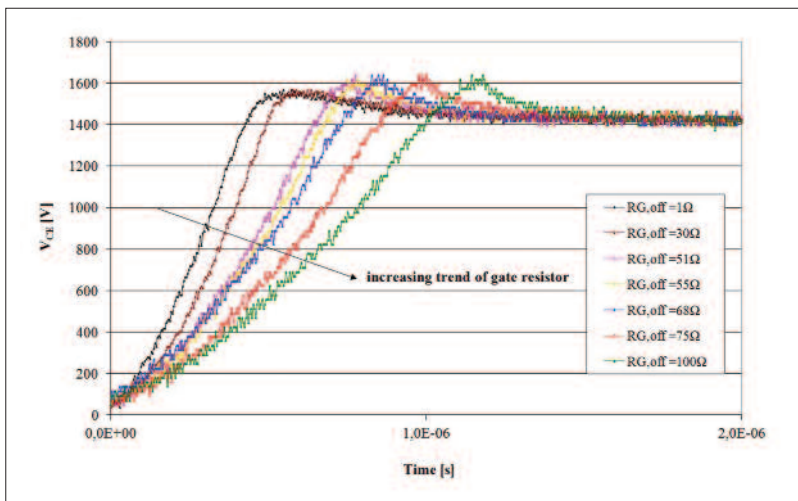


Figure 5: Turn-off of 3.3kV IGBT3, single chip switched with different gate resistors at  $V_{DC}=1400$  V,  $I_c=60$  A,  $t_{on}=100$   $\mu$ s. See the variation in  $dV/dt$  with changing the resistor

similar to loading a capacitor by a constant current. This leads to the equivalent circuit of Figure 2, which represents the switching of a Trench-Fieldstop IGBT by the output characteristics to describe the static characteristics, a collector-gate voltage dependent capacitance a constant gate emitter capacitance and an additional output capacitance  $C_a$ , which is much larger than the usual junction capacitance between collector and emitter. The tail current is described by an R-C element. The additional output capacitance varies with the amount of stored charge, which depends not only on load current but also on the time the IGBT was in conduction mode. The charge, which is stored in conduction mode and is extracted during collector voltage rise until  $V_{ce}=V_{DC}$ , is presented in Figure 4 with reference to the on-time of the IGBT.

A further influence of the stored charge on the switching behavior can be shown by variation of the gate turn-off resistance. Figure 5 illustrates the turn-off under different gate resistors. For gate resistors ranging from 1 to 30  $\Omega$ , the  $dV/dt$  of the collector voltage is constant. The  $dV/dt$  is intrinsically limited. The reason is the stored charge controlling the voltage rise. For gate resistors of more than 30  $\Omega$  the  $dV/dt$  becomes reduced and controlled by the gate resistor  $R_g$ . The Miller plateau is stretched. During this Miller plateau a significant amount of stored charge is withdrawn, resulting in a higher  $dI/dt$  during current fall. This can be detected by an increased over-voltage in Figure 5.

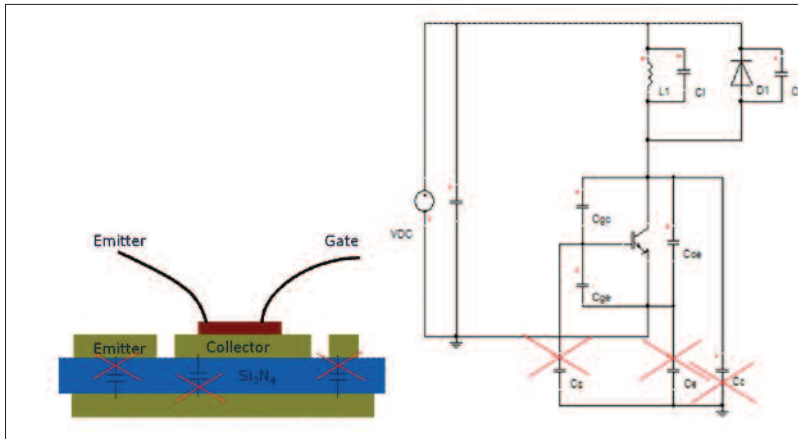
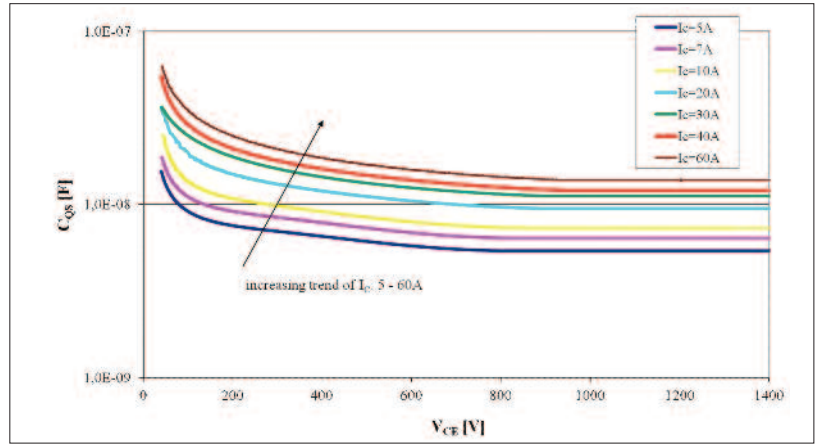
The additional output capacitance  $C_a$  in Figure 2 shall describe the self limitation of  $dV/dt$  and the effect of stored charge whereas  $C_a(V_{ce})$  is a function of  $V_{ce(t)}$ . During turn-off the collector current divides into MOS-channel and stored charge current. The amount of the MOS-Channel current can be detected by measurement of gate emitter voltage and calculated using the transfer characteristics of the IGBT. The difference between collector current and the MOS-channel current is the share of the stored charge. In the phase of turn-off where the MOS-channel current is negligible (for low  $R_g$ ) the output capacitance  $C_a$  carries the whole load current and determines the  $dV/dt$ . The characterization of  $C_a$  for the whole range of gate resistors, currents,  $V_{DC}$  and  $t_{on}$  allows to describe the turn-off with respect to more or less stored charge. As an example this calculated capacitance for different load currents is presented in Figure 6 with reference to the collector voltage of the IGBT.

For the characterization of the IGBT a test setup, which prevents package capacitances, was used. Figure 7 shows a sectional view of



**RIGHT Figure 6:** Calculated output capacitance  $C_{os}$  for different load currents as a function of the collector voltage ( $V_{DC}=1400\text{ V}$ ,  $R_C=1\ \Omega$ )

the IGBT on the substrate and the circuit diagram for the test. Only one IGBT chip without free-wheeling diode was tested. This reduced the total capacitance which was charged and discharged during  $dV/dt$  of the collector voltage and no paralleling effects between two or more IGBTs occurred. For the measurement of the true gate emitter voltage the internal gate resistor was shorted. This test setup allowed a pure characterization of the static and dynamic



**LEFT Figure 7:** Sectional view of the IGBT on the substrate (left) and test circuit diagram (right)

parameters without influence of parasitic package capacitances.

**Conclusion**

A simple behavior model is presented which is easy to establish by characterization and implementation in circuit simulators. It allows better understanding of gate drive and turn-off characteristics of new IGBT generations. The model is applied to the recently introduced 3.3kV IGBT3.

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