Infrared Determination of Junction Temperature and Switching Losses

Junction temperature of power MOSFETS is one of the major criteria to obtain temperature derating curves for power converters. It is quite evident that the hottest spot temperature on the lead and case (package) areas of a power MOSFET is typically a couple of degrees less than the junction temperature. This hottest spot temperature can be accurately measured by an infrared camera without the heat flow intrusion.

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In order to keep the junction temperature (Tj) within specifications, allowable drain (leads) temperature (T_D) is often calculated by the formula:

$$T_D = Tj - Pj * \theta_{JD}, \quad (1)$$

where Pj is the total heat power generated inside the package (includes conduction losses, switching losses and gate losses), θ_{JD} is the junction-to-drain (leads) thermal resistance, which is a package related parameter defined by the MOSFET manufacturers in their data sheets. Typical values of θ_{JD} for some standard power MOSFET packages are shown in Table 1.

If for example, a MOSFET in an SO8 package (θ_{JD}=15 K/W) that dissipates Pj=1 W of power which must maintain a junction temperature below 125°C, then the measured drain temperature must not exceed 110°C according to (1) : T_D =125°C - 1 W * 15 K/W = 110°C.

Using equation (1) implies that Pj can be determined under any operational condition and also that the total power generated inside the package is dissipated to ambient through the drain leads. In reality, the accuracy of the Pj calculation is relatively low because switching losses in the MOSFET cannot be calculated accurately enough. Also since a portion of the Pj is dissipated to ambient through the MOSFET package, actual heat flow through the drain leads is smaller than Pj which presents another source of error while using equation (1).

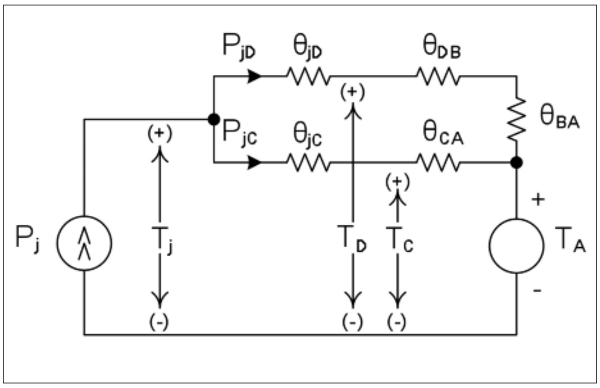

Figure 1: MOSFET thermal model - total heat Pj generated in the MOSFET is dissipated to ambient through two parallel branches: junction-drain (leads)-PCB-ambient and junction-case (package)-ambient

Method for determining a MOSFET junction temperature and switching losses

The objective of this article is to present a method for determining a MOSFET junction temperature and switching losses based on the given thermal resistances and lead and case (package) temperature measurements. In order to develop such a technique let us consider the MOSFET thermal model in Figure1 which is a modification of the model used in [1].

According to this model, the total heat generated in the package, represented by a current source Pj, flows to ambient through two parallel branches: junction-drain (leads) -PCB-ambient ("drain" or "lead" branch, labeled Pj_D) with θ_{JD} - junction-to-drain thermal resistance, θ_{DB} - drain-to-PCB thermal resistance and θ_{BA} - PCB-to-ambient thermal resistance, and junction-case (package)-ambient ("case" or "package" branch, labeled Pjc) with θ_{JC} - junction-to-case thermal resistance and θ_{CA} - case-to-ambient thermal resistance. Also in Figure1, T_c is the case temperature and T_A is the ambient temperature represented by a voltage source.

Applying conventional electrical circuit analogy to the diagram in Figure.1 and Ohm's law, we obtain the following

Thermal Resistance	Package Type					
	DirectFET	PowerPAKSO8	DPAK	D2PAK	LFPAK	SO8
θ_{JD}, K/W	1	1.5	1.5	1.5	2	15

Table 1: Typical values of junction-to-drain (leads) for some standard power MOSFET packages

equations for the heat portions Pj_D and Pjc flowing through the respective “drain” and “case” branches:

$$Pj_D = Pj/(1+ \theta_D/\theta_C), \quad (2)$$

$$Pjc = Pj/(1+ \theta_C/\theta_D), \quad (3)$$

where $\theta_D = \theta_{JD} + \theta_{DB} + \theta_{BA}$ (total “drain” branch thermal resistance) and $\theta_C = \theta_{JC} + \theta_{CA}$ (total “case” branch thermal resistance) so that total heat flow Pj is:

$$Pj = Pj_D + Pjc. \quad (4)$$

Applying Ohm’s law to the series combinations of thermal resistances in each branch of the diagram in Figure 1 we get two equations for junction temperature Tj:

$$T_j = T_D + (T_D - T_A) * \theta_{JD} / (\theta_{DB} + \theta_{BA}) = T_D + (T_D - T_A) * \theta_{JD} / \theta_{DA}, \quad (5)$$

$$T_j = Tc + (Tc - T_A) * \theta_{JC} / \theta_{CA}. \quad (6)$$

Both equations (5) and (6) do not contain heat power Pj and each of them can be used for calculating the junction temperature Tj as long as the case, the drain, ambient temperatures and thermal resistances of the package are known.

If we apply these equations to a typical SO8 power MOSFET with thermal resistances $\theta_{CA} = 380$ K/W, $\theta_{JC} = 18$ K/W, $\theta_{JD} = 15$ K/W and $\theta_{DA} = 20$ K/W (given in [1]), substituting these values into equations (2) and (3) we obtain:

$$Pj_D/Pj = 1/[1+(15+20)/(18+380)] = 0.92 \quad (7)$$

$$Pjc/Pj = 0.08. \quad (8)$$

In other words, 92% of total power generated in the silicon is dissipated to ambient through the drain and the remaining 8% - through the case. Another important observation is that θ_{CA} is much greater than any other thermal resistance in the system, which makes the second term in equation (6) relatively small. Assuming Tc=125°C and T_A=85°C for the set of parameters given above, the junction temperature according to (6) is Tj = 125+(125-85)*18 / 380=126.9°C. This is only 1.9 K greater than the case temperature. Using equation (5) to calculate the drain temperature, we obtain $T_D = (Tj + T_A * \theta_{JD} / \theta_{DA})/(1+ \theta_{JD} / \theta_{DA}) = (126.9+85*15/20)/(1+15/20) = 108.9$°C.

This temperature is lower than the case temperature by 16.1°C. This implies that for an SO8 power MOSFET with θ_{JD} being on the same order as θ_{DA} and with θ_{CA} being much greater than θ_{JC}, the drain temperature tends to be lower than the case temperature, not only that but the plastic case temperature is an accurate representation of the junction temperature. According to the measurement results in [1] the difference between Tj and Tc for SO8 packages is typically 1-3 K. If we use the same equations for other MOSFET packages like PPAKSO8, D2PAK, DPAK and LFPAK with low junction-to-drain thermal resistances θ_{JD} (see Table 1), both the drain and case temperatures are close to the junction temperature Tj. For DirectFET type MOSFETs with metal case θ_{JD} is even lower and, according to (5), the drain temperature is an accurate representation of the junction temperature.

For a more accurate Tj calculation based on (5), parameter θ_{DA} unavailable from MOSFET data sheets can be determined as follows. According to Figure1 junction-to-ambient thermal resistance θj_A, provided in the MOSFET data sheets, is a parallel combination of θ_D and θ_C resistances and $\theta_{DA} = \theta_D - \theta J_D$. Applying this to the diagram in Figure1 we can get:

$$\theta_{DA} = \theta j_A/(1 - \theta j_A/ \theta_C) - \theta_{JD}. \quad (9)$$

Taking into account that θ_C is approximately one order greater than θj_A, equation (9) can be rewritten as:

$$\theta_{DA} \approx 1.1 * \theta j_A - \theta_{JD}. \quad (10)$$

Substituting (10) into (5) we get:

$$Tj \approx T_D + (T_D - T_A) * \theta_{JD} / (1.1 * \theta j_A - \theta_{JD}), \quad (11)$$

where all the thermal resistance values are available from the data sheets.

The junction temperature was calculated above based on parameters specified on the component data sheet and temperature measurements taken from the device under test conditions. A conventional drain (lead) and case (package) temperature measurement technique is based on the thermocouples placement on the package and on the lead areas. The measured temperatures with the thermocouples are lower than actual temperatures for two reasons: first, the thermocouple itself works as a heat sink cooling the device down and second, its physical placement is critical when trying to determine the hottest temperature of the device. A more accurate temperature measurement method is the use of an infrared camera which determines the hottest spot temperature in the areas of interest (case and lead) without the heat flow intrusion.

As soon as the junction temperature Tj is determined, total power Pj generated in the silicon can be calculated by the formula:

$$Pj = (Tj - T_A) / \theta j_A, \quad (12)$$

where θj_A - junction-to-ambient thermal resistance is available from the MOSFET data sheets. Pj can also be calculated based on equation (2) and junction-to-drain thermal resistance θ_{JD} which is also available from the MOSFET data sheets:

$$Pj = (1+ \theta_D/\theta_C)*(T_D - T_A) / \theta_{JD}. \quad (13)$$

θ_D and θ_C are not available from the data sheets but since θ_C is approximately one order greater than θ_D, equation (13) can be rewritten as:

$$Pj \approx 1.1*(T_D - T_A) / \theta_{JD}. \quad (14)$$

After Pj is determined, switching losses Psw can be calculated in the conventional way:

$$Psw = Pj - Pdc - Pg = Pj - I_{rms}^2 * Rds_{on} - Q * V_g * F_{sw}, \quad (15)$$

where Pdc - conduction (DC) losses, Pg - gate drive losses, I_{rms} - RMS value of drain current, R_{dson} - MOSFET ON-resistance, Q - total gate charge, V_g - peak gate voltage, F_{sw} - switching frequency. For a square wave drain current with peak I_{pk} and duty cycle D, $I_{rms}^2 = I_{pk}^2 * D$.

Results

From the above analysis based on the thermal model in Figure1 it is quite evident that the hottest spot temperature on the lead and case (package) areas of a power MOSFET is typically a couple of degrees Celsius less than the junction temperature. This hottest spot temperature can be accurately measured by an infrared camera without the heat flow intrusion.

A more accurate junction temperature value can be calculated by equations (5), (6) and (11) based on lead and case temperatures measured by an infrared camera and thermal resistance values provided in the MOSFET data sheet.

Total power generated inside the silicon and switching losses can be determined by equations (13)-(15).

Literature

[1] www.irf.com/technical-info/designtp/dt99-2.pdf