# High Frequency Oscillations due to Driver Coupling

The coupling between the driver and the power module is usually given too little attention. Yet, many problems can be tracked back to this very interface, such as when IGBTs are switched very rapidly, or when desaturation takes place during short circuits. This article outlines some of the considerations with regard to potential causes. **Stefan Schuler, Development Engineer, SEMIKRON, Nuremberg, Germany**

**A driver's primary task is to provide the** power required for switching the IGBTs, and to establish a galvanic insulation between the input signals.

The underlying principle of a driver which provides galvanic insulation to the TOP and BOT sides, e.g. by means of two transformers, is shown in Figure 1. The downstream circuits are the signal processing and the actual driver stage. Besides the typical activation voltage of +15V and a negative shutoff voltage, the power supply may provide additional voltage for logic circuits or microcontrollers. The connection to the power module is often implemented by empirically defined gate resistors. A series of complex test procedures makes sure the module switches safely and correctly under all and any circumstances.

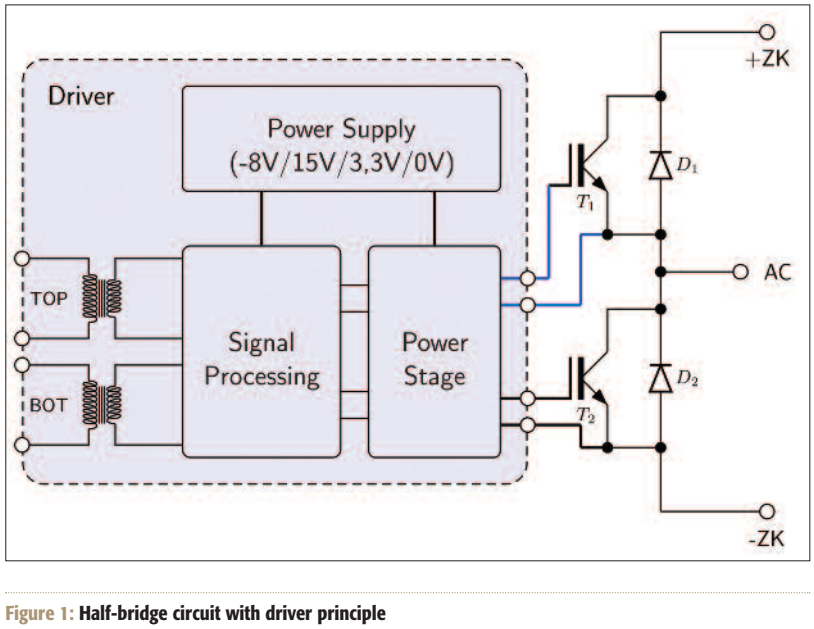


Figure 1: **Half-bridge circuit with driver principle**

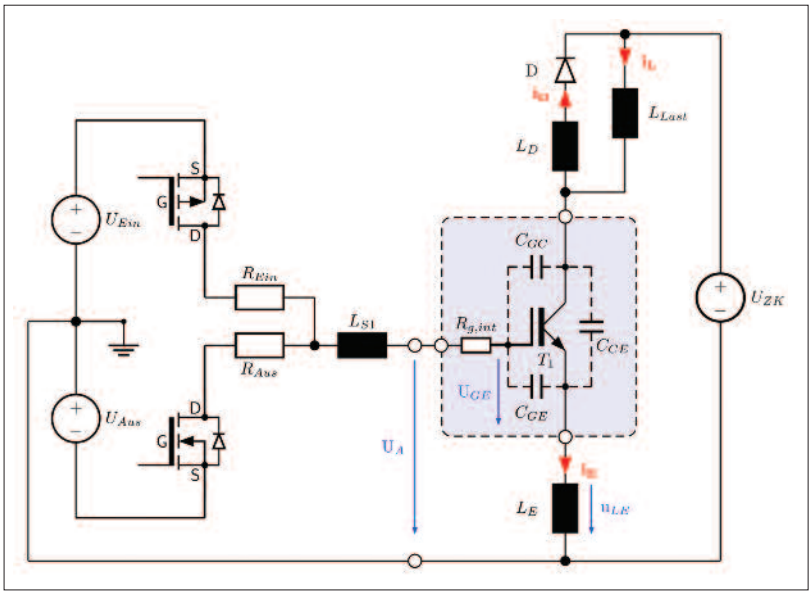


Figure 2: **Equivalent circuit diagram with driver connection**

## Focus on parasitics

The electric coupling allows for generating a greatly simplified equivalent circuit diagram (Figure 2). It shows the switching lower IGBT (BOT), its parasitic capacitances and the integrated series resistor, a load $L_{LOAD}$, and the free-wheeling diode D in the TOP branch. The parasitic inductances $L_D$ and $L_E$ (also called leakage inductances) represent the conductor tracks and bonding wires of the diode and the IGBT. On the driver side, the schematic shows a push-pull output with power supply, gate series resistors and the parasitic conductor track inductance $L_{S1}$.

The driver's output voltage $U_A$ is parallel to the actual gate-emitter voltage $u_{GE}$ and the voltage drop $u_{LE}$ of the parasitic inductance in the emitter branch. A current change in the IGBTs generates an induced voltage uLE that equals $L_E$ multiplied by $di_E/dt$. Quickly, the bonding wires on the emitter side are identified as the main causes of the parasitic inductance. As a rule of thumb, calculations are made with one nanohenry (nH) per millimeter of bonding wire length. Major current changes easily induce several volts of voltage. However, the ohmic resistance can easily be neglected, as it is only approximately 5…10 mΩ per bonding wire, so in a 75 A chip, for instance, it would clearly stay below 100 mV.

## Coupled LC circuits

A closer look at Figure 2 shows a first LC

circuit which consists of the components $L_{S1}$, $L_E$ (summarized into $L_S$) and the gate-emitter capacitance $C_{GE}$. The gate series resistors $R_{g,int}$ and $R_{On/Off}$ summarized into $R_g$, dampen this LC circuit. On the one hand, this causes a shift of the angular resonance frequency towards smaller values for ω, on the other hand, the resonance spectrum becomes greater while at the same time, the amplitude is dampened. In short - the quality is diminished. A second LC circuit is formed by the parasitic components of the intermediate circuit, the IGBT that is being looked into, and the parasitic inductance $L_E$, which is the link towards the driver circuit.

Finally, there is a third LC circuit, consisting of the Miller capacitance $C_{GC}$ and the finite, yet frequency-defining switching time of the IGBT. Therefore, repercussions on the driver are possible via two different mechanisms: on the one hand, via the emitter's inductance $L_E$, and, on the other hand, via the Miller capacitance as mentioned above. The following chapters shall look into more details of which one of the two effects stated will be the dominant one in each individual case, causing a tendency towards oscillation in the whole system.

## Emitter inductance influence

The measurable influence of the emitter's parasitic inductance is limited to large current changes, which primarily occur when switching takes place. Analyzing the switch-on process (Figures 3 and 4), one initially recognizes a negative feedback phase that turns into a positive feedback phase. This circumstance is owed to the diode's reverse recovery charge which causes a positive feedback while it discharges because the emitter's current decreases, making di/dt negative for a short period of time. The switch-off process, however, is characterized by an exclusive negative feedback phase. In both cases, the proportion of the coupling level is determined by the current intensity to be switched within a time window, while during the switch-on process, said recovery charge of the free-wheeling diode needs to be taken into account. Generally, the negative emitter coupling is a desirable circumstance, as it contributes to a certain stabilization of the whole system by causing the effective current slopes of the individual IGBTs to assimilate.

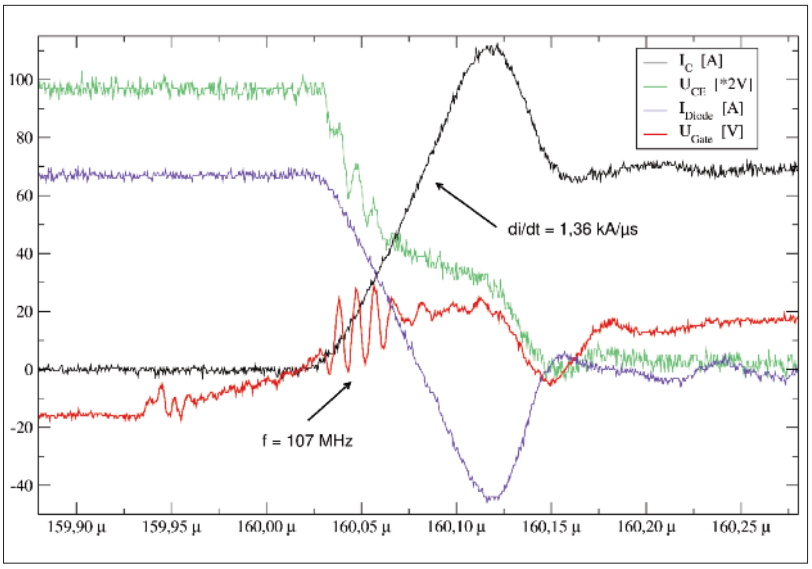


**Figure 3: Switch-on process with 100 ns slope time of the collector current (10-90 %)**

**Source: Dominic Malane**

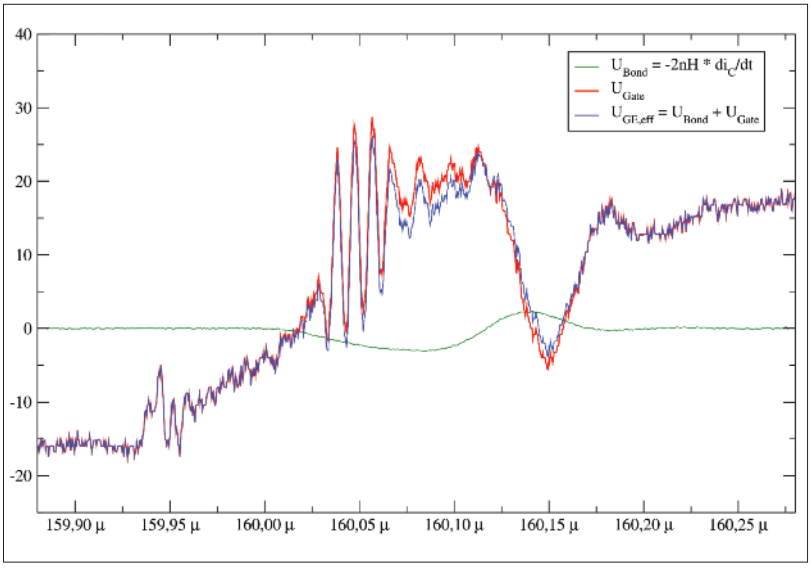


**Figure 4: Gate voltage curve during switch-on (excerpt from Fig. 3). Green shows the curve of the voltage induced at the eight parallel emitter bonding wires (2 nH total). The blue line is the calculated effective gate voltage**

## Miller capacitance influence

Basically, the Miller effect is a negative coupling, because a rapidly declining emitter-collector voltage (switch-on) will cause a displacement current to flow from the gate to the collector. The IGBT will then be a little less conductive until an equilibrium is established between the gate current and the displacement current, which becomes visible in the oscilliogram as a Miller Plateau with its charateristic flat shape. The displacement current is proportional to the Miller capacitance and the collector-emitter voltage change $du_{CE}/dt$. However, the Miller capacitance itself strongly depends on the voltage: it reaches a minimum when uCE equals the DC link voltage, and peaks when $u_{CE}$ is lower than the gate voltage $u_{GE}$. This can be monitored very well when comparing the plateau curve against the collector-emitter voltage curve.

Now, while the switching time determined by the driver is significantly longer than the switch-on delay of the IGBT, the displacement current will be moderate, the Miller Plateau will be nicely articulated and the system only contains a non-critical discrepancy between the actual and target conditions. When the switching is too aggressive, however, it is not

possible to establish a stable equilibrium, as the high $du_{CE}/dt$ caused by this circumstance will cause a high displacement current and, hence, a rapidly changing gate potential which the IGBT is unable to compensate quickly enough due to its latency. The consequence is a strong resonance at the gate and the collector. In tests, it was easily possible to produce a frequency amplitude of 28 V at the gate with an DC link voltage of 200 V.

### Switch on

When the active gate-emitter uGE reaches the threshold voltage, the current slowly begins to commutate from the free-wheeling diode to the IGBT. This current change is the reason for the voltage induced at the emitter's inductance that counteracts the driver voltage $U_A$ and reduces the effective gate-emitter voltage $u_{GE}$ – a classic case of negative feedback.

According to general assumption, the consequence would be for di/dt to be reduced, and along with this, also the negative feedback, due to the IGBT's reduced conductivity, so the current is able to increase, which in turn causes a high-frequency oscillation (of the current). This assumption is not perfectly correct, because as a matter of fact, it's not the current that is being modulated, but the collector-emitter voltage. The current curve itself is very inert, its velocity of change is low, so the induced voltage of the emitter's inductance remains almost constant across a wide range. However, a distinction must be made at this point between different cases, namely 1) driver switching speed higher than IGBT and 2) driver switching speed lower than IGBT.

In the first case, the current is modulated by the IGBT's switching behavior, resulting in the familiar curves where the collector-emitter voltage only drops steeply after the entire current has commuted to the IGBT. In the second case, the maximum current increase is determined by the environment, i.e. the effective inductances during the commutation. This specific case allows the IGBT to go to early partial saturation, which shows in the fact of the collector-emitter voltage already dropping significantly during the current increase (Figure 3).

The reduction of the collector-emitter voltage that occurs during the commutation process can mostly be tracked down to parasitic inductances along the path which can be calculated from the ratio of the voltage difference between $U_{ZK}$ and $u_{CE}$ and the current slope. In case of high switching speeds, this characteristic flat spot in the $u_{CE}$ curve will disappear.

Across a wide range, the increase rate of the current is determined by the gate series resistor. When, during a later switching cycle, higher currents commute to the IGBT, the time window will enlarge accordingly. The conditions for $di_E/dt$ will therefore stabilize, which causes a negative feedback that changes only slowly, and which might be the reason for higher switching losses but does not cause any tendency towards oscillation.

However, the situation is dramatic for the Miller effect, particularly for steep voltage slopes (9.8 kV/µs in Figure 3). By nature, it's a negative feedback, but it is phase-shifted by the IGBT's response time. When excited with a certain frequency, the negative feedback might turn into a positive feedback – resonance scenario! This shows in a clear tendency towards oscillation with high displacement currents (more than 2 A in this example). The oscillation will only end after a few cycles, usually at the time when the effective emitter-side negative feedback peaks.

### Energy transfer

The emitter's inductance feeds energy into the driver circuit during a high diE/dt. The curve of the energy feed is continuous and rather slow, so no excitation of the driver's LC circuit might occur.

The elements of the coupled driver that determine the frequency are the parasitic inductances and the gate-emitter capacitance $C_{GE}$ (approx. 4 nF in the example). In the test described, the gate achieved a frequency of approx. 100 MHz, with the time behavior of this primary, feed-providing LC circuit is mostly determined by the switching delay of the IGBT. The coupling element to the secondary driver LC circuit is the gate-collector capacitance.

### Approaches

So, which measures need to be taken in order to suppress the undesirable oscillation behavior?

In most cases, the first means of choice will be to try to increase the gate series resistor. Firstly, this will increase the IGBT's switching times, secondly, this provides a classic way of damping the whole system. The slower switching times will effectively reduce the displacement current and the excitation energy, the disadvantage lies in the higher switching losses.

Another common alternative is the purposeful tuning of the secondary LC circuit by means of a capacitance that is parallel to the gate-emitter capacitance. This measure also dampens the Miller effect due to the better capacitance ratio. In some cases, one would also install an upstream R-C element, so effectively, together with an integrated gate resistor and gate capacitance, this would translate into an R-C-R-C element constellation, more widely known as a two-stage low pass. When the cut-off frequencies of both filter parts match, the total cut-off frequency will be reduced to half the value of each individual low pass. In many cases, this is a pretty useful compromise, yet, at the sacrifice of slower switching times and higher losses.

So, what to do? It's desirable to have an advantageous impedance curve of the driver, also for high frequencies. Twisted wires that are as short as possible leading to the module constitute an effective and mostly cost-efficient measure. What's more, smart routing of the conductor tracks will reduce the inductance, i.e. at least parallel routing of the auxiliary emitter and gate tracks, or even better, in two adjacent layers. What's very important is to provide impulse-resistant capacitors at the supply connectors of the push-pull output. These will reduce the inductive influence of the two supply wires to the output transistors. Last but not least, the focus should be on fast and low-resistive output transistors. When these measures are implemented stringently, artificially slowed down switching can be omitted just the same as complex and expensive filters.

### Conclusion

In power modules, parasitic inductances and capacitances prohibit fast switching with low losses. The design of the new driver needs to be matched to the module, i.e. in the switching process, the feedback of the IGBT on the driver must not induce oscillation. Classic damping approaches do not always produce satisfactory results; oftentimes, these measures are put in place only later. It is much more efficient to focus on the interface already during the design of the driver, and to ensure low-impedance adjustment across the entire frequency range by design.

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