

GaN Matures for Industry with Monolithic Power ICs

Power GaN has come of age with high performance, high frequency and high reliability. It has taken over 15 years for the material to mature from university curiosity to industry-qualified product, from the early days of dMode (normally-on, depletion) to eMode (normally-off, enhancement) devices. Now, manufacturing issues have been resolved and lateral 'GaN-on-Si' devices have been qualified on 6" wafers using conventional, low cost Si fabrication equipment. Now, the introduction of GaN Power ICs – with monolithically-integrated gate drive, logic and FET in low-cost, high volume packaging – enables power systems to run at multi-MHz switching frequencies simply, predictably and with high device and system reliability. **Dan Kinzer, CTO, COO; and Stephen Oliver, VP Marketing, Navitas Semiconductor, El Segundo, USA**

Superjunction Silicon (SJ Si) is no longer the best solution for off-line power supplies. Power Gallium Nitride (GaN) manufacturing processes are mature and devices are operating with higher frequencies, higher efficiencies, higher power densities and lower system costs.

Gallium Nitride (GaN) is a wide bandgap (WBG) material, even wider than SiC. As GaN can be formed with a two-dimensional electron gas (2-DEG) by using an AlGaIn/GaN heteroepitaxy structure, It can have very high mobility and very high carrier density in the channel and drain

drift region. This gives GaN a big resistance advantage compared to existing devices in the 650 V class. (see figure 1a).

On the way to maturity

The earliest GaN power devices were d-mode (depletion mode) which are turned on with zero gate-to-source voltage (V_{GS}), and require a negative V_{GS} to turn off – not a practical solution for off-line applications. This unwanted "always on" characteristic of d-mode devices was mitigated by the addition of a second, low voltage 'cascode' silicon FET that is used to turn the GaN power

device on and off. This essentially converts the depletion-mode into an "always off" device, required to block high bus voltages when a power converter is first turned on.

The cascode FET allows for a standard gate drive signal to be used (0 V = OFF) where zero volts turns the device off and a positive gate drive voltage turns the device on. Cascoding results in a two-switch module that presents a variety of concerns including complex (multiple and/or stacked die) packaging, high parasitic inductance, ceramic interposers for isolation, tendency for oscillation and

RIGHT Figure 1: Comparison of Si, SiC, GaN physical properties, plus AlGaIn lateral 'GaN-on-Si' construction

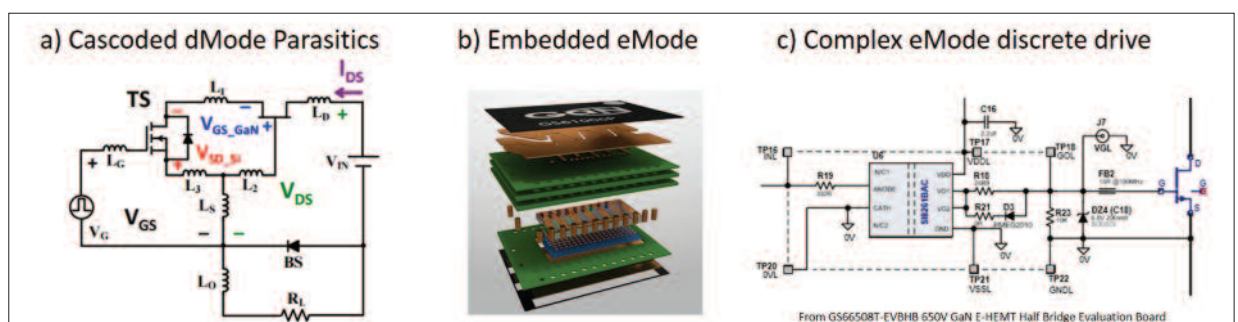
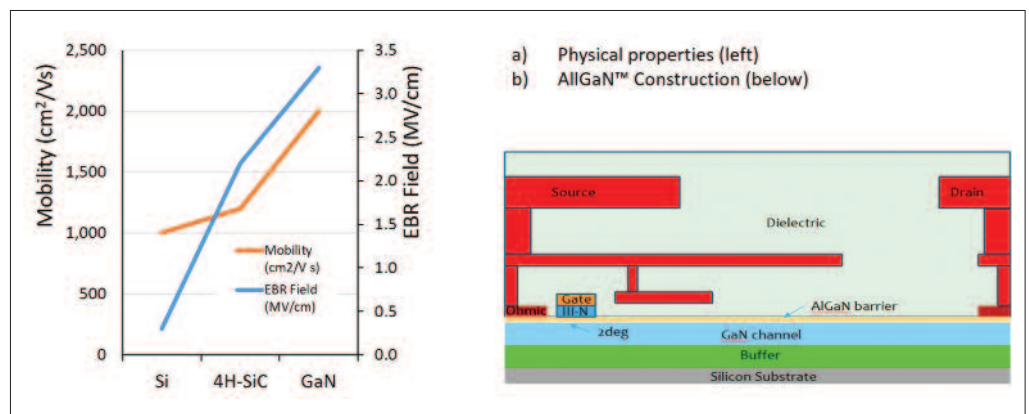


Figure 2: Early dMode & eMode GaN packaging and gate drive

internal over-voltage stress, reduced overall yield, and ultimately a higher cost (see figure 2a).

Early enhancement (e-mode) devices have been implemented in wafer-level chipscale packaging up to 200 V. Others have been offered in standard low performance through-hole packages, but these require on-state gate current and still need a negative gate to ensure they are fully off. Still others more recently have been offered in expensive, non-standard PCB-embedded packaging (figure 2b).

In all of these cases, a high level of sensitivity exists at the gate due to a very low threshold voltage, so tightly regulated gate voltage is required and the devices are very susceptible to noise and voltage spikes that can easily occur due to high-frequency and high-dv/dt noise from the surrounding switched-mode converter circuit. To mitigate these problems, a complex external gate drive circuit (Figure 2c) may be required that includes a voltage regulator circuit, a Zener clamp, an additional gate capacitor, and a ferrite bead. Also, since the gate drive circuit is placed and routed with PCB traces, much care is needed for layout design to reduce parasitic inductance such as cross-coupling of devices and PCB layers.

Dealing with all of these issues by

adding components and PCB layers, while trying to increase switching frequency and increase power density, can be a major roadblock to bringing a product out of the lab and into production. A simpler and more reliable solution is needed without adding additional concerns or difficulties.

AllGaN and GaN Power ICs

AllGaN™ is the first platform which allows monolithic integration of 650 V GaN IC circuits (drive, logic) with GaN FETs. It is based on a very high density, lateral e-mode device structure with extremely high speed switching capability. The result is a device which liberates the performance of e-mode GaN using a simple digital signal, with the previously vulnerable gate now safely protected.

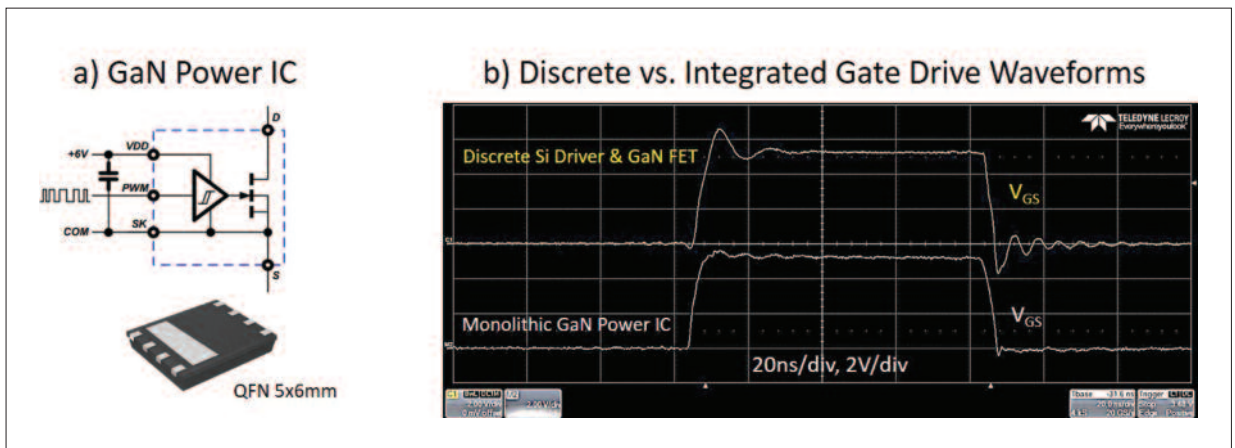
This 'GaN Power IC' contains features such as hysteretic input, voltage regulation and ESD protection – all integrated in the same GaN layer as the main power device (see figure 1b). This monolithic integration of drive and switch is impractical using d-mode GaN, vertical GaN or SiC. Lateral 'GaN-on-Si' construction means immediate high volume capability using existing foundry processes.

Within the AllGaN solution, the GaN FET gate is driven safely, precisely and

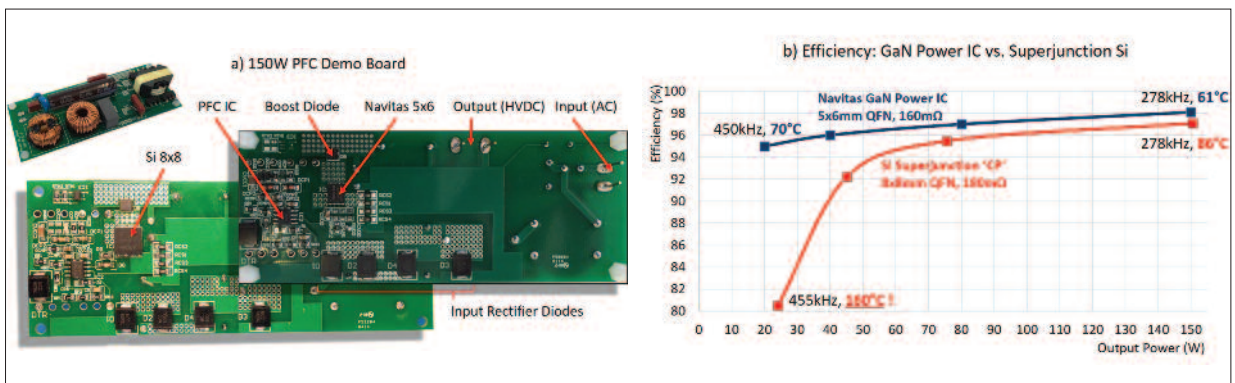
efficiently by the upstream integrated GaN driver. Standard 3.3 V, 5 V or 15 V PWM signals are fed directly into the GaN Power IC for an easy, low component count design (Figure 3a). Integrating the driver also reduces ringing and enables tight control of turn-on, turn-off for high-frequency half-bridge applications (Figure 3b).

Practical PFC application

A 150W PFC boost converter was used as a test case for the 650 V GaN Power IC and also the benchmark Si FET (650 V 'CP' SJ, Figure 4). The circuit uses a standard L6562 controller running in Critical Conduction Mode (CrCM), with switching frequency varying with load and AC line. At full power (~280 kHz), the 5 mm x 6 mm GaN Power IC runs 25°C cooler than the 8mm x 8 mm 'CP' SJ, with 33 % lower loss. This circuit highlights one frequency limitation with Silicon – high capacitance. As the load is reduced, the highly non-linear output capacitance of Si (C_{oss}) at low V_{DS} creates a lossy, non-ZVS condition as frequency increases. Silicon reaches an unsustainable 160°C case temperature while the GaN C_{oss} is so low that it runs very cool at only 70°C for the same conditions. A single CrCM PFC circuit can be comfortably designed up to 250 W,



ABOVE Figure 3: GaN Power IC schematic, gate switching waveforms



ABOVE Figure 4: PFC boost application example (demo board, GaN Power IC vs. Superjunction Si)

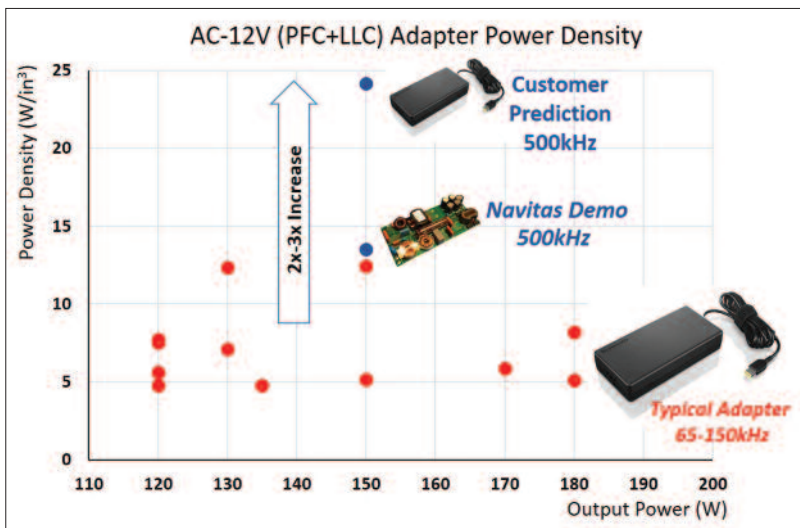


Figure 5: LLC application example: power density increase with frequency

then may be interleaved for higher power applications while maintaining a very low profile.

Switching frequency plays a major part in converter size and cost due to the effects on magnetic components. A study of EMI chokes (common mode, differential mode) and PFC boost inductors showed that magnetics costs could be reduced by 40 % and size reduced by 75 % by

increasing switching frequency 5x from a nominal 200 kHz to 1 MHz.

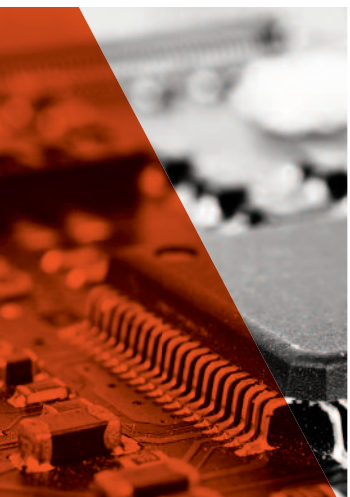
Higher power density with high frequency

High specification 'gamer' laptops, all-in-one PCs and 38"-50" TVs use AC-DC adapters in the power range 120-180 W. Today, the majority of adapters run at 65 kHz/100 kHz with typical power densities

around 8 W/in³ with a few benchmark adapters at 12 W/in³. Customer estimates, based on a non-optimized, 500 kHz 150 W PFC+LLC demonstration board using GaN Power ICs indicate that 24 W/in³ will be achieved. This is a 2x-3x increase on today's designs (Figure 5). This simple example showing that the higher frequency enabled by GaN Power ICs shrinks magnetics and enables high efficiency, higher power density solutions.

Conclusions

For power system designers, GaN Power ICs represent breakthrough - yet mature - technology, which brings new benchmarks in switching speed, efficiency and power density to a broad array of applications at a wide range of power levels. Unlike other, earlier wide bandgap proposals, GaN Power ICs also represent a simple, fast, scalable and dependable building-block approach to system design, to minimize risk / respins and maximize chance of success. With the AllGaN lateral 'GaN-on-Si' platform qualified on 6" wafers using conventional, low cost Si fabrication equipment, and with products assembled using high volume, industry-standard QFN packaging, monolithic GaN Power ICs are ready for industry.



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