

Quantification of Cracked Areas in IGBT Modules

Degradation of the thermal conduction path is one of the most common failure mechanisms of power semiconductor modules. Typically, solder fatigue happens due to the thermo-mechanical stresses at the interfacing contacts resulting from mismatched coefficient of thermal expansions (CTE) between different materials and causes cracking. Thermal transient measurement using Mentor Graphics' T3Ster® hardware is a characterization method for heat conduction path in power semiconductor packages. **Mohammed Amir Eleffendi, Li Yang, Pearl Agyakwa, and Mark Johnson, Department of Electrical and Electronics Engineering, University of Nottingham, UK**

The heat flow path in this type of test can be represented by an equivalent electrical Resistance-Capacitance Cauer-type model. T3Ster uses thermal impedance via "structure functions" as a non-destructive evaluation technique to detect structural defects in the heat conduction path. Junction-to-case thermal resistance (R_{thjc}) and cracked area, from

structure functions, are compared to the cracked and unattached area estimated by Scanning Acoustic Microscopy (SAM) for a conventional 1.2 kV/200 A IGBT power module that is actively power-cycled to degrade the solder at the substrate-base plate interface. SAM imaging was performed at regular intervals for multiple stages of the power cycling test to observe

the gradual degradation of the solder layer. The power module under test was an off-the-shelf 3-phase IGBT module consisting of three substrate tiles mounted on a copper baseplate with two IGBT chips and two free-wheeling diodes.

Power module test procedure

The IGBT module was mounted onto a cold plate with a 25 μm thick Kapton film used as an interfacing material between the cold plate and the baseplate. The purpose of this film was to increase the case-to-ambient thermal resistance in order to achieve a temperature swing at the substrate-case interface and so accelerate the degradation of the substrate mount-down solder layer compared to other failure mechanisms. All IGBTs were biased with a $V_{ce} = 15\text{ V}$ such that the cycling current I_C as well as the measurement current I_M were shared between the three legs of the module. The collector-emitter voltage V_{ce} is a global measurement across the whole module and therefore, it represents an "average" measurement of the three legs.

A calibration curve $T_J = f(V_{ce})$ at a constant measurement current of 200 mA was used to calculate junction temperature T_J . The cycling current I_C was regulated by the power tester to preserve a constant $\Delta T_J = 120\text{ K}$ with $T_{Jmax} = 140^\circ\text{C}$ and $T_{Jmin} = 20^\circ\text{C}$ as estimated from V_{ce} with the water temperature maintained at 20°C . The heating time and cooling time were fixed at 50 s, and 60 s respectively. This achieved a ΔT of 70 K at the substrate with $T_{max} = 90^\circ\text{C}$ and $T_{min} = 20^\circ\text{C}$. The test started with an initial cycling current of 236 A which resulted in a power dissipation $P_D = 704\text{ W}$. As the thermal



Figure 1: High-power multi-chip power modules can be characterized using MicRed Power Tester® 1500A

resistance increased during the test due to solder fatigue, the cycling current was regulated to keep the ΔT_j constant.

Under these conditions, the wire-bond lift-off mechanism is not the dominant mechanism and the substrate mount-down solder degrades before any wire-bond lift-off is observed. The power cycling was paused regularly every 1000 cycles, at which time a thermal impedance measurement was made of the module in situ by the 1500A Power Tester (Figure 1) and this resulted in a total of 17 thermal impedance measurements during the test.

SAM characterization was carried out during the power cycling test using a PVA TePla AM300. Scanning acoustic microscopy is a non-destructive technique that allows to image the internal features of a specimen and can detect discontinuities and voids of sub-micron thickness. It creates 2D greyscale images from the reflected ultrasonic echoes.

Defects at any of the internal layers cause discontinuity in the structure and block the ultrasonic signal preventing it from penetrating through the layers beneath the defected areas. Thus, defects in the substrate solder result in a black shadow appearing in the C scan images taken from the chip level (Figure 2). In this

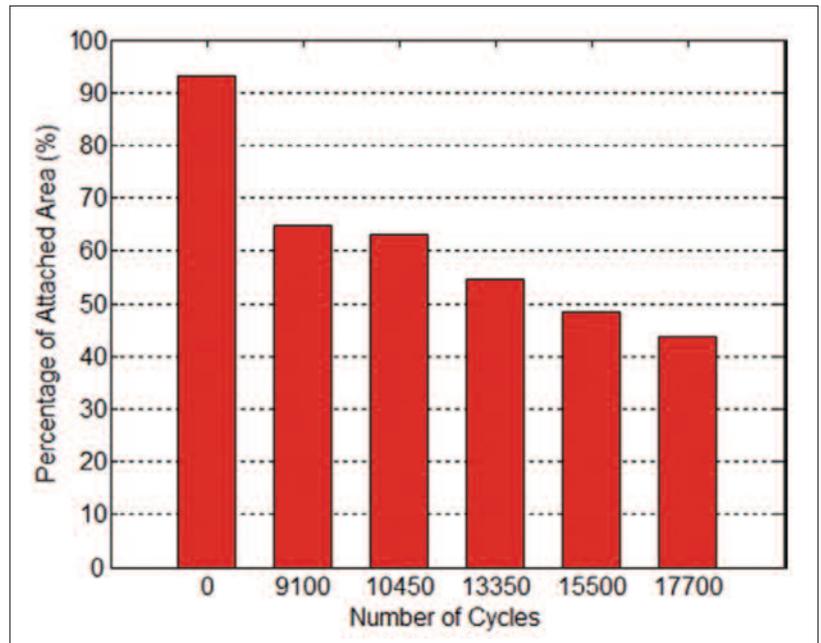


Figure 4: Estimated attached area of solder layer during the cycling test from SAM images

way, the C scan images were used to obtain distinct boundaries between the attached and discontinuous areas. However, the exact location of the defects within the structure can be unclear from SAM images, and therefore, correlative

metallurgical cross-sectioning was necessary (Figure 3). Figure 4 shows the estimated attached area of the solder layer at different cycle numbers during the cycling test. As the number of cycles increases, cracking propagates through the solder causing the attached area to be reduced gradually until it reaches 43 % attached area after 17,700 cycles.

The power cycling test was terminated after 17,700 cycles by which time the total junction-to-ambient thermal resistance R_{thja} had increased by 14% from its original value. After examination, all IGBT devices were still electrically functional.

But the SAM image showed different levels of discontinuity beneath the individual IGBT devices. Therefore, an investigation was carried out to examine whether this non-uniformity in heat flow can be observed in the structure functions for the individual IGBT chips in addition to the module as a whole. For this study, thermal paste was used as the interface material instead of the Kapton film used during the power cycling test. The local thermal impedance of each individual IGBT in the module was measured and the structure function was calculated. The attached area under each individual IGBT

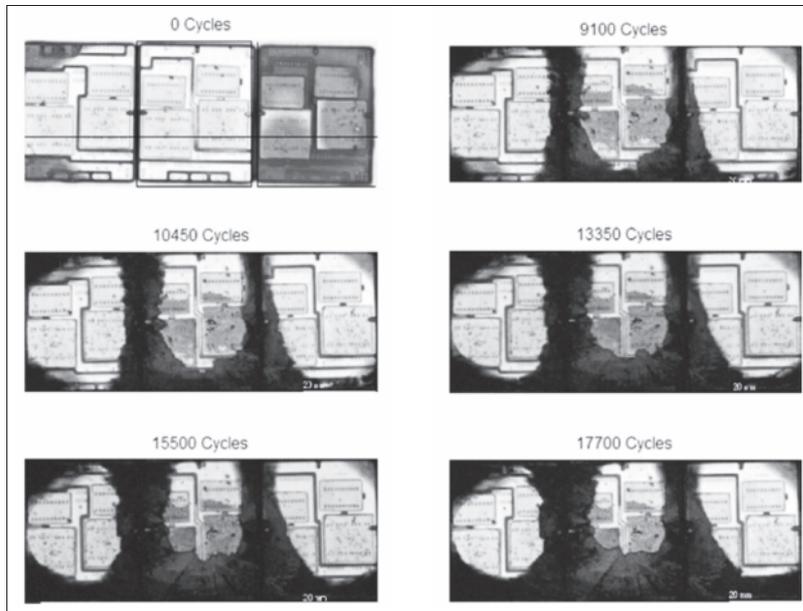
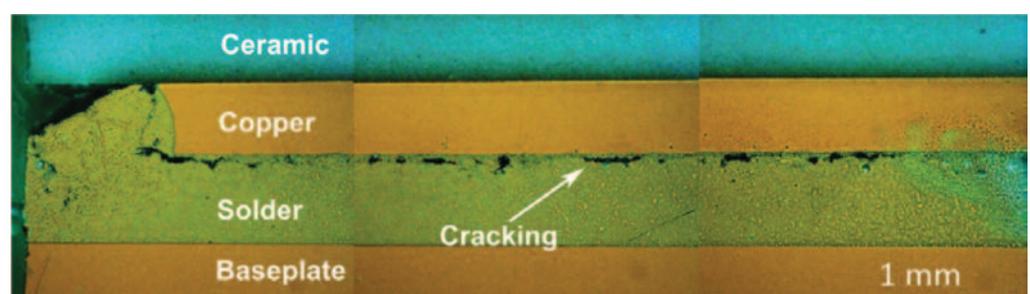


Figure 2: Scanning Acoustic Microscopy (SAM) images at different cycles during the power cycling test

RIGHT Figure 3:
Image of metallurgical cross-section showing the cracking resulting from power cycling at the substrate-baseplate interface



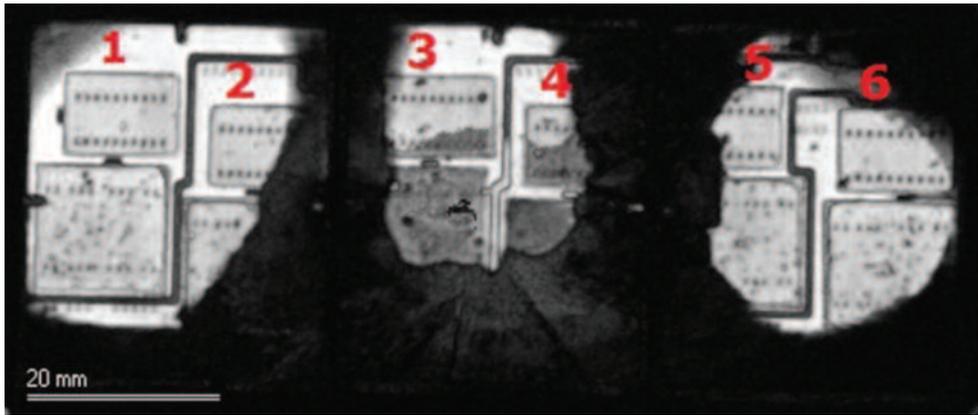


Figure 5: SAM image of the cycled module at 17,700 cycles shows different levels of delamination under the 6 IGBT devices

was estimated from the SAM image at 17,700 cycles shown in Figure 5.

The different thermal layers can be easily identified related to Device 1 and Device 6 as they are the least affected by solder fatigue. Features of the different layers in the structure start to disappear as the level of local delamination increases in the other devices. Device 4 is the worst affected by cracking. Hence the thermal resistance R_{thjc} may be directly compared with the percentage of attached area below the individual IGBTs.

Conclusions

An evaluation using MicReD T3Ster structure

functions within a Mentor Graphics 1500A Power Tester as a non-destructive testing tool for examining the integrity of the heat flow path in high power multi-chip semiconductor modules under repeated cycling. A 1.2 kV/200 A IGBT power module (with six IGBTs) was power cycled to activate the solder fatigue failure mechanism at the substrate–baseplate interface. Thermal impedance measurements and SAM imaging were performed at regular intervals during the power cycling test. From this data, the thermal structure function was calculated and the cracked area in the solder layer was estimated. Failure analysis by cross-sectioning confirmed the location of the

discontinuity at the substrate–baseplate solder layer. A clear correlation was found between the change in the junction-to-case thermal resistance R_{thjc} estimated from the structure function and the remaining attached area of the solder layer calculated from SAM images.

Literature

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