# Accurate Mains Frequency Monitor with Calibration

An AC power mains utility frequency is typically either 50 Hz or 60 Hz. The frequency variation is normally restricted to about +/- 1% in most countries. Variation occurs usually because of varying load on the grid; a higher load causes the frequency to drop and vice versa. The importance of monitoring power frequency is especially important when a local minigrid is set up – such as with solar-powered or wind-powered installations. The inverter in such cases must shoulder the responsibility of monitoring the output power quality. The Silego GreenPAK SLG46620 and a few external components can be used to design a frequency deviation monitor that signals an alert if the frequency deviates by a specified margin.

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**In industrial setups that use equipment** such as induction motors, it is important to maintain the proper frequency because the speed of an induction motor is a function of the frequency. More elaborate and sensitive setups may use AC drives to maintain the motor speed, but in many situations the motor may be directly connected to the power source without a drive, in which case variations in power frequency directly impact the motor speed.

## Broad design strategy

The design is based on measuring the period of the waveform. Many designs use a zero-crossing detector as the basis for period measurement. The mains input is stepped down and half-wave rectified with a few components shown in Figure 1. The rectified pulses are fed to the GreenPAK chip (see sidebar) and used to trigger an analog comparator (ACMP) reading at Pin 12. The ACMP's IN-terminal is held at 50 mV, and when it toggles, it enables a counter which counts pulses from an internal oscillator until the end of the half-cycle. The ACMP's low-bandwidth mode is enabled to prevent spurious responses due to noise. To determine whether the deviation of the mains input frequency is acceptable, two DCMPs are used to compare the output of the counter at the end of the half-cycle with two registers which store the upper and lower bounds of interest. DCMPs are available in the GreenPAK 4 series, such as the SLG46620.

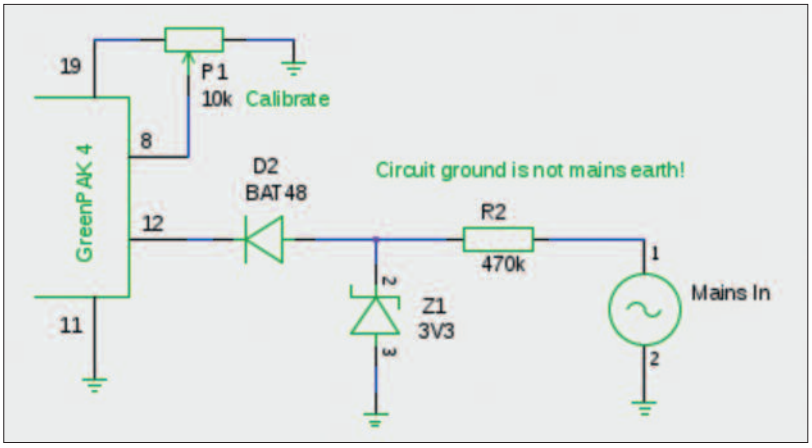



Figure 1: **Suggested input schematic**

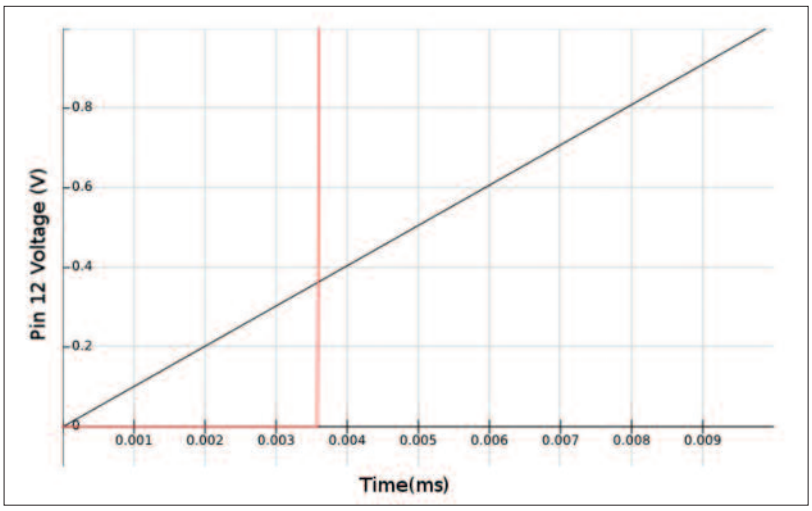



Figure 2: **The first few microseconds of a 230 V/50 Hz mains waveform**

The graph in Figure 2 shows the first few microseconds of the half-wave cycle for a 230 V, 50 Hz waveform (black curve). The error introduced by the use of a half-wave rectifier in the above fashion is quite small. Given the presence of the protective Schottky diode BAT48 at the input, we need a voltage of at most 350 mV to trigger the ACMP. The time taken for the mains voltage to reach a level of 350 mV is about 3.6µs; double that to account for the ramp-down as well, and we have a 0.07 % error which can be neglected in most mains frequency monitoring applications. The output of the ACMP is shown by the red line in Figure 2.

## Realization with the GreenPAK designer

Figures 3 and 4 show the GreenPAK

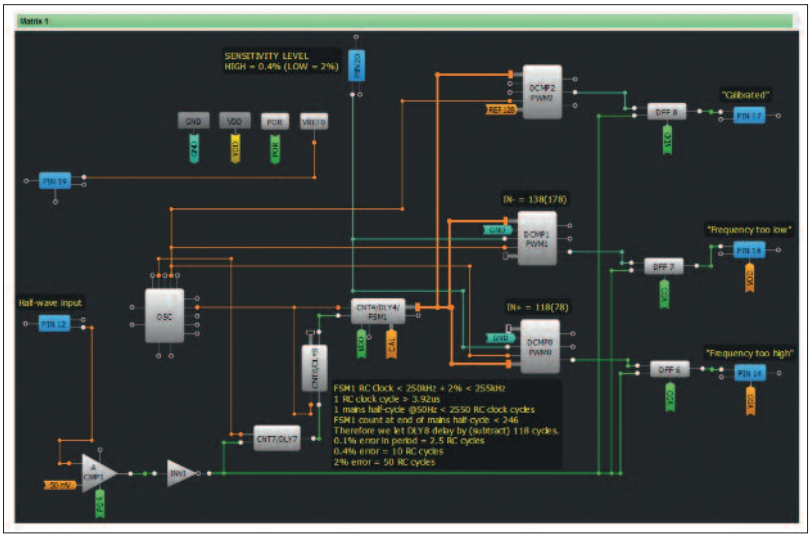



**Figure 3:** **GreenPAK Design - Matrix 1**

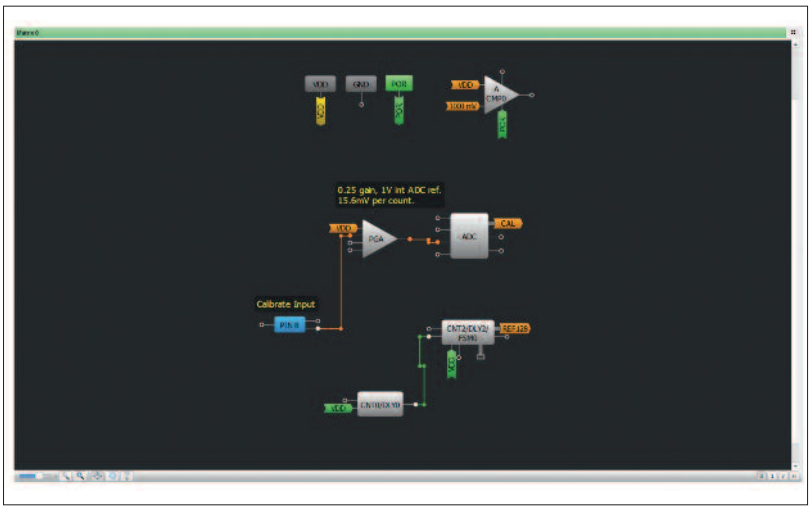



**Figure 4:** **GreenPAK Design - Matrix 0**

design. The broad idea is to drive the SET input of FSM1 low when the mains half-cycle starts, and bring it back high when the half-cycle ends. When the half-cycle ends, the rising edge produced by INV1 feeds into DFF6/7/8, locking the DCMPs' states into pins 14, 16 and 17 respectively, after which the rising edge (delayed slightly by DLY7), SETs FSM1.

To make the above strategy work in practice, we need to work around a couple of things. Firstly, we note that the GreenPAK 4's DCMP works with 8-bit data, which offers us a resolution of only 1 part in 256. What if we are interested in better accuracy than this? Secondly, the internal oscillator is not as accurate as a crystal oscillator so if we need to keep the external parts count really low we need a method of calibrating the frequency monitor. We will describe how both these are achieved.

## Oscillator and counter design

We choose OSC's 2 MHz RC oscillator. The OSC output divisor and the FSM1 clock input divisor are set to 2 and 4 respectively so that the counter frequency is now 2000/8 = 250 kHz (period = 4 µs). Let us see what happens with a nominal mains frequency of 50 Hz, with the half cycle being 10 ms. Suppose FSM1 is configured to count UP with counter data = 0. Then at the end of the 10 ms half-cycle, the Q output of FSM1 will be 10 ms/4 µs = 2500 modulo 256 = 196. Let us call this the "STOP value" for further discussion.

However we now need to take cognisance of the error in the oscillator frequency. From the device's datasheet we see that if the SLG46620 operates at a supply voltage of 3.3 V, the frequency tolerance of the 2 MHz RC oscillator at 25°C is -1.74 % / +1.55 %. Instead of adding an external crystal oscillator, we show how we can institute a calibration procedure to compensate for this variation in an actual implementation.

As a first step towards achieving this, we design things with an assumed OSC frequency that is at the upper end of the range (or a little beyond, to account for minor temperature variations). In other words, we design things in such a way that if the OSC frequency error was +2 %, then the STOP value would be 128, which is the midpoint of the possible range 0-255 of the STOP value. Knowing that the OSC error is actually less than 2 %, what this implies is that the actual STOP value will be (slightly) less than 128. The next step is to have a trimmer external to the GreenPAK which may be tweaked to "push" the actual STOP value to 128 when the input frequency is known to be exactly 50 Hz. This would give us a practical calibration procedure that can be used in the field.

Let us now work out the numbers and calculate the STOP value:

- Assumed OSC RC frequency = 2040 kHz/8 = 255 kHz
- One RC clock cycle = 3.92µs
- STOP value after 10ms = 246
- Delay introduced by DLY8 = 118 cycles
- New STOP value = 246-118=128 which is desired.

## Field calibration

When the actual OSC frequency is less than 2040 kHz, the STOP value will be somewhat less than 128. How do we now "push" the STOP value using an external trimmer? Enter the ADC (Figure 4). The ADC takes an analog voltage from Pin 8 and generates a digital value labelled CAL, that is used by FSM1 as its counter data. When the input voltage at Pin 8 is zero, the CAL value is zero. As we increase the voltage, the CAL value increases. Since FSM1 starts counting at the CAL value rather than at zero when it receives a SET signal, the STOP value also increases. We now have the following procedure for field calibration when the input signal is known to be at 50.00 Hz: the Pin 8 voltage is increased slowly from zero till the STOP value touches 128. At that point, DCMP2, whose IN- pin is fed with the constant reference value of 128 generated by FSM0, outputs a signal on its EQ output which lights up an LED on Pin 17 indicating that the unit is calibrated.

The calibraton input voltage for Pin 8 may be conveniently generated by using the $V_{REF}$ macrocell to output a reference voltage of 1 V on Pin 19 and using a trimmer as shown in Figure 1.

Now comes the relatively simple part: deciding what the reference values for DCMP0/1 should be. From the calculations we see that a 0.1 % error in mains frequency amounts to an error of 2.5 in the STOP value. For this application we have chosen selectable sensitivity levels of 0.4 % and 2 %. A 0.4 % error

equals 10 RC cycles and 2 % error equals 50 RC cycles. Correspondingly, the lower and upper limits for the DCMPs may be set to 128 +/- 10 or 128 +/- 50 depending on the sensitivity level desired. The sensitivity level is selectable using a LOW/HIGH input on Pin 20 which feed the MTRX SEL inputs of the two DCMPs which select from Register 0-3 into which the corresponding bounds are programmed.

### Implementation notes and results

For the most part, the design can be tested with emulation. The emulation signal generator has a resolution of about 1 % so it is possible to test the basic correctness of the design with a sensitivity not greater than 1 %. It is difficult to test a breadboarded unit with mains input because of the stray hum pickup at the ACMP inputs that cause spurious readings. The author has tested this design under emulation where the calibration input to Pin 8 was via emulation, and the waveform input at Pin 12 was from a Tektronix SG502 square wave generator set to 50 Hz. Time periods were verified using a Tektronix DC503A counter reading the time period at a resolution of 0.001 ms. The unit under emulation attained calibrated at a Pin8 voltage of about 440 mV, corresponding to a CAL value of about 28, after which the design worked correctly at both low and high sensitivities.

### Conclusion

In this application a simple but useful design for a mains frequency monitor has been described. The design can be used for simple alert or data collection purposes, or can be made a part of a more elaborate feedback loop or changeover/shutdown circuitry in, say, an inverter design. In a real implementation, care must be taken to lay out the circuit and provide adequate shielding so that there is no noise or hum at the ACMP input that could cause spurious triggering and affect the reliability of the unit. A demonstration can be seen at Electronica 2016, Nov. 8-11 in Munich, hall A6 booth 428.

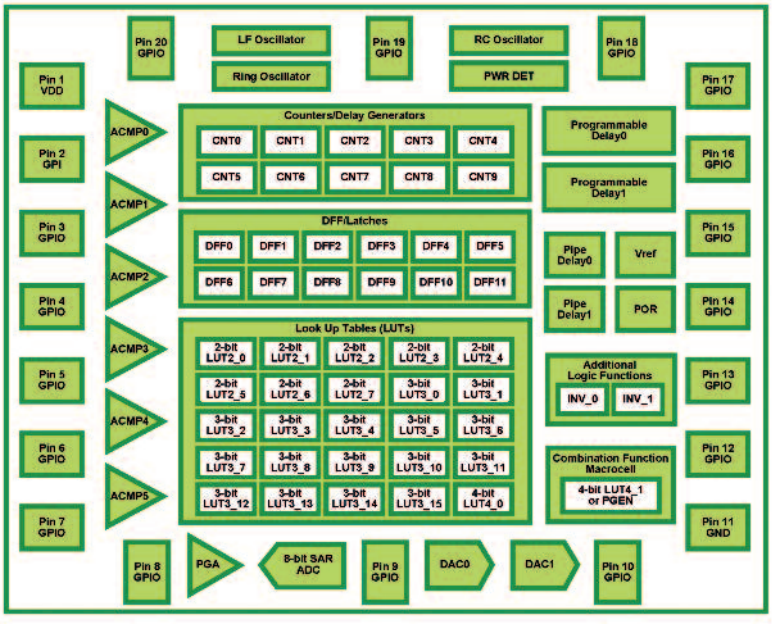
# Programming Mixed-Signal Functions

The SLG46620 provides a small, low power component for commonly used mixed-signal functions. The user creates their circuit design by programming the one time Non-Volatile Memory (NVM) to configure the interconnect logic, the I/O Pins and the macro cells. This versatile device allows a wide variety of mixed-signal functions to be designed within a very small, low power single integrated circuit.

The SLG46620 has two Connection Matrices, which are used to create the internal routing for internal digital signals inside the device, once it is programmed. The registers are programmed from the one-time NVM cells during Test Mode Operation. All of the connection points for each logic cell have a specific digital bit code assigned to it that is either set to active "High" or inactive "Low" based on the design that is created. Once the 2048 register bits are programmed, a fully custom circuit will be created.

Each Connection Matrix within the device has 64 inputs and 95 outputs. Each of the 64 inputs to each Connection Matrix is hard-wired to the digital output of a particular source macro-cell, including I/O pins, LUTs, ADC, analog comparators, other digital macro-cells and VDD and VSS. The input to a digital macro-cell uses a 6-bit register to select one of these 64 input lines. All macro-cells associated with a particular matrix has both its inputs and outputs connected to that matrix. To make connections to macro-cells associated with the other matrix, the user can select the Matrix Cross Connection lines. Each matrix has 10 dedicated output connections for connecting to the other matrix, known as the "Cross Connection "outputs. When using these cross connections, any macro-cell can be connected to any other macro-cell in the device by first going through the other matrix. As there is fixed number of the Matrix Cross Connections, it is important when making connections of the outputs of macro-cells to the inputs of other macro-cells that this is done within the same matrix whenever possible. This will leave the Matrix Cross Connection lines free for digital connections to resources associated with the other matrix.

When a design is ready for in-circuit testing, the GreenPAK development tools can be used to program the NVM and create samples for small quantity builds. Once the NVM is programmed, the device will retain this configuration for the duration of its lifetime. Once the design is finalized, the design file can be forwarded to Silego to integrate into the production process.




**Block diagram of the SLG46620**