High-Side Current Sensing Questions

Ask any experienced electrical engineer - for example Gureux, an applications engineer with 30 years of experience in our story - about what to put in front of a MOSFET gate and you will probably hear "a resistor, approximately 100 Ω." Despite this certainty, one still wonders why and questions the utility and the resistance value. Because of that curiosity, these questions will be examined in the following example. Neubean, a young applications engineer, looks to test if it is actually necessary to place a 100 Ω resistor in front of a MOSFET gate for stabilization. Gureux, monitors his experiments and gives his expert opinion along the way in the technical discussion. **Aaron Schultz, Applications Engineering Manager, Analog Devices/Linear Technology, USA**

The circuit in Figure 1 shows a typical example of high-side current sense. Negative feedback tries to force the voltage VSENSE upon gain resistor R_{GAIN}. The current through R_{GAIN} flows through P-channel MOSFET (PMOS) to resistor R_{OUT}, which develops a ground referenced output voltage. The overall gain is according to equation 1:

$$V_{OUT} = I_{SENSE} \times R_{SENSE} \times \frac{R_{OUT}}{R_{GAIN}}$$

Optional capacitance C_{OUT} across the resistor R_{OUT} serves to filter the output voltage. Even if the drain current of the PMOS quickly follows the sensed current, the output voltage will exhibit a single-pole exponential trajectory. The resistor R_{GATE} in the schematic separates the amplifier from the PMOS gate. What is the value? "100 Ω, of course!" the experienced applications engineer might say.

Trying out the appropriate resistance

Neubean, a student of Gureux's, thinks that with enough capacitance from the gate to the source, or with enough gate resistance, he should be able to cause stability problems. Once it is clear that R_{GATE} and C_{GATE} interact detrimentally, then it will be possible to debunk the myth that 100 Ω, or in fact any gate resistance, is automatically appropriate.

Figure 2 shows an example of an LTspice simulation used to highlight the circuit behavior. Neubean runs simulations to show the stability problems that he believes will occur as R_{GATE} increases. After all, the pole from R_{GATE} and C_{GATE} ought to erode the phase margin associated with the open loop. Yet, no value of R_{GATE} shows any sort of problems in the time domain response.

In looking at the frequency response, Neubean needs to take care of identifying what the open loop response is. The forward path that forms the loop, when combining the unity negative feedback, starts from the difference and ends at the resulting negative input terminal. Neubean then simulates and plots $V_S/(V_P - V_S)$, or V_S/V_E. Figure 3 shows a plot's frequency domain plot for this open-loop response. In the Bode plot of Figure 3, there is very little DC gain and no evidence of phase margin problems at the crossover. In fact, the plot overall looks very strange as the crossover frequency is less than 0.001 Hz.

The decomposition of the circuit into a control system appears in Figure 4. The LTC2063, like almost all voltage feedback op amps, starts with high dc gain and a single pole. The op amp gains the error signal and drives the PMOS gate through

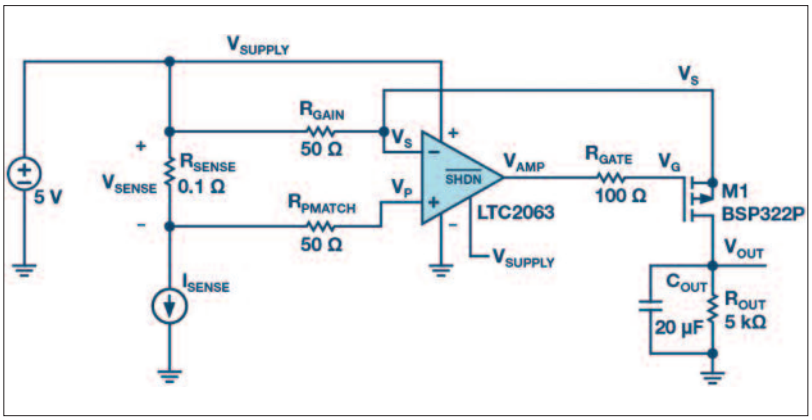

Figure 1: High-side current sense

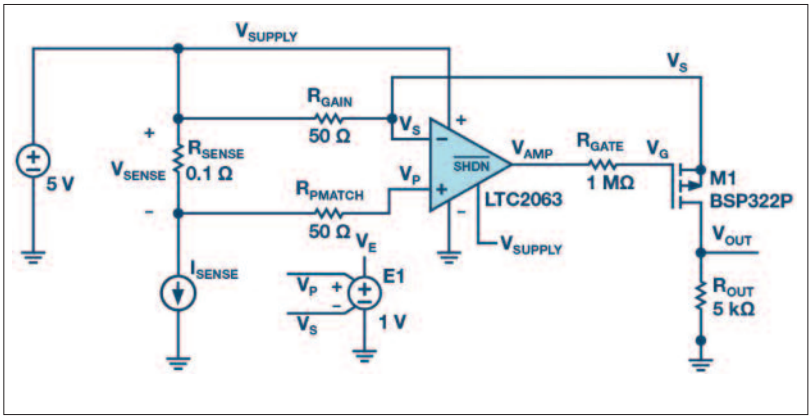

Figure 2: High-side current sense simulation

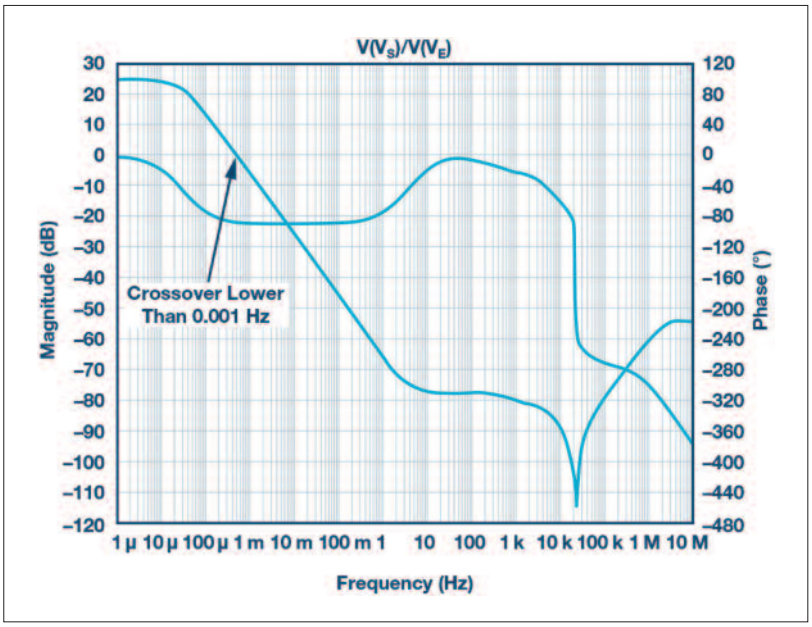

Figure 3: Frequency response from the error voltage to the source voltage

the R_{GATE} – C_{GATE} filter. The CGATE and PMOS source connect together to the –IN input of the op amp. R_{GAIN} connects from that node to the low impedance source. Even in Figure 4, it might appear that the R_{GATE} – C_{GATE} filter should cause stability problems, particularly if R_{GATE} is much larger than R_{GAIN}. After all, the C_{GATE} voltage, which directly affects the R_{GAIN} current in the system, lags op amp output changes.

Neubean offers one explanation to why perhaps R_{GATE} and C_{GATE} do not cause instability: The gate source is a fixed voltage, so then the R_{GATE} – C_{GATE} circuit is irrelevant. Adjust the gate and the source follows - it's a source follower. His more experienced colleague notes - actually, no. This is only valid when the PMOS operates normally as a gain block in the circuit. Thus Neubean writes the following equations:

$$\frac{V_S}{V_E} = \frac{A}{(1+\frac{s}{\omega_A})} \times \frac{gm \times R_1 + s \times R_1 \times C_G}{gm \times R_1 + s \times R_1 \times C_G + (1+\frac{s}{\omega_G})}$$

with

$$\omega_G = \frac{1}{R_G \times C_G}$$

op amp gain A, and op amp pole ωA.

$$\frac{V_S}{V_G} = \frac{gm + s \times C_G}{gm + s \times C_G + \frac{1}{R_1}}$$

so, what is the important term gm for a MOSFET?

$$gm = \sqrt{2 \times Kn \times Id}$$

Looking at the circuit back in Figure 1, with zero current through R_{SENSE}, the current through the PMOS ought to be zero. With zero current, gm is zero, because the PMOS is effectively off, not being used, unbiased, and has no gain. When gm = 0, V_S/V_E is 0 at 0 Hz and V_S/V_G is 0 at 0 Hz, so there is no gain at all and the plots in Figure 3 may be valid after all.

Try to Go unstable with the LTC2063

Armed with this revelation, a few simulations with non-zero I_{SENSE} have been tried.

Figure 5 shows what looks like a much more normal gain/phase plot of the response from V_E to V_S, crossing from >0 dB to <0 dB. Figure 5 should show about 2 kHz, with lots of PM at 100 Ω, a bit less PM at 100 kΩ, and even less with 1 MΩ, but not unstable.

In the lab a sense current with the high-side sense circuit LTC2063 of 100 kΩ and 1 MΩ have been inserted, expecting to see unstable behavior or at least some kind of ringing. Unfortunately, not. By increasing the drain current in the MOSFET first by using more I_{SENSE} and then by using a smaller R_{GAIN} resistance, no destabilization can be observed. Also in the simulation by filling a phase margin with non-zero I_{SENSE}, it seems difficult, if not impossible, to find instability or low phase margin.

Neubean asks Gureux why he is failing to destabilize the circuit. Gureux advises him to do the numbers. Neubean examines what might be the actual pole associated with R_{GATE} and the total gate capacitance. With 100 Ω and 250 pF, the

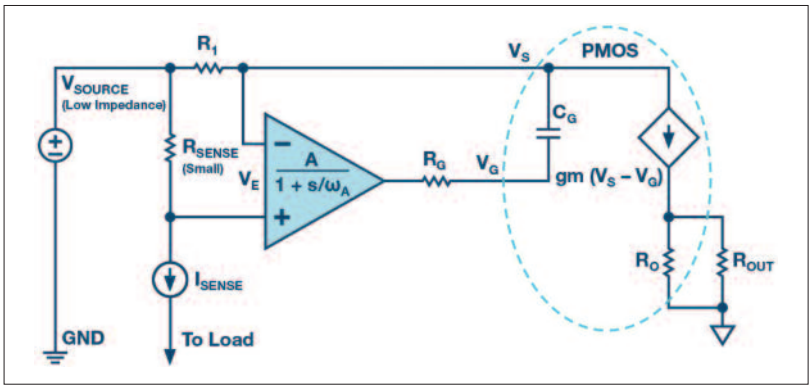

Figure 4: High-side sense circuit as a block diagram

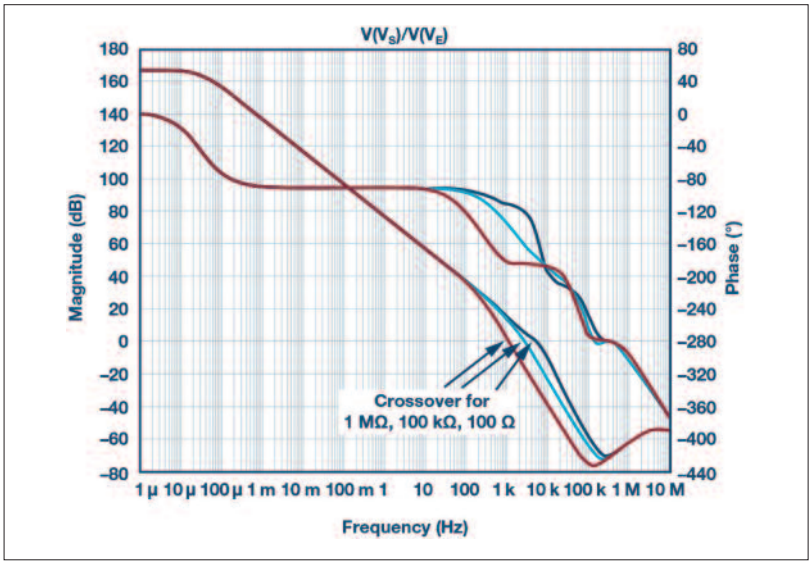

Figure 5: Frequency response from the error voltage to the source voltage, non-zero sense current

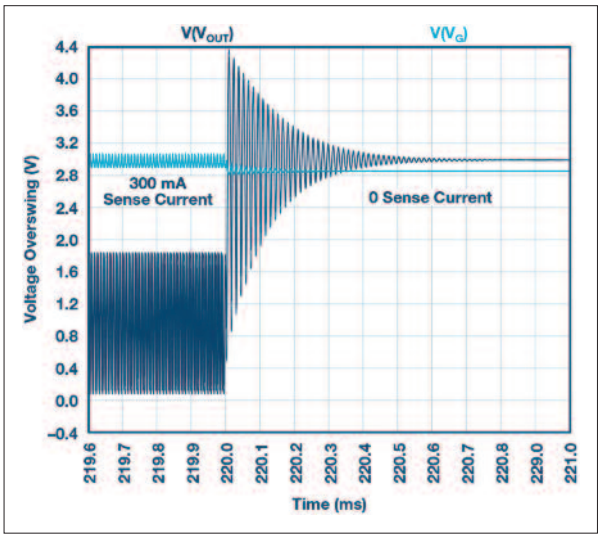

Figure 6: A time domain plot with ringing

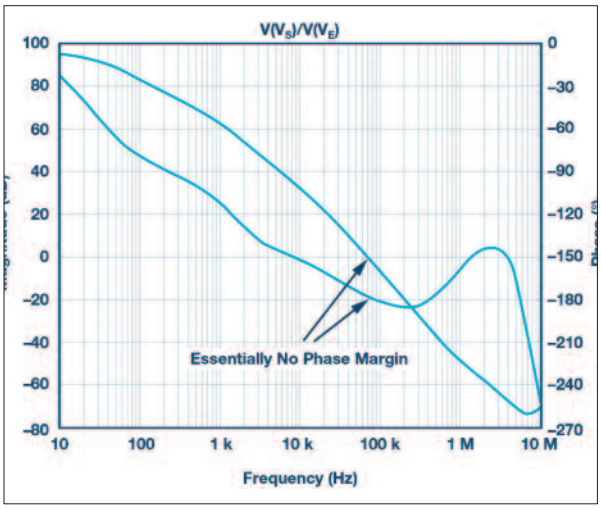

Figure 7: A normal Bode plot with added current, V_E to V_S, with terrible phase margin

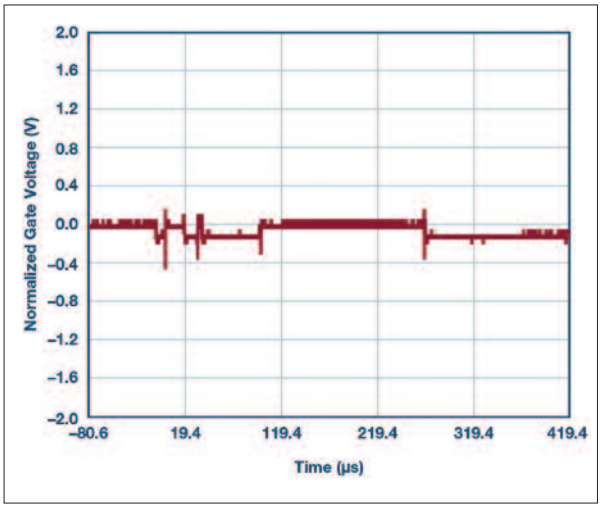

Figure 8: RGATE = 100 Ω, current from low to high transient

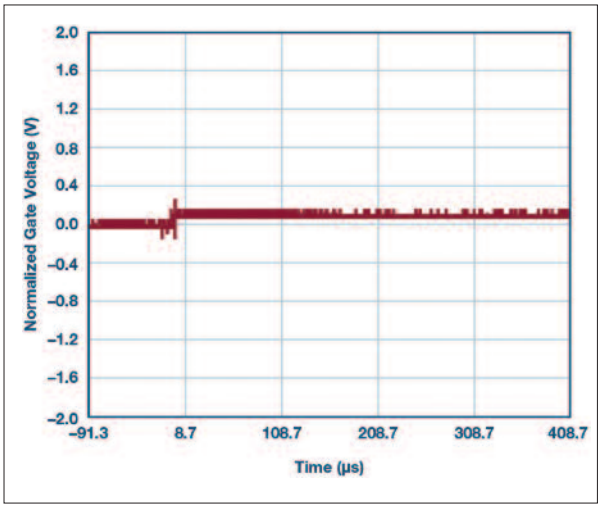

Figure 9: RGATE = 100 Ω, current from high to low transient

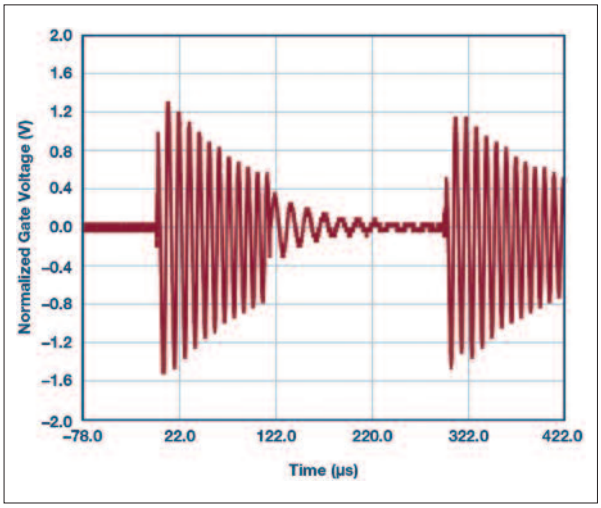

Figure 10: RGATE = 100 kΩ, current from low to high transient

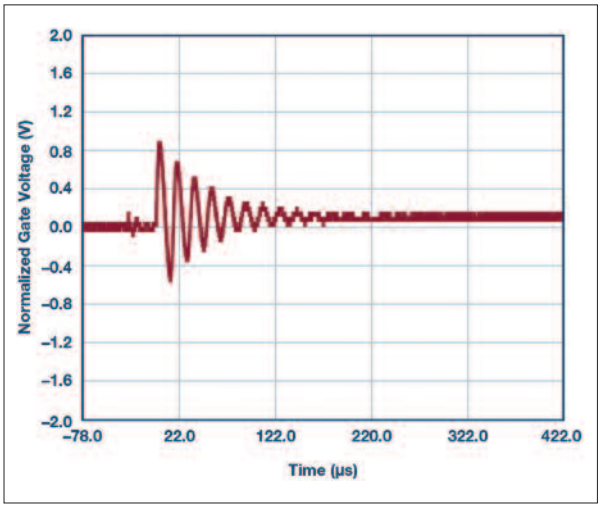

Figure 11: RGATE = 100 kΩ, current from high to low transient

pole is at 6.4 MHz; with 100 kΩ, the pole is at 6.4 kHz; and with 1 MΩ, the pole is at 640 Hz. The LTC2063 gain bandwidth product (GBP) is 20 kHz. When the LTC2063 takes gain, the closed-loop crossover frequency can easily slide below any effect of the R_{GATE} – C_{GATE} pole.

Realizing that the op amp dynamics need to continue up into the range of the RGATE – CGATE pole, a higher gain bandwidth product has been chosen. The LTC6255 5 V op amp will directly fit into the circuit with a higher 6.5 MHz GBP. Thus, a simulation with 100 kΩ gate resistance and with 300 mA sense current

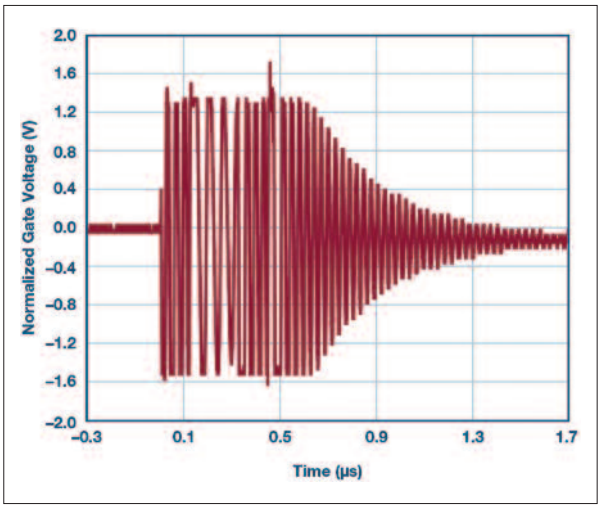

Figure 12: **RGATE = 1 MΩ, current from low to high transient**

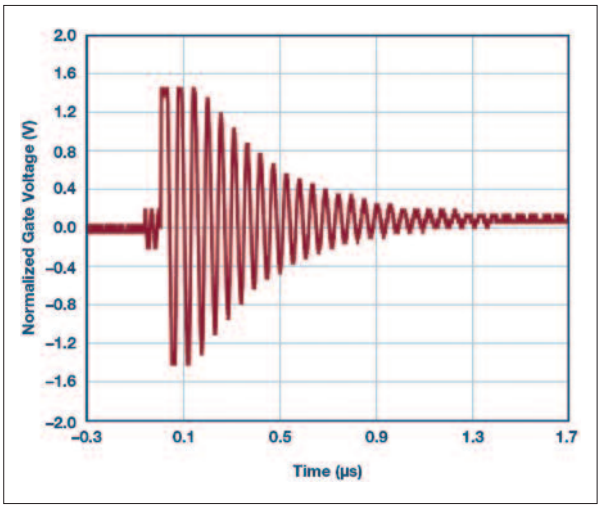

Figure 13: **RGATE = 1 MΩ, current from high to low transient**

have been tried. Neubean then proceeds to add R_{GATE} in simulation. With enough R_{GATE}, an extra pole can destabilize a circuit.

Figure 6 and Figure 7 show simulation results with high R_{GATE} values. At a constant 300 mA sense current, this simulation shows instability.

Lab results

Wanting to see if the circuit might act badly while sensing a non-zero current, Neubean tries the LTC6255 with a step changing load current and uses three different R_{GATE} values. I_{SENSE} transitions from a base of 60 mA to a higher value of 220 mA enabled by a momentary switch that brings in more parallel load resistance. There is no zero I_{SENSE} measurement, because it is already shown that the MOSFET gain is too low in that case.

Indeed, Figure 8 finally shows truly compromised stability with 100 kΩ and 1 MΩ resistors. Because the output voltage is heavily filtered, the gate voltage becomes the detector for ringing. Ringing denotes poor or negative phase margin, and ringing frequency indicates crossover frequency.

A moment to brainstorm

Neubean realizes that he has seen many high-side integrated current sense circuits and, unfortunately, there is no chance for an engineer to decide on gate resistance, because everything is inside the part. Examples that came to his mind were AD8212, LTC6101, LTC6102, and LTC6104 high voltage, high-side current sense devices. In fact, the AD8212 uses a PNP transistor rather than a PMOS FET. Thus it doesn't really matter, because modern devices already solve this problem?

The professional responds: "Let's say you want a combination of extremely low supply current and zero-drift input offset, such as in a remotely located battery-powered instrument. You might want an LTC2063 or LTC2066 as the primary amplifier. Or, perhaps, you need to measure a low level current level perhaps through a 470 Ω shunt as accurately and noiselessly as possible; in that case you might want to use the ADA4528, which has rail-to-rail input capability. In these cases you will need to deal with the MOSFET drive circuitry."

Clearly, then, it is possible to destabilize the high-side current sense circuit by using too large of a gate resistor. RGATE can in fact destabilize the circuit, but the initial inability to find this behavior drew from a wrongly formulated problem. There needed to be gain, which in this circuit required there to be non-zero signal being measured. When a pole erodes the phase margin at a crossover, ringing happens. But a 1 MΩ of added gate resistance is absurd—even 100 kΩ is crazy. It is always good to try to limit the output current of an op amp in case it tries to swing a gate capacitance from one rail to another rail. "So what value of resistance do I use?" Gureux notes confidently, "100 Ω."

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