Flying Capacitor Topology for Ultra Efficient Inverter Applications

High efficiency and reduced effort for filtering are the main arguments for three-level (3L) topologies. Actually, there are several 3L topologies used in solar applications. The limitation of all Neutral Point Clamped (NPC) three-level topologies is the fact that a 150 Hz ripple has to be filtered with DC capacitors, which are independent on the frequency of the Pulse With Modulation (PWM). With high frequency and utilization of SiC semiconductors it is possible to reduce the size of the output filter, but, however, the DC-capacitors are still required as the same size. There is an alternative Flying-Capacitor (FC) concept in which the 150 Hz ripple is not present. The basic principle of three-level (3L) and four-level (4L) inverter concept is introduced here. Michael Frisch, Director Product Marketing; Erno Temesi, Chief Engineer; Vincotech Germany and Hungary

The Neutral Point Clamped (NPC) inverters are widely used in highly efficient solar, UPS and other power electronics applications. This topology (Figure 1) provides advantages in switching losses in a reduced size of the inductor. However, there is one disadvantage to be named, which is the voltage ripple of 3x line frequency (e.g. 3 x 50 Hz => 150 Hz) in the DC bus. This results in an additional effort for DC capacitors to filter the ripple.

DC voltage ripple at NPC inverters
In symmetrical loaded three-phase systems the power is constant, $P = P_1 + P_2 + P_3$ ($P_1, 2, 3$ = power of the three power lines)

$P(t) = V_{(peak)}*I_{(peak)}*\sin(\omega t)$

The lines are shifted with $2\pi/3$.

The total power is:

$P_{tot} = V_{(peak)}*I_{(peak)}*[\sin'(\omega t) + \sin'(\omega t+2\pi/3) + \sin'(\omega t+4\pi/3)] = 1.5 * V_{(peak)}*I_{(peak)} = \text{constant}$

This is also valid for NPC. The problem is that NPC uses a third level which has to be built up by capacitors, and the charge-discharge cycle is only balanced after one sine wave of the grid frequency or 1/3 of a sine wave in the three-phase system. This leads to a ripple with 3x line frequency of usually 150 Hz.

Principle of FC inverters
Compared to NPC inverters, there is no additional external voltage level than DC voltage required, the additional level is generated in the circuit itself. The basic topology is shown in Figure 2. The capacitors are charged in order to provide the voltage for the three levels:

1. V(DC+): $V_{dc}$
2. V(FC): $1/2xV_{dc}$
3. V(DC-): 0 V

In case of 1200 VDC voltage C(F) is charged with 600V C(F1).

The three levels are: V(DC+): 1200 V, V(FC) = 600 V, V(DC-) = 0 V. The switching sequence is controlled in a way that the FCs are kept on the same voltage. The capacitor is charged and discharged within the defined voltage limits in the operation.

Excitation in Level 1 and freewheeling in Level 2: During the excitation the upper switches T1, T2 are turned on. For the freewheeling one of the two switches is turned off. For a balanced system the switches are alternating. In every freewheeling cycle a different switch is turned off.

The switching frequency in the switches is only half of the frequency at the inductor. This leads to identical load and losses in all switches. The optimum for all switches regarding static losses and switching losses is the same. This is also valid in reactive power and reverse power direction.

The switching sequence of a 3L FC inverter and charging / discharging status of the FC is shown in Tables 1/2.

Every first freewheeling cycle is charging and every second is discharging the FC. The capacitor is in average at the same voltage. In long term the asymmetry in the circuit might cause an imbalance of the capacitor voltage. The target voltage is 1/2 of the DC voltage.

Here is a simple logic for balancing - the target voltage of the FC is half of the DC voltage:

- if V(FC) < 1/2xV(DC) => charge FC, use Level 2.1 for freewheeling => turn off T2
- if V(FC) > 1/2xV(DC) => discharging FC, use Level 2.2 for freewheeling => turn off T1

It is also possible to use the same PWM.
sequence as for a standard NPC inverter and just assign the turn-off signal to the right switch according to this logic.

For the balancing the charging status of the FC is required. The following information is needed for a proper controlling of the voltage in the FC:

- $V(FC) < \frac{1}{2}x V(DC)$
- $V(FC) > \frac{1}{2}x V(DC)$

This is possible without an expensive isolation amplifier. In Figure 3 it is shown that with a voltage divider and a differential amplifier it is possible to compare the voltage of the DC capacitor and the FC, and to provide the data if the voltage in the FC is above or below the target. A simple optocoupler is able to send the information to the microcontroller.

**Principle of 4L FC inverters**

Here the four-level flying-capacitors are further discussed. The basic topology is shown in Figure 4.

The capacitors are charged in order to provide the voltage for the four levels:

1. $V(DC+): V_{dc}$
2. $V(FC1): \frac{2}{3}x V_{dc}$
3. $V(FC2): \frac{1}{3}x V_{dc}$
4. $V(DC-): 0V$

In case of 1200V DC voltage, the capacitors are charged with 800 V $C(F1)$ and 400 V $C(F2)$.

The four levels are: $V(DC+)$ = 1200 V, $V(FC1)$ = 800 V, $V(FC2)$ = 400 V, $V(DC-)$ = 0V.

The switching sequence is controlled in a way that the FCs are kept on the same voltage. The capacitors are charged and discharged within the defined voltage limits in the operation.

At real mode, in the positive half-wave there are two different sections of switching, the sinusoidal grid voltage $V(t) > 1/3x V_{DC}$ and $V(t) < 1/3x V_{DC}$:

1. $V(t) > 1/3x V_{DC}$: Excitation in level 1 and freewheeling in level 2. During the excitation the upper switches T1, T2, T3 are turned on. For freewheeling one of the three switches is turned off. For a balanced system in every freewheeling cycle a different switch is turned off.
2. $V(t) < 1/3x V_{DC}$: Excitation in Level 2 and freewheeling in Level 3. During the excitation two of the three upper switches are turned on. For freewheeling only one. To avoid additional switching losses we have the additional frame condition to change the switching status only for one switch at one time. The result is that the PWM frequency is reduced to 1/3 per switch, but all three switches are involved (Figures 5/6).

<table>
<thead>
<tr>
<th>Table 1: The switching sequence of a 3L FC inverter</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
</tr>
<tr>
<td>------------------</td>
</tr>
<tr>
<td>Real Power Level 1</td>
</tr>
<tr>
<td>Level 2.1</td>
</tr>
<tr>
<td>Level 2.2</td>
</tr>
<tr>
<td>Level 1</td>
</tr>
<tr>
<td>Level 1</td>
</tr>
</tbody>
</table>

| Table 2: Switching sequence of a 3L FC inverter and charging / discharging status of the FC7 |

Figure 3: Voltage detection in 3L FC inverter

Figure 4: Topology of 4L FC inverter

Figure 5: FC gate signal level 1, 2

Figure 6: FC gate signal level 2, 3
The switching frequency in the switches is only one third of the frequency at the inductor. This leads to identical load and losses in all switches. The optimum for all switches regarding static losses and switching losses is the same. This is also valid in reactive power and reverse power direction. Operation at real power (positive half-wave) is shown in Tables 3/4.

In a sequence of three times excitation and freewheeling there are one (Level 1-2 / 4-3) or two (Level 2-3) cycles of charging / discharging the FC capacitors. Charging and discharging of the FC is compensating each other, so that the voltage of the FC will stay within the functional limits (e.g. +/- 10% of the DC voltage). In the long run the tolerances will lead to some imbalance in the FC’s and have to be compensated.

Here is a simple logic for balancing - the target voltage of the FC is:

\[
\begin{align*}
V(F1) &= \frac{2}{3} \times V(DC); \ X1 = \frac{V(F1)_{\text{actual}}}{V(F1)_{\text{target}}} \\
V(F2) &= \frac{1}{3} \times V(DC); \ X2 = \frac{V(F2)_{\text{actual}}}{V(F2)_{\text{target}}}
\end{align*}
\]

There are the following possible situations:

- \(X1 > 1, X2 > 1\) => discharge FC1, FC2
- \(X1 < 1, X2 > 1\) => charge FC1, discharge FC2
- \(X1 > 1, X2 < 1\) => discharge FC1, charge FC2
- \(X1 < 1, X2 < 1\) => charge FC1, FC2

The circuit switches between Level 1 and the three different Level 2 options. During Level 1 it has to be decided which option will be taken - example:

- \(X1 > 1\) => discharge FC1 (repeat level 1 / level 2.1)
- \(X1 < 1\) => avoid discharge FC1 (skip level 2.1)
- \(X2 > 1\) => avoid charge FC2 (skip level 2.3)
- \(X2 < 1\) => charge FC2 (repeat level 1 / level 2.3)

The balancing at Level 2-3 is more complicated, because there are three different options for Level 2, and three different options for Level 3. Another frame condition is that only one switch is changing its state during one switching cycle. The goal is now to add a charge or discharge cycle for one capacitor without changing the voltage of the second capacitor. This is possible, if a short sequence is repeated where the targeted capacitor is getting the additional cycle (charge or discharge) but the other capacitor is getting the same cycles for both (charge/discharge).

Example:

- \(X1 > 1\) => discharge FC1 (level 3.3 => 2.1 => 3.2 => 2.1 => 3.3...)
- \(X1 < 1\) => charge FC1 (level 2.2 => 3.1 => 2.3 => 3.1 => 2.2...)
- \(X2 > 1\) => discharge FC2 (level 3.2 => 2.2 => 3.1 => 2.2 => 3.2...)
- \(X2 < 1\) => charge FC2 (level 3.1 => 2.3 => 3.3 => 2.3 => 3.1...)

Table 3: Operation of 4L FC inverter at real power

Table 4: 4L FC inverter switching sequence
It is now possible to change the switching sequence in order to compensate the imbalance with this input. Every switching sequence has the actual condition of $X_1$ and $X_2$ and an expected result after execution of the next switching cycle. If the expected result is not achieved, the cycle will be repeated one time. The signal at the output filter is not affected, it is the same as without the additional balancing sequence (see Tables 5/6).

**Table 5: Levels 1-2.3**

<table>
<thead>
<tr>
<th>Level</th>
<th>T1</th>
<th>T2</th>
<th>T3</th>
<th>V(OUT)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Level 1</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>1200V</td>
</tr>
<tr>
<td>Level 2.1</td>
<td>OFF</td>
<td>ON</td>
<td>ON</td>
<td>800V</td>
</tr>
<tr>
<td>Level 1</td>
<td>ON</td>
<td>OFF</td>
<td>ON</td>
<td>1200V</td>
</tr>
<tr>
<td>Level 2.2</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
<td>800V</td>
</tr>
<tr>
<td>Level 2.3</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>800V</td>
</tr>
</tbody>
</table>

**Table 6: Levels 2.1 – 3.3**

<table>
<thead>
<tr>
<th>Level</th>
<th>T1</th>
<th>T2</th>
<th>T3</th>
<th>V(OUT)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Level 3.3</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>400V</td>
</tr>
<tr>
<td>Level 3.1</td>
<td>OFF</td>
<td>OFF</td>
<td>ON</td>
<td>800V</td>
</tr>
<tr>
<td>Level 3.2</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>800V</td>
</tr>
</tbody>
</table>

**Voltage measurement in the 4L FC**

Analog voltage measurement requires additional effort in isolated measurement. Fortunately, only the ratio between the DC voltages ($V_{FC1} = 2/3 \times V_{DC}$ and $V_{FC2} = 1/3 \times V_{DC}$) is required, or if the voltage is fixed, it would be enough to detect if the voltage in the FC is above or below a fixed target voltage. Figure 7 shows a proposal for a detection of the target voltage ratio.

**Conclusions**

The special features of FC inverters are:

- **No requirement to provide additional external voltage levels,** the switching level
- **No presence of low frequency ripple** (150 Hz)
- **Inductor frequency is 2x (3L) 3x (4L)** switching frequency of the individual switches
- All switches are loaded identical during one output sine wave
- The balancing of the FC voltage is possible with low effort in the circuit design and cost (voltage detection and switching sequence)

The utilization of the listed features open opportunities for high efficient FC inverter ideas.

**Literature**


A. Ruderman, B. Reznikov, "Simple Analysis of a Flying Capacitor Converter Voltage Balance Dynamics for DC Modulation" EPE/PEMC 2008, Aachen, Germany