The Next Innovations in Interleaved PFC Control

Over the years many innovative power factor correction (PFC) techniques have been developed. One of the first innovations was active power factor correction using a boost topology. This increased power densities by removing the need for bulky passive PFC solutions. Another innovation was a transition mode PFC. It removed the reverse recovery current in the boost diode of the PFC pre-regulator, which reduced the converters switching losses and improved systems efficiency. The next step in power factor correction to increase power densities and improve system efficiency is interleaving PFC pre-regulators. This article reviews some of the benefits of interleaved PFC, along with control techniques that can be used to increase power densities, improve system efficiency, and reduce system costs. **Michael O'Loughlin, Applications Engineer, Texas Instruments, USA**

Power supply designers have been designing interleaved PFC converters for a few years now. However, the power supply's control had to be done discreetly because controllers were not available. To make interleave PFC designs easier, two PFC controllers have been developed: one for interleaved average current mode pre-regulators UCC28070 (Figure 1); and the other for interleaved transition mode pre-regulators (UCC28060).

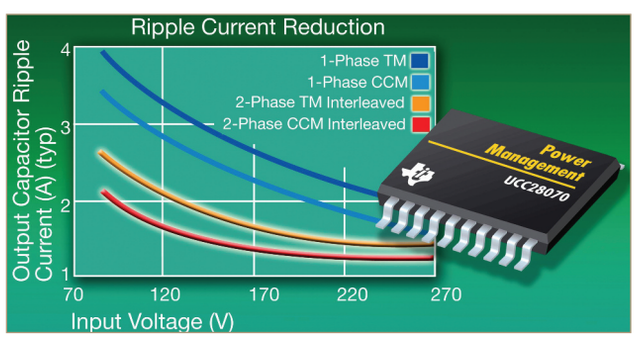

Figure 1: New PFC controller for interleaved average current mode pre-regulators

Interleaved PFC boost pre-regulator

The interleaved PFC boost pre-regulator (Figure 2) is simply two PFC boost converters operating 180° out-of-phase with each other. This technique reduces the input current (I_{IN}) caused by the inductor currents (I_{L1} and I_{L2}). Because the inductors high-frequency ripple currents are out-of-phase, they cancel each other out – reducing the input ripple current caused by the boost inductors' currents. The inductor ripple current cancellation allows for paralleling boost PFC pre-regulators while decreasing input ripple caused by the boost inductors. This technique can lead to less total inductor boost volume and/or a reduction in the size of the EMI filter. Interleaving PFC pre-regulators also have roughly 50% less high-frequency output capacitor root mean square (RMS) current (I_{COUT}) compared to a single-stage topology. The reduction in high-frequency boost capacitor RMS current can result in up to a 25% reduction in boost capacitor volume. This is not to be confused with the amount of capacitance required by the design. Typically, the amount of capacitance required by the converter is based on hold-up requirements.

Interleaving PFC pre-regulators can

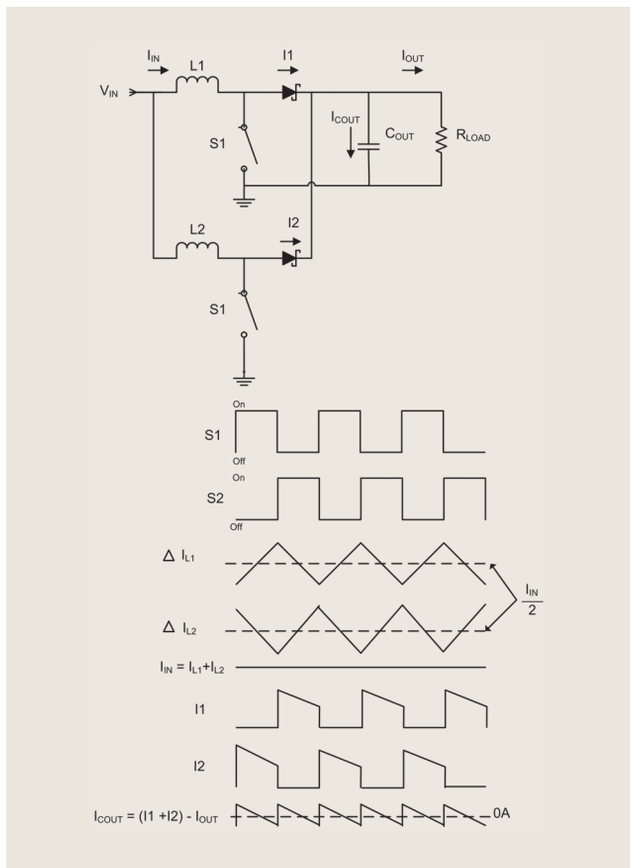

Figure 2: Interleaved boost stage

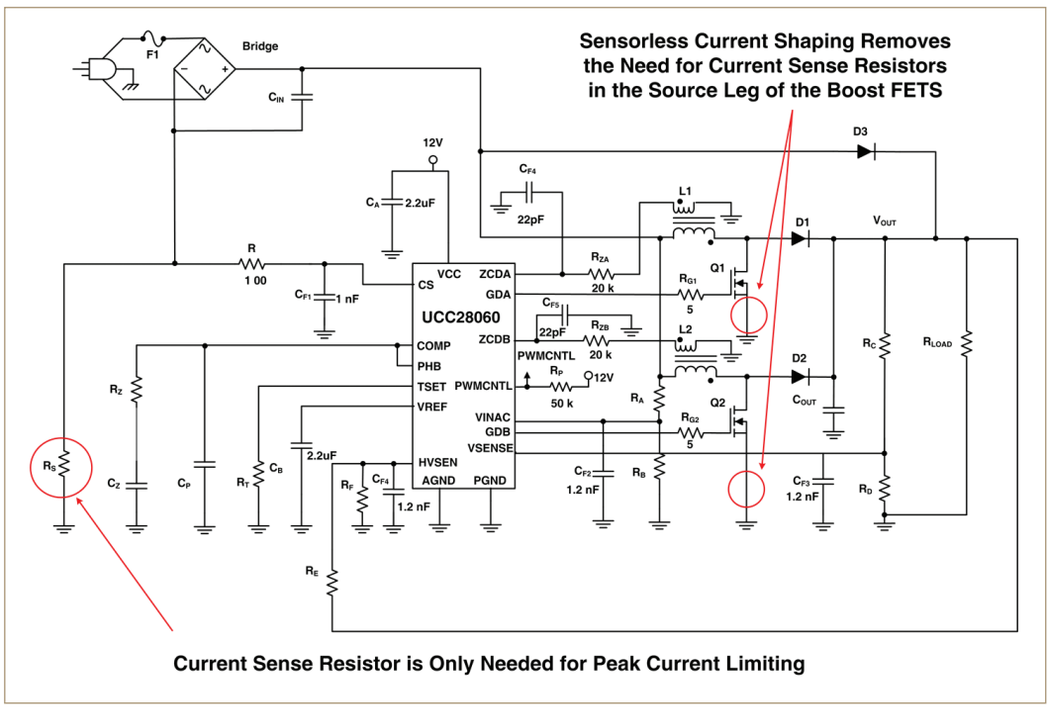

Figure 3: Transition mode interleaved PFC

reduce the total inductor energy required by the design by up to 50%, compared to a single-stage pre-regulator. To show how this is possible, we can study the equations 1a/b/c for the inductor energy required for a single stage PFC ($E_{SINGLE(L)}$), and the total inductor energy required by an interleaved PFC ($E_{INTERLEAVED(L1+L2)}$):

$$E_{SINGLE(L)} = \frac{1}{2}LI^2 \quad (1a)$$

$$E_{INTERLEAVED(L1+L2)} = \frac{1}{2}L\left(\frac{I}{2}\right)^2 + \frac{1}{2}L\left(\frac{I}{2}\right)^2 = \frac{1}{4}LI^2 \quad (1b)$$

$$E_{Single(L)} = 2E_{Interleaved(L1+L2)} \quad (1c)$$

If the same inductance is used in both designs for the same power level, the total inductor energy required by the interleaved design would be half of what is required in a single-stage design. In practice, the energy reduction by interleaving could lead up to a 32% reduction in magnetic volume.

Interleaving PFC pre-regulators can reduce conduction losses by up to 50% when compared to a single-stage power factor corrected converter. This can be observed by comparing the conduction losses for a single-stage PFC ($P_{CONDUCTION\_SINGLE}$) to the total conduction losses of an interleaved PFC ($P_{CONDUCTION\_INTERLEAVED}$). The reduction in conduction losses should make the interleaved PFC pre-regulator more efficient at higher power levels, where conduction losses dominate according to equations 2a/b/c:

$$P_{CONDUCTION\_SINGLE} = I^2R \quad (2a)$$

$$P_{CONDUCTION\_INTERLEAVED} = \left(\frac{I}{2}\right)^2 R + \left(\frac{I}{2}\right)^2 R = \frac{I^2}{2}R \quad (2b)$$

$$P_{CONDUCTION\_SINGLE} = 2P_{CONDUCTION\_INTERLEAVED} \quad (2c)$$

In the past, power supply designers were forced to interleave PFC pre-regulators with discrete control solutions. To aid power supply designers with interleaved designs, TI created two interleaved PFC controllers. The first is the UCC28060 controls, which interleaves two transition mode PFC pre-regulators. This IC does not just interleave two transition mode PFC controllers. It also uses constant on-time control, which does not require current sensing for current shaping. This technique removes the need for current sense resistors in the source legs of the boost FET. Current sensing is required only for peak current limiting to protect the boost FETs. The peak current limit comparator was designed to trip at 200mV, which is less than a sixth of the current sense signal that is typically required by transition mode PFC controllers. This innovation drastically reduces conduction losses due to current sensing (see Figure 3 for a schematic of interleaved PFC pre-regulator using the UCC28060 control IC).

Even though interleaving PFC pre-regulators can improve efficiency by reducing conduction losses, it will actually reduce the converters light load efficiency where switching losses ($P_{SWITCHING}$) dominate. Equation 3 describes the two-phase interleaved boost diodes and boost FETs switching losses, where V_{DS} and I_{DS} are the FET drain to source switching voltage and FET drain current, respectively. Variables t_r and t_f are the FET's drain to source rise and fall times. C_{oss} is the FET's parasitic drain to source capacitance. Q_g is the FET's gate charge, and V_g is the gate drive voltage applied to the FET's gate drive to activate it. Variable f_s represents the converters switching frequency, while I_{rr} represents the boost diodes reverse recovery current.

$$P_{SWITCHING} = 2\left(I_{DS}V_{DS}\left(t_r + t_f\right)f_s + \frac{C_{oss}\times\left(V_{DS}\right)^2 f_s}{2} + \frac{V_g}{2}Q_g f_s + I_{rr}V_{BOOST} f_s\right) \quad (3)$$

This equation shows that the losses caused by total C_{OSS}, Q_g and I_{rr} are double what they would have been in a single-stage PFC pre-regulator. To increase efficiency at lighter load conditions, it would be beneficial to turn one of the interleaved phases and go into single phase operation. To increase light load efficiency, the UCC28060 has optional built-in phase management circuitry to increase light load efficiency. By enabling this function the systems light load efficiency can be increased by 1% to 3%.

Interleaving two average current mode PFC boost stages

The second control IC designed for interleaved PFC is the UCC28070 interleaving two average current mode PFC

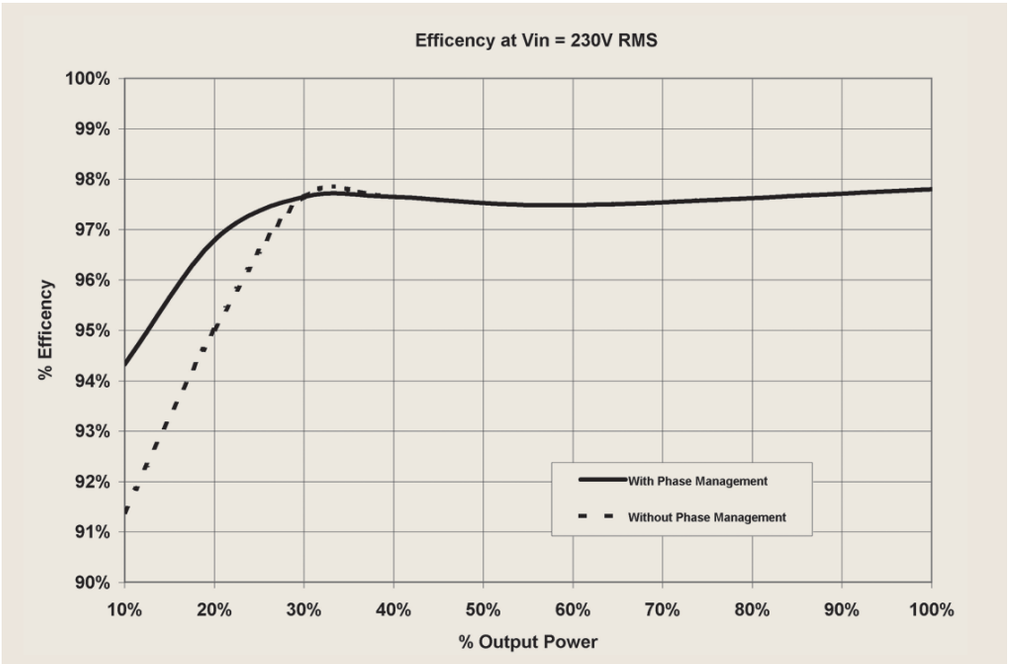

Figure 4: **Efficiency improvement with phase management**

boost stages. To ensure the highest efficiency possible in the pre-regulator, this IC works with current sensing via current sense transformer and operates with a single voltage loop and two separate current loops.

A PFC boost pre-regulator using current sense transformers typically requires current sensing in the boost diode (D1), and the boost switch (Q1). The current sense circuitry generally consists of two current sense transformers (CT1 and CT2), two rectifier diodes (D), two reset resistors (R_R), and one current sense resistor (R_S) resistor (see Figure 5). In an interleaved PFC pre-regulator configuration current sensing would have to be done in each phase. To reduce system costs, TI developed a current synthesis technique to synthesize the boost diode current by removing the need to sense the boost diode current. This removes the need of a current sense transformer (CT2), a rectifier diode, and a reset resistor.

Conclusion

Interleaving PFC pre-regulators can increase power densities by reducing capacitor volume and total inductor volume. Interleaving power converters can lower conduction losses, improving the overall system efficiency. In the past, power supply designers had to do the interleaved PFC control discreetly because PFC controllers were not available. To aid in the design process and to help make interleaved PFC control simpler, TI developed two interleaved PFC controllers. The UCC28060 was designed for transition mode interleaved PFC with built-in phase management to improve light-load efficiency. The UCC28070 was designed for interleaved average current mode PFC, which has an innovative current synthesis technique that reduces system costs by reducing the amount of components needed for current transformer current sensing.

Literature

More PFC Performance, Power Electronics Europe 8/2007, page 6

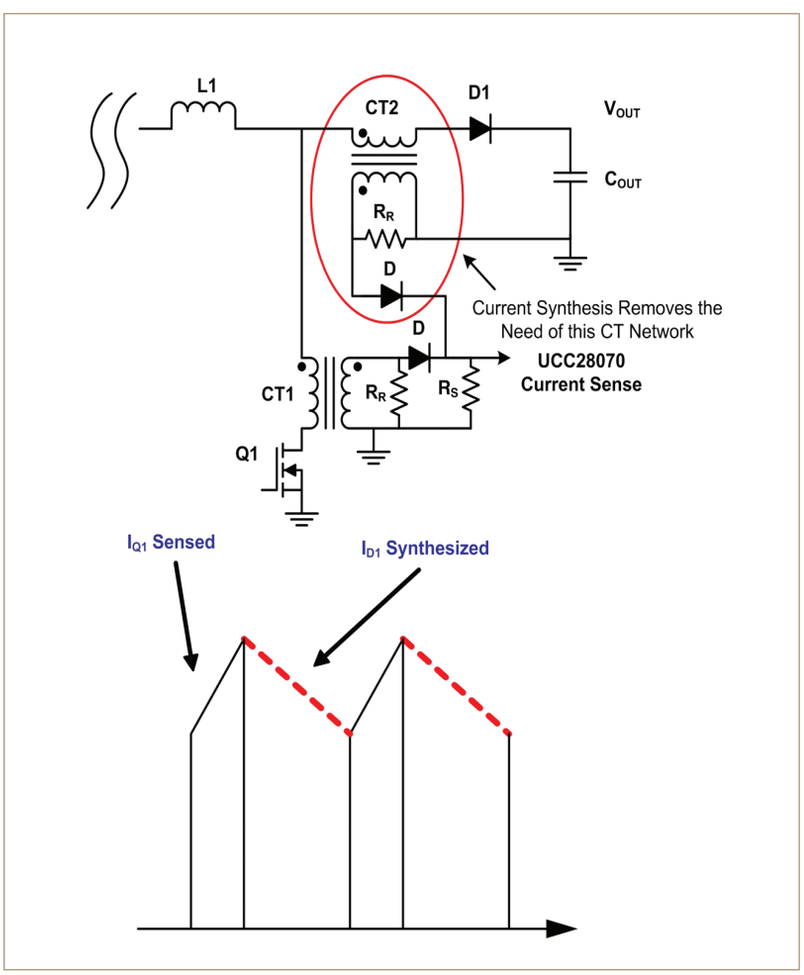

Figure 5: **Current synthesis reduces current sense transformer count**