Emulated Peak Current Mode Enhances PWM Current Mode Operation

Great steps have been made in recent years in process technology to enhance the performance of power converters. Improved switching devices have boosted efficiency, allowing faster switching frequency and increased power density. All of these technology improvements are useless without a careful and scrupulous analysis of the application, and the inherent applicable limitation of the control scheme adopted in the design. This article summarises the practical restriction of the classic pulse-width modulation (PWM) current mode scheme and highlights the inherent advantages of the more novel emulated current mode solution. **Michele Sclocchi and and Werner Berns, National Semiconductor Italy and Germany**

High power density design and better copper utilisation force system designers to distribute higher-level unregulated input voltage buses and design local step-down converters at the point where a regulated voltage is needed.

Typically, when isolation is not required, the buck topology provides the lowest cost solution and easiest implementation. The most important characteristics such as a buck converter solution can be summarised as follows: easy implementation with limited number of active components; high efficiency and good thermal dissipation capability; high power density with small external components; design flexibility, with the possibility to synchronise multiple buck regulators to the most suitable switching frequency; high noise immunity; wide input voltage range with fast line transient responds; fast load transient responds from minimum to maximum load and vice-versa; and high DC accuracy, reduced output window regulation and low ripple noise.

High power density and high efficiency

These points can be addressed by choosing the maximum allowed switching frequency compatible with the overall target efficiency, the ambient temperature, and the maximum junction temperature of the active components.

The total power losses of the switching regulator can be estimated by the sum of three contributes - the bias losses, which are mainly the ground pin current (I_q) times the input voltage (V_{in}) according to equation 1:

$$P_{bias} = I_q \cdot V_{in} \quad (1)$$

The power conduction losses are the losses built in the transistor while fully turned on (equation 2):

$$P_{cond} = D \cdot R_{dson} \cdot Iout^2 \quad (2)$$

where D is the duty cycle, R_{dson} is the on-state resistance of the internal MOSFET, Iout is the maximum output current.

The switching losses are the losses that occur during the transition time of the internal MOSFET (equation 3):

$$P_{switch} = (Iout \cdot V_{in} / 2) \cdot freq \cdot (t_{LH} + t_{HL}) \quad (3)$$

where freq is the selected switching frequency, t_{LH} and t_{HL} are respectively on and off transition time of the internal MOSFET.

The total regulator's losses are the sum of the above three individual losses (equation 4):

$$P_{regulator} = P_{bias} + P_{cond} + P_{switch} \quad (4)$$

Finally, the power losses of the external schottky diode can be estimated by the off-duty-cycle-time (1-D), maximum output current and its forward drop voltage V_{fw} (equation 5):

$$P_{diode} = Iout \cdot (1 - D) \cdot V_{fw} \quad (5)$$

The operating switching frequency can be selected in order to meet the overall target efficiency and the maximum junction temperature (T_j) of the IC, estimated with equation 6:

$$T_J = T_{amb} + P_{regulator} \cdot \theta_{JC} \quad (6)$$

where T_{amb} is the maximum ambient temperature and Θ_{JC} is the junction to case thermal resistance.

Unfortunately, it is difficult to precisely estimate the junction temperature and overall efficiency, since there are many other factors to be taken into account, like switching times, PCB dissipation and thermal interaction with the external diode losses located very close to the switching regulator.

Figure 1 shows a typical configuration of an industrial application, where four independent outputs are obtained from a 36V input bus using the LM5574, LM5575, LM5576 regulators. All four converters operate at same switching frequency of 500kHz synchronised to the same clock. Synchronising all the controllers to the same frequency reduces system noise and radio frequency interference. Multiple LM5576 devices can be synchronised simply by connecting the Sync. pin together, and all the devices will be synchronised to the highest frequency device.

Various control schemes

Fast load and line transient responds are synonymous with a fast control loop system obtained with scrupulous close loop

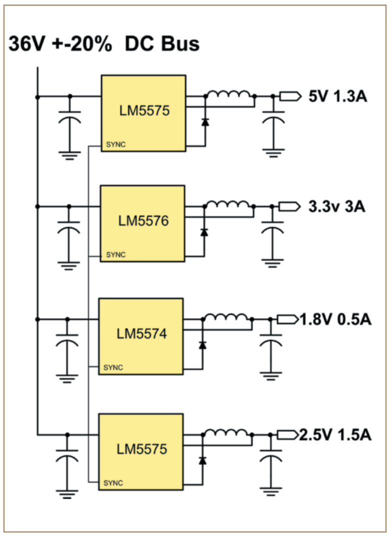

Figure 1: Typical four output step down converter powered form a 36V bus, with all switching frequency synchronised to the same clock

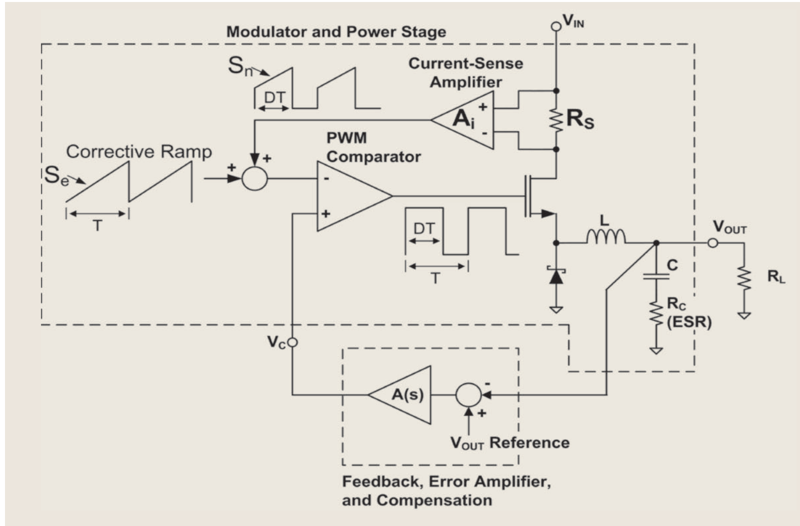

Figure 3: Current mode buck regulator basic architecture, used in Simple Switchers LM267x

compensation design and an excellent PWM control scheme.

The most common controller is the classic PWM scheme, where an internal clock leads the beginning of each duty cycle, which corresponds to the start of the ON transition of the main MOSFET. The off-time is timed by the control voltage V_c compared with a saw-tooth ramp V_P (see Figure 2). The saw-tooth ramp has been generated by three different methods, voltage mode, voltage mode feed-forward, and current mode control schemes and is now expanded with a forth control scheme - emulated current mode. To better understand the differences, let's have a look at the traditional methods first.

The classical voltage mode controller generates internally a constant sawtooth ramp and has a constant amplitude. Voltage mode avoids the complications of slope compensation required with current mode control; it is less susceptible to noise and can operate with very short on-time. The loop gain and the bandwidth increase with the increase of the input voltage. Voltage mode is widely used for its simplicity in low output current applications, where the input line is relatively stable with slow line transients.

The voltage mode feed-forward controller features basically the same control scheme as the classic voltage mode, but with improved performance on line transient response. This is obtained by varying the amplitude of the sawtooth proportional to the input voltage. This results in an inherent duty cycle change caused by a change of V_{in} and thus, better line transient response.

Rather than using a constant sawtooth ramp to control the duty cycle, traditional current mode control uses the sawtooth ramp generated by the output inductor current (see Figure 3). A current sense amplifier detects the inductor current by measuring the current on the main MOSFET when it is conducting. A fixed corrective ramp is added to avoid the problem of sub-harmonic oscillation when the duty cycle is over 50%. At the beginning of a switching period, the switch is turned on, and the inductor current is sensed by R_s and the current sense amplifier. This current sense signal is added to a corrective ramp, and when the sum of these two waveforms exceeds V_c, the comparator output goes low, turning the output switch off.

Current mode control offers several advantages, such as good current sharing between phases connected in parallel, better compensation due to the single pole of the L-C output filter, precise cycle by cycle current limit, and immunity to input disturbance.

One of the main disadvantages of current mode control is the difficulty in measuring the current with small duty cycle. This measurement can be quite susceptible to noise and the modulation can be erratic at times. Propagation delays and noise susceptibility make it almost impossible to use conventional current mode control for high input voltage, large step-down buck regulator applications where very small on-times are required.

The challenge of accurate switch current measurement in high frequency buck converters can be avoided with a new method that emulates the buck switch current.

The inductor current can be reconstructed by measuring the current at the end of the switching cycle in the free-wheeling diode and adding on top of it a ramp that is proportional to the current ramp in the inductor. To emulate the ramping portion of the inductor's current, an external capacitor is charged with a constant current proportional to the difference between the input and the output voltage. The resulting ramp voltage at the capacitor is proportional to the ramping current in the inductor itself (see Figure 4).

Emulated peak current mode offers all the intrinsic advantage of a classic current mode controller without the noise susceptibility problem often encountered from diode reverse recovery current, ringing on the switch node and current measurement propagation delays, while

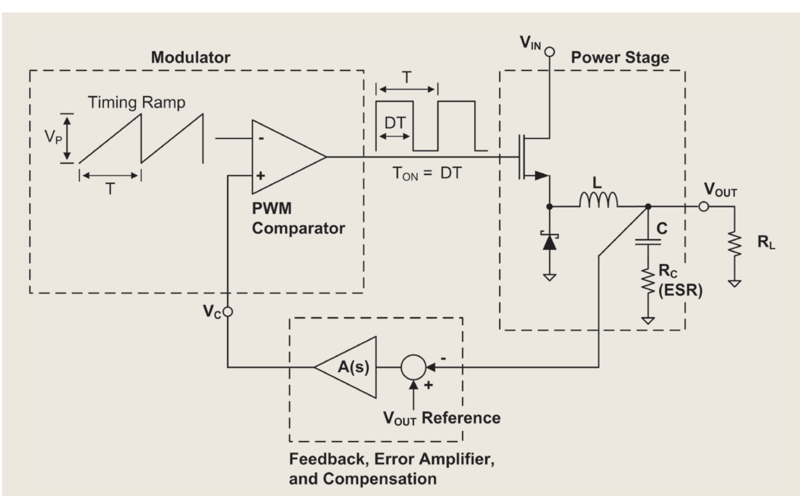

Figure 2: Voltage mode buck regulator basic architecture used in Simple Switchers LM257x and LM259x

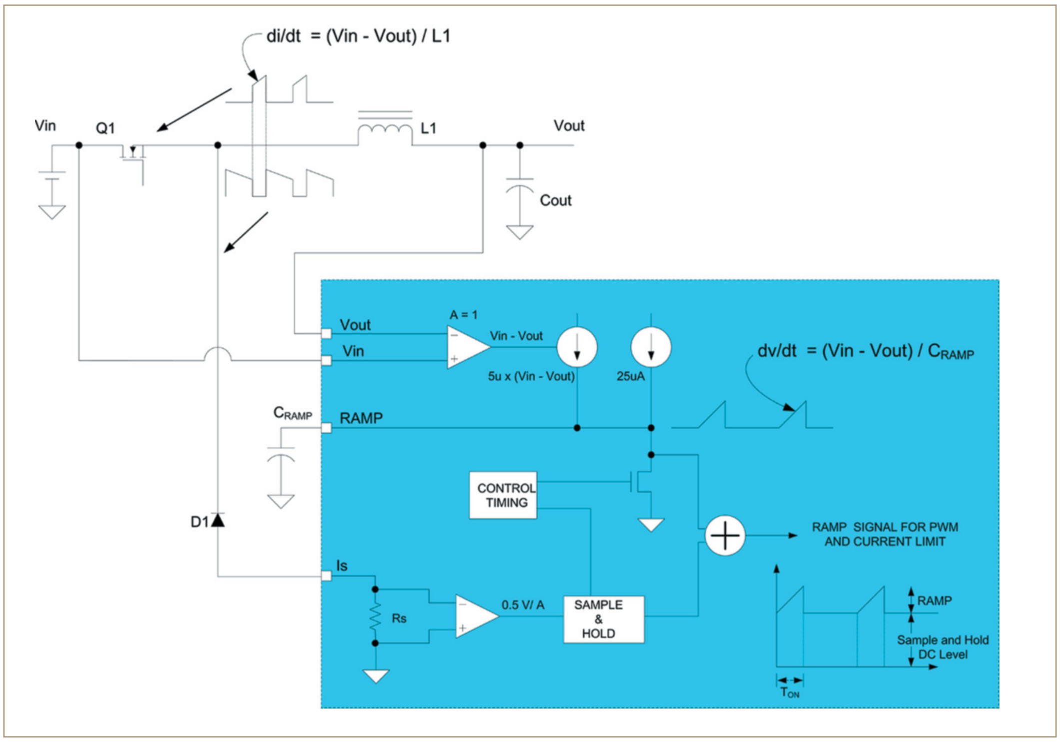

Figure 4: Emulated current mode control ramp generator, used in National's new Simple Switchers LM2557x and LM557x

achieving very small on-times necessary to regulate low output voltages from high input voltage rails.

Conclusion

National Semiconductor has enhanced the established family of Simple Switchers by adding a new generation of regulators with wide input voltage ranges from 6 to 75V. This new line uses emulated current mode architecture, which enables excellent transient response, ultra-short duty cycle and reduced noise sensitivity. An adjustable and synchroniseable switching frequency (up to 1MHz) and more general flexibility gives the designer the freedom required for tomorrow's power designs.