Power Cycling Induced Failure Mechanisms in High Temperature Applications

The specific cooling conditions of hybrid electric cars and the trend to higher current densities in power electronic applications demand the operation of semiconductors at junction temperatures above the common level of 125°C. **Thomas Licht, Thomas Schütze, Infineon Technologies AG, Warstein, Germany**

The maximum operation temperature is mainly limited by the reliability of the assembly and interconnection technology to reach the number of required temperature cycles during lifetime. Known weak points are bond wires and solder joints.

Power cycling test

Figure 1 demonstrates the run of dissipated power as well as upper and lower level T_{high} and T_{low} of the die temperature T_j by which a power cycling test can be described.

IGBT forward voltage drop V_{CE}, forward current I_C, virtual junction temperature T_j and heatsink temperature T_h are continuously monitored during the test. The thermal resistance R_{thjh} is calculated from these values. Since both V_{CE} as well

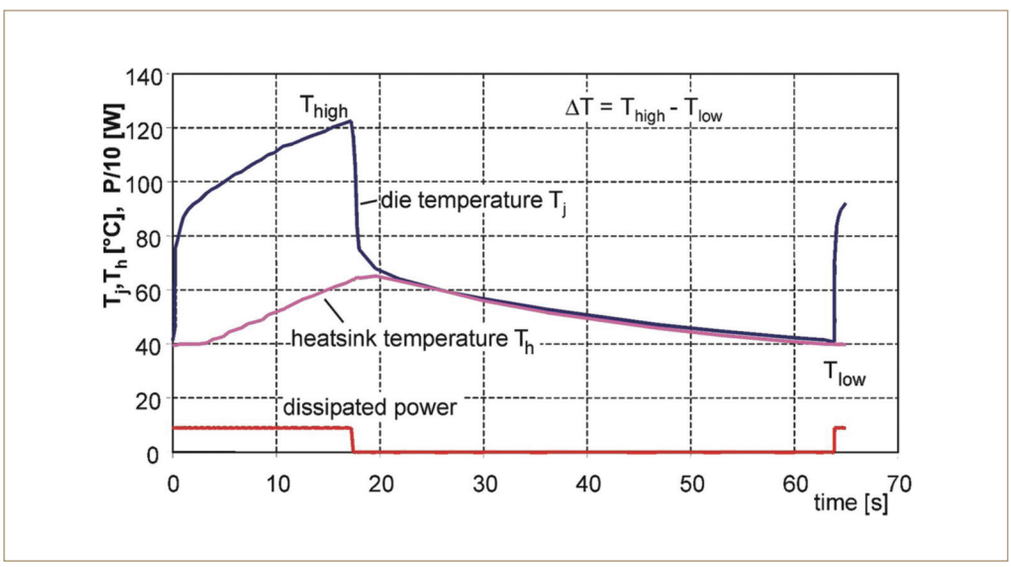

Figure 1: Characteristic variables of a power cycling test: dissipated power and resulting temperatures of junction and heatsink

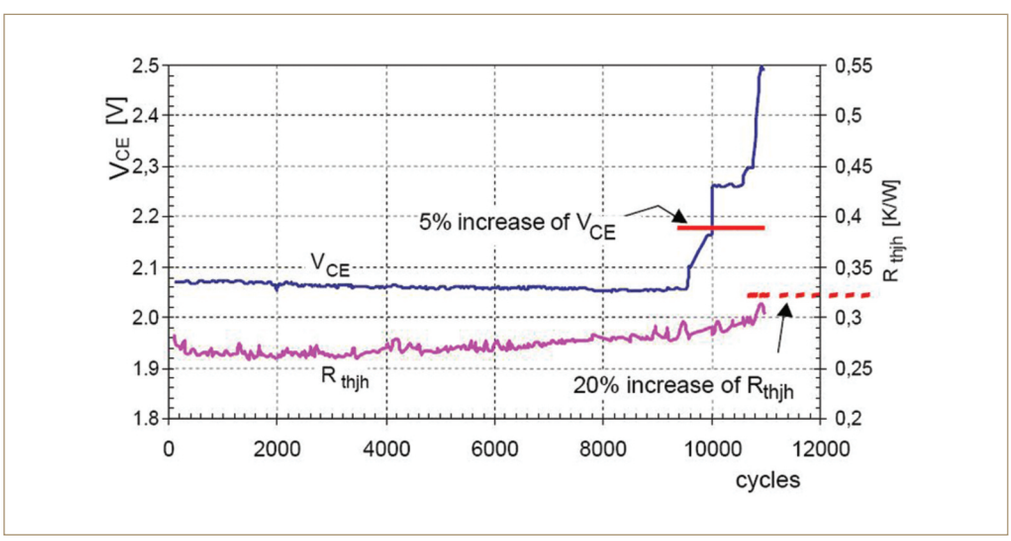

Figure 2: Recording V_{CE} and R_{thjh} in power cycling test with high $\varnothing T$ = 123K

Figure 3: **Bond lift-off as a result of power cycling**

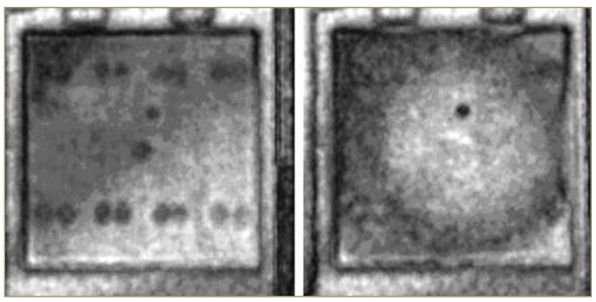

Figure 4: **Ultrasonic image of a lead-free unstressed (left) and stressed (right) chip solder layer**

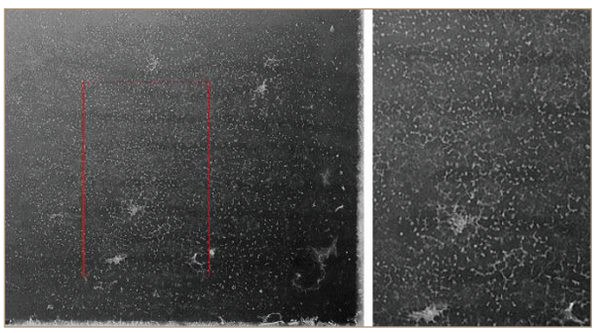

Figure 5: **Lead-rich soft solder with damage in centre and zoom of the damage (right)**

as R_{thjh} may increase during the test, one must distinguish both factors.Therefore either an increase of V_{CE} by 5% or an increase of R_{thjh} by 20% are defined as failure limits.

In Figure 2, the V_{CE} failure limit is reached after approximately 10,000 cycles. The sudden leaps in the V_{CE} curve indicate lift-off of single bond wires. After 6,000 cycles a slow increase of R_{thjh} can already be observed, a sign of solder fatigue. The failure limit of R_{thjh} would be reached after approximately 11,000 cycles. The progressive increase of R_{thjh} raises the temperature T_{high}, and thus enlarges the thermal stress for the bond wires at the same time. Also, solder fatigue is a significant failure mechanism in this test; it could even be the main failure mechanism.

Bond wires

For a long time bond wires were discussed to be the main weak point for power cycling. Figure 3 shows the typical failure mode, the lift-off of a bond wire. There is no adherence in the centre of the bond area.

The bond wire process could be improved significantly. From the viewpoint of high temperature applications, bond wires seem to be no longer the main weak point, if a proper technology is used. In [1] it was shown, that by the use of Low Temperature Joining Technique (LTJT) the power cycling capability could be raised even for cycles up to $\Delta T = 160K$.

Solder layers

By improved bond wire technology, limits of solder layers become more and more visible. Using large area silicon dies (>0.5cm²) the hottest spot is under the centre of the device. Figure 4 demonstrates that the degradation of lead-free solder layer starts in the centre of the device.

Degradation below the device centre is also found, if lead-rich solders are used. This becomes visible only in high-resolution X-ray images. The sample of Figure 5 reached the V_{CE} + 5% limit at 24,800 cycles. The test parameters have been t_{on} = 17s, T_{high} = 156°C, ΔT = 120K and the increase of R_{th} between junction and substrate has been 10%.

Degradation at the hottest point is also found for the solder layer between substrate and base plate. The example shown in Figure 6 was executed with an

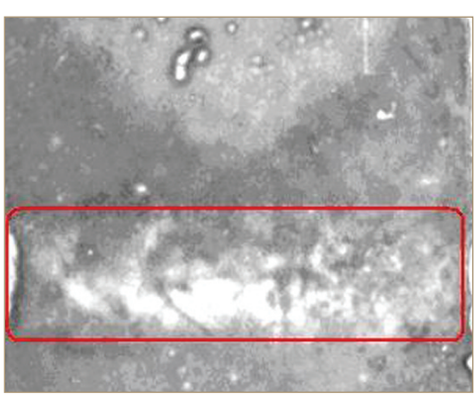

Figure 6: **Damage below active power cycled IGBTs in a lead-free substrate solder joint**

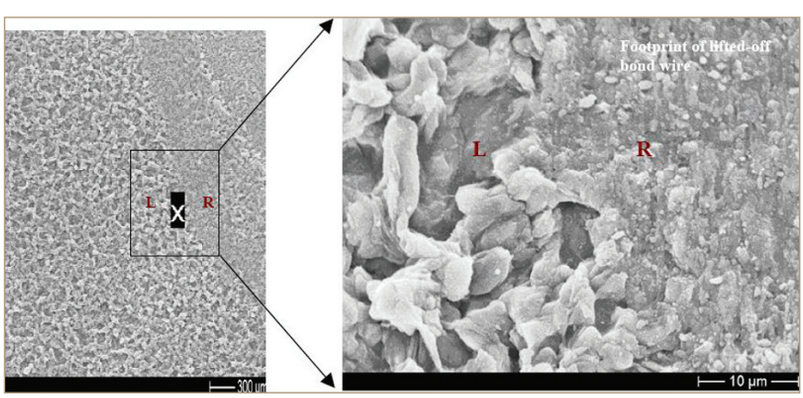

Figure 7: **Region adjacent to the footprint of a lifted-off bond**

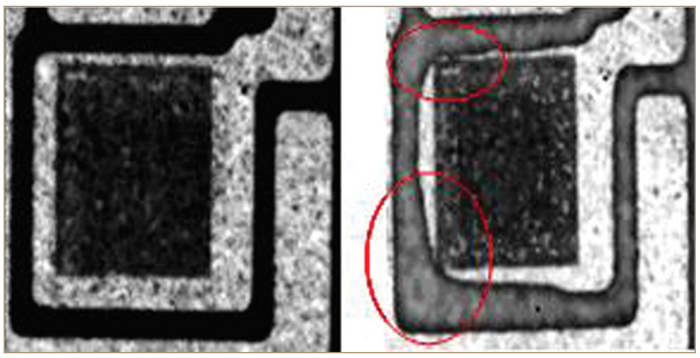

Figure 8: Comparison of unstressed (left) and stressed (right) DCB substrate

AlSiC base plate module at $\varnothing T$ = 70K, T_{high} =150°C, the number of cycles to V_{CE} +5% was 255,000.

It must be noted that these results contradict often used models which assume crack propagation starting at the edges of the devices. These models are valid for temperature cycling tests, in which the module is heated and cooled passively, and where a homogeneous temperature is given. In active power cycling, there are significant temperature gradients appearing between the different layers. On large dies with areas >1cm², temperature differences of up to 20K are possible between the hot centre and the edge of the silicon die.

Reconstruction of metallisation

Besides bond wire lift-off and solder degradation, thermo-mechanical stress can cause reconstruction of the metallisation. Although a resistivity increase of up to 41% for a metallisation with strong reconstruction was found, the effect on the forward voltage drop is rather low.

Figure 7 shows a detail of the metallisation adjacent to the footprint of a lifted-off bond. The device survived 44,500 cycles with $\varnothing T_j$ = 130K, T_{high} = 170°C. The high number of cycles was achieved by applying single-side LTJT technology. From this observation, we do not suppose reconstruction to be a mechanism which leads directly to bond-wire lift-off.

Nevertheless, the effect of reconstruction should be regarded in further investigations, because it may affect the current distribution and may be of negative influence to the surge current capability of free-wheeling diodes.

Substrate delamination

Under same conditions, $\varnothing T$ >130K, LTJ technology, limits of the Direct Copper Bonding (DCB) substrates were found. Figure 8 gives an example of failure analysis after 56,780 cycles.

The devices under test were baseplate-less modules without a substrate solder joint. Substrate delamination was found, which usually only occurs under passive temperature cycles. A possible improvement is e.g. the introduction of so- called dimples which help to reduce mechanical stress in the corners of the Cu pads.

Conclusion

With improved bond wire technology, limits of solder layers become more and more visible. Besides cracks propagating from the centre to the edge, solder fatigue starting from the centre of the devices is also found. In substrate solder joints, fatigue starting at the locations of the dies and therewith the hottest point of the solder interconnection was also found. Additionally, a strong reconstruction of the die metallisation layers occurs. The metallisation below the bond wire is less affected, but the resistivity of the metallisation is increasing significantly.

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Literature

[1] R. Amro, J. Lutz, J. Rudzki, R. Sittig, M. Thoben: 'Power Cycling at High Temperature Swings of Modules with Low Temperature Joining Technique', Proceedings of the ISPSD 2006, Naples, Italy