Improved Efficiency in Redundant Power Systems

Traditionally, redundant power systems have relied upon diodes to couple multiple power supplies onto a single rail. A more effective way to improve system efficiency is by eliminating the forward drops associated with semiconductor rectifiers, while still preventing even low levels of reverse current flow. This can be accomplished with an ORing controller such as the TPS2410. **Alan Hastings, Senior Design Engineer and TI Fellow, Texas Instruments, USA**

High-reliability systems often use multiple power sources to ensure continued operation despite the failure of a source. Schottky diodes placed in series with each supply ensure that a failed supply cannot load down the output bus. Unfortunately, Schottky diodes typically have forward voltage drops of 0.5 to 1.0V. These diodes dissipate significant power and, thus, compromise the efficiency of the entire system. Replacing the Schottky diodes with low-RDS(ON) MOSFET transistors greatly reduces forward voltage drops. The TPS2410 ORing controller contains all of the control and drive circuitry required to operate one external N-channel MOSFET transistor. It accommodates bus voltages of 3 to 16.5V, and down to 0.8V with an auxiliary supply connected to VDD. Figure 1 shows an application circuit in which two ORing controllers couple separate 12V sources, VIN1 and VIN2, onto a single output bus, VOUT.

MOS pass transistors M1 and M2 are oriented so that their body diodes block reverse conduction. Capacitors C1 and C3 act as energy storage capacitors for the charge pumps internal to the ORing controllers; C2, C4, and C5 are bypass capacitors. Resistors R1–R8 program various optional features supported by the controller, including under-voltage and over-voltage protection, and fast shutdown threshold. The TPS2410 also offers fault monitoring and deglitch filtering (not shown in Figure 1).

Inside the controller

The TPS2410 is a monolithic BiCMOS IC combining a control amplifier, a fast shutdown comparator, a charge pump, a gate driver, and all associated control circuitry (Figure 2).

Control amplifier A1 forms the heart of the controller. This amplifier attempts to regulate the voltage across the external pass transistor to 10mV. If the voltage exceeds 10mV, then the amplifier increases gate drive to reduce its forward drop. If the voltage falls below 10mV, then the amplifier throttles back the gate drive to force the transistor back to the regulation point. The control amplifier turns the pass transistor off whenever the smallest reverse current attempts to flow.

Fast shutdown comparator C1 protects the system against supply shorts. The control amplifier only sinks 5mA, so it cannot pull off the pass transistor quickly enough when a bus is shorted. Instead, comparator C1 senses the voltage drop generated by the reverse current and trips a gate driver, if it exceeds a user-specified threshold. This driver pulls roughly 2A for 12µs and then folds back to 20mA to hold off the pass transistor. Shutdown typically requires less than 150ns. Amplifier A2 allows the user to set the fast shutdown threshold using a resistor connected from RSET to ground.

Comparators C2 and C3 implement fault detection. Comparator C2 reports a fault if the control amplifier cannot enhance the pass transistor sufficiently to reduce its series drop to less than 0.4V, indicating an open-circuit failure. Comparator C3 reports a fault if the amplifier cannot enhance the pass transistor's gate by more than 0.75V, indicating a gate short failure. If either of

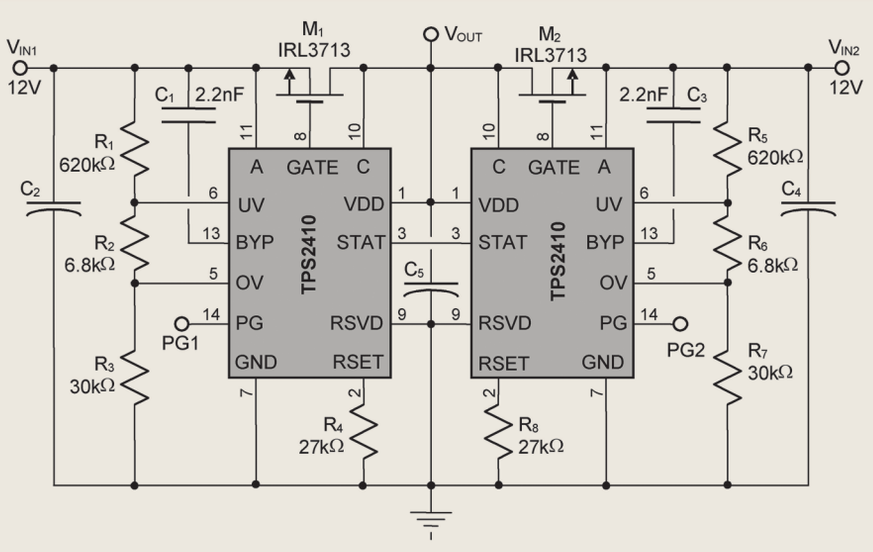

Figure 1: Typical application circuit using the TPS2410 ORing controller (pull up resistors for open-drain outputs PG1 and PG2 are not shown)

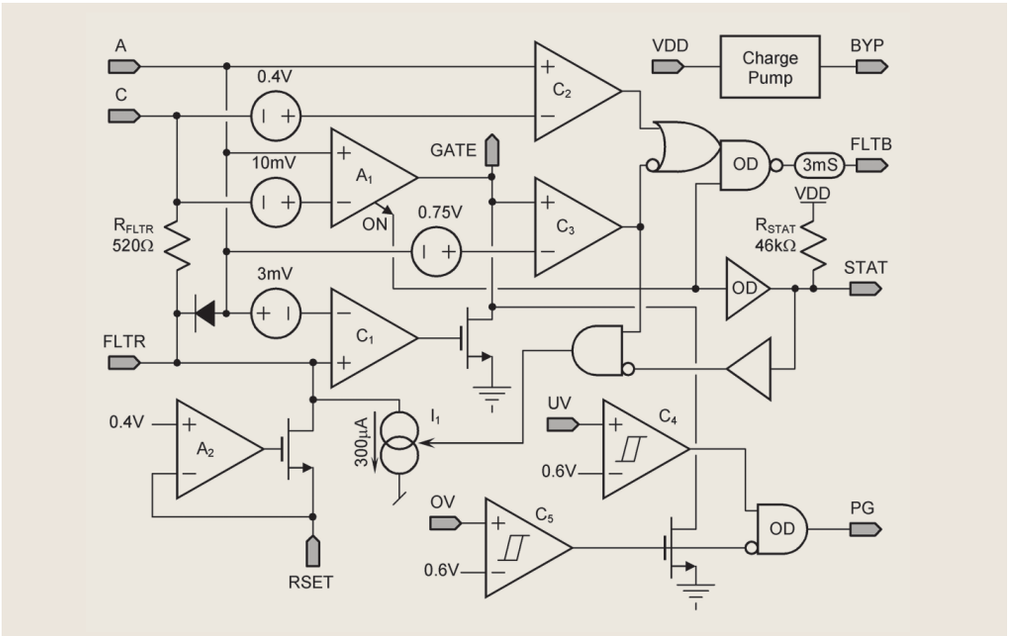

Figure 2: Simplified block diagram of the TPS2410 ORing controller (gates marked OD have open-drain outputs)

these fault conditions remains for more than 3ms, an open-drain output driver pulls FLTB low.

Comparators C4 and C5 implement under-voltage and over-voltage detection. Comparator C4 reports an under-voltage condition, if less than 0.6V appears at the UV pin. Comparator C5 reports an overvoltage condition and turns off the pass transistor, if more than 0.6V appears at the OV pin. Whenever either condition occurs, the open-drain output driver pulls the PG pin low. The user can monitor an input supply, the output rail, or any other desired node voltage. Alternatively, the OV pin can serve as an enable input.

The STAT pin reports the status of the external pass transistor. An open-drain output driver pulls STAT low when the pass transistor is off, and an internal resistor pulls STAT to V_{DD} whenever the transistor is on. In Figure 1, the circuit of the STAT pins of the two controllers are wired together to generate a signal that goes low whenever either pass device is disabled. This wired-OR configuration enables current source I1 to desensitise the fast shutdown comparator by 160mV, whenever the other controller disables its pass transistor. This feature helps prevent transient disturbances from disabling all power sources feeding the output bus. Leaving the STAT pins of the controllers unconnected disables this feature.

The FLTR pin provides an alternative means of desensitising the fast shutdown comparator to transient disturbances. An external capacitor connected from A to FLTR, in conjunction with internal resistor RFLTR, forms a low-pass filter. The larger the capacitor the slower is the comparator's response – and the greater the noise immunity.

Design procedure

The first step in designing an application circuit around the TPS2410 is to select a suitable pass transistor. It should withstand 150% of the rated supply voltage, carry the full-rated supply current, and not dissipate

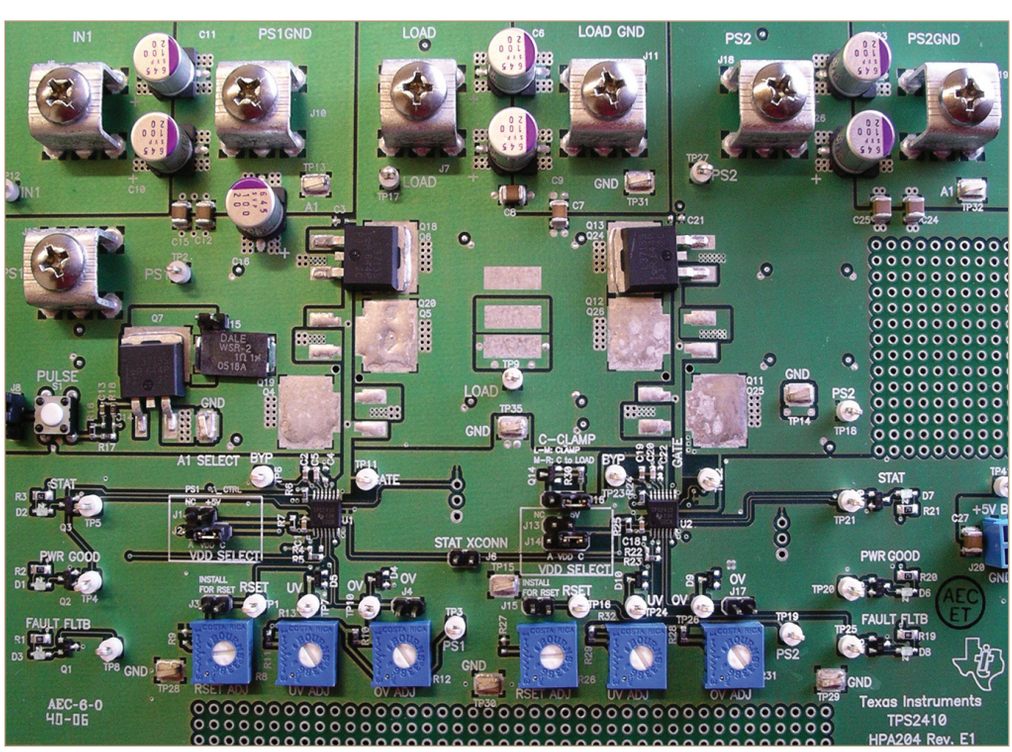

Figure 3: TPS2410 evaluation module HPA204)

excessive power at V_{GS} = 10V. The transistor's threshold voltage should equal at least 1V. The IRL3713 meets these conditions for many 12V applications.

Next, the designer must select the fast shutdown threshold V_{OFF}. Omitting the RSET resistor sets the threshold at a forward bias (from A to C) of 3mV. Inserting the resistor shifts the threshold downwards to a value according to equation 1.

$$V_{off} = 3mV - \frac{520\Omega}{R_{SET}}(400mV) \quad (1)$$

Applications that cannot tolerate reverse current flow use the default threshold. The circuit shown in Figure 1 uses a slightly negative threshold to minimise the chance of transient disruptions, triggering the fast threshold comparator. The 27kΩ resistors generate a threshold of about –5mV.

The internal charge pump requires an output storage capacitor, usually consisting of a 2200pF ceramic capacitor connected from BYP to the input rail. Input and output bypass capacitors, each typically 1nF, provide a return path around the internal charge pump. Minimise the area of the loop from BYP to V_{DD} through the storage capacitor (C1), input bypass capacitor (C2), and output bypass capacitor (C5). These bypass capacitors also help absorb system-level ESD transients.

Although the circuit of Figure 1 does not show a filter capacitor connected from A to FLTR, most applications will benefit from the installation of a 100pF capacitor in this position to provide additional protection against transient disturbances on the buses. Designers should allocate a place for this capacitor, begin testing with it in place, and then determine whether or not it can be removed.

The built-in control amplifier imposes certain stability criteria on the system. The gate capacitance C_{iss} of the pass transistor should exceed 1nF. The output rail should have at least 100µF of low ESR bulk capacitance to swamp the impedance of downstream wiring and input filters. The load should also draw a continuous current of at least a few milliamps to bias the pass transistor into conduction. If stability proves problematic, consider replacing the TPS2410 with the TPS2411. The control amplifier of a TPS2410 eliminates continuous reverse currents that can become very large in high-power applications using low $R_{DS(ON)}$ MOSFETs. The TPS2411 uses a comparator to turn the pass transistor on under forward bias and off under reverse bias, an especially useful arrangement for systems that experience large transient steps from light loads.

Finally, the designer should decide whether to employ any of the optional features built into the TPS2410. The circuit of Figure 1 uses the power good circuitry in each controller to monitor the associated power supply. Three resistors configure the undervoltage and overvoltage trip points. For example, to size resistors R1, R2, and R3 in Figure 1 follow equations 2 and 3.

$$V_{UV} = \frac{R_1 + R_2 + R_3}{R_2 + R_3}(0.6V) \quad (2)$$

$$V_{OV} = \frac{R_1 + R_2 + R_3}{R_3}(0.6V) \quad (3)$$

The resistor values used in the circuit of Figure 1 yield an undervoltage threshold V_{UV} = 10.7V and an overvoltage threshold V_{OV} = 13.1V.

Conclusion

The TPS2410 ORing controller presents an opportunity to enhance system efficiency by eliminating the forward voltage drops associated with semiconductor rectifiers. For those who wish to examine the TPS2410 further, an evaluation module (see Figure 3) can be ordered online. Related devices include the TPS2411 which features on/off gate control, and the TPS2412 and TPS2413 which omit certain optional functions to fit in 8-pin TSSOP packages.