High-Frequency Power Inductor Packaging

Placing a high-frequency power inductor inside a semiconductor package has its challenges. Encapsulating the inductor in mould compound causes stress that alters its electrical properties, particularly during thermal cycling. The article explores all the key issues encountered when co-packaging an inductor with a switching regulator, and introduces the culmination of this technology, the MEMs inductor, fabricated in an extension to standard semiconductor processing. **Matt Wilkowski and Paul Greenland, Empirion, Santa Clara, USA**

The trend in power electronics is to reduce the size of the power delivery circuits, as well as to improve the transient response to load changes, to support electronic circuit loads operating at high frequencies. The design of discrete inductor for traditional DC/DC converter (Figure 1) applications typically requires a trade-off of three electrical performance criteria within an allowable component footprint and component profile requirements. These three criteria are inductance value, energy storage requirement (peak current capability) and allowable contribution to the overall power efficiency budget.

The designer of a DC/DC converter traditionally accommodates design criteria such as thermal and EMI performance, as well as compatibility with semiconductor manufacturing and packaging requirements, after the suitable inductor design is identified. The size of the inductor must shrink to the approximate size for both footprint and profile of the CMOS die to which it will be coupled within a package assembly, in order to be compatible with semiconductor manufacturing and packaging processes (Figure 2). This is true whether the package layout strategy is to treat the CMOS die and the inductor as side-by-side die, stacked die or as a single integrated die.

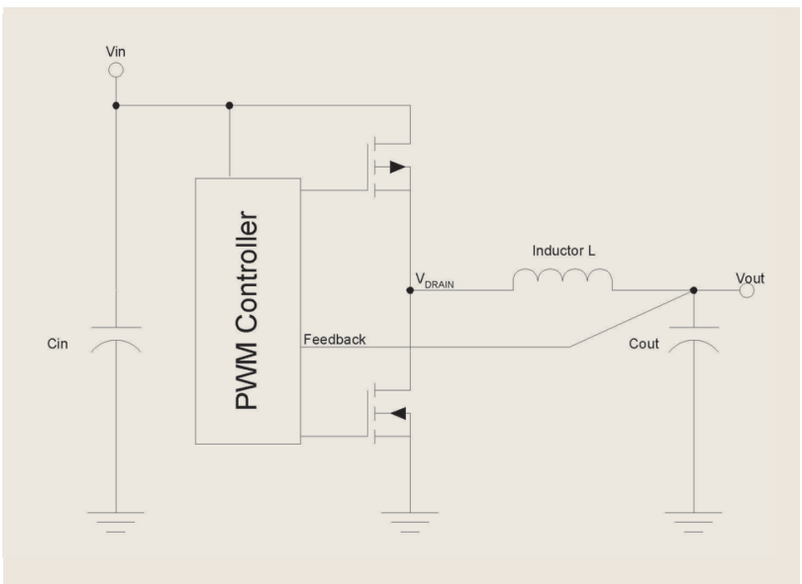


Figure 1: Simplified synchronous DC/DC buck converter

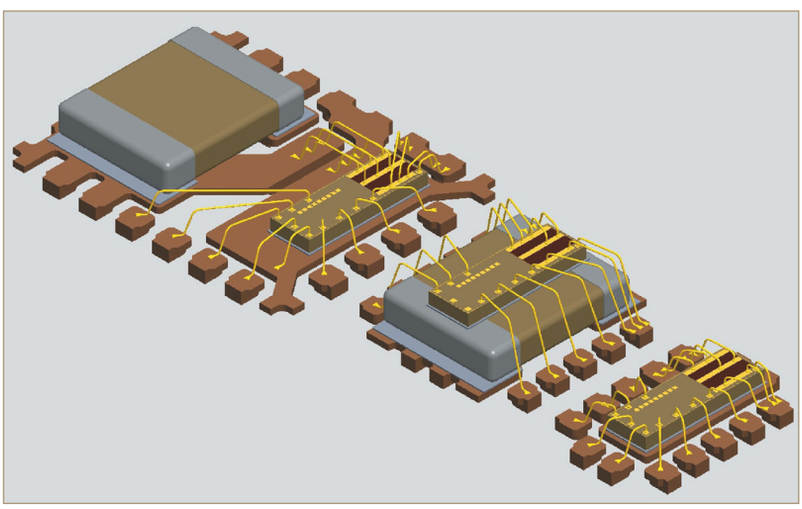


Figure 2: Three possible options for package layout strategy

Inductors and losses

Since the energy storage capability (1/2 LI^2_{PEAK}) of an inductor is proportional to its volume for a given magnetic material, there will significant impact on the other two traditional primary design criteria, inductance value and overall power loss, if the volume of the inductor is expected to decrease between three to four orders of magnitude. The increase of switching frequency can only reduce the required value of inductance for a given value of peak to peak current for a given range of input and output voltages and a switching topology. The relationship between the required inductance value and peak to peak ripple current and the operating conditions of DC/DC synchronous buck converter are given in equation 1.

$$L = \frac{V_{OUT} - \frac{V_{OUT}^{\ 2}}{V_{IN}}}{F_{SWITCH} * \Delta I_{PEAK-PEAK}} \quad (1)$$

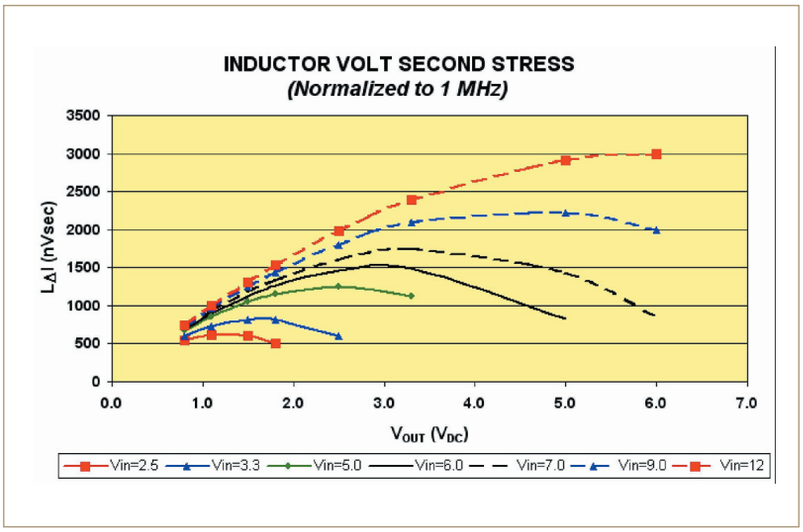


Figure 3: Volt - second stress on output inductor at 1MHz

A graphical relationship between the product of peak-to-peak ripple current and inductance and a synchronous buck DC/DC converter's input and output voltage with a normalised frequency of 1MHz is illustrated in Figure 3.

The peak current I_{PEAK} in an inductor is related to the DC value of current and the peak-to-peak ripple current by the relationship indicated in equation 2.

$$I_{PEAK} = I_{DC} + \frac{\Delta I_{PEAK-PEAK}}{2} \quad (2)$$

Increasing the switching frequency of a DC/DC converter to reduce the value of inductance for a given value of peak-to-peak ripple current will maintain the same value of peak current in the inductor. Increasing the switching frequency will only decrease the amount of energy storage, inversely proportional to the increase of the switching frequency, if the same peak to peak current ripple requirements are maintained at the higher switching frequency as the lower switching frequency. Clinging to traditional peak-to-peak ripple current criteria will only decrease the required volume of a magnetic component by one order of magnitude if the frequency is increased by one order of magnitude, with all other design parameters such as peak-to-peak ripple current, magnetic material, etc, being the same.

Further decrease in component inductor size must come from additional circuit requirement choices, as well as magnetic material choices. The most obvious circuit requirement choices are allowable ripple current, as well as allowable efficiency budget for the inductor. Increasing the allowable ripple current from 20% of full load current to 75% of full load current is consistent with lower inductance values required for improved transient response. However, the decreased value of inductance and increased magnitude of ripple current does require some design consideration for the effect of higher switching currents on the power losses of components that must conduct the higher currents, as well as use of capacitors with lower equivalent series inductance (ESL) values to maintain ripple voltage requirements. An approximate equation for the output ripple voltage, as it is related to the equivalent series resistance (ESR) and equivalent series inductance (ESL) of the output capacitors, is indicated in equation 3.

$$\Delta V_{RIPPLE} \approx (V_{IN} - V_{OUT}) * \left[\frac{\frac{V_{OUT}}{V_{IN}}}{L_{OUT} * F_{SWITCH}} * ESR + \frac{ESL}{L_{OUT}} \right] \quad (3)$$

Suitable magnetic materials

The most common magnetic materials used for output inductors at switching frequencies above 100 kHz are NiZn ferrite, MnZn ferrite, powdered iron, sendust or thin metal films. Magnetic cores composed of ferrite materials tend to have lower AC power losses at the expense of lower saturation flux densities and a sharp saturation characteristic. Magnetic cores composed of powdered iron and sendust materials have higher saturation flux densities, thus allowing for higher energy storage. These materials tend to have higher AC power losses and a soft saturation characteristic. NiFe metal and FeCo metal films have higher saturation flux density, a sharp saturation characteristic, and can exhibit lower ac power loss if the film thickness is appropriately thin relative to the operating frequency.

The peak flux density (B_{PEAK}) in a magnetic core is related to the inductance (L), peak current (I_{PEAK}), coil turns (N) and magnetic cross section area at the core at its minimum cross section area point (A_{MIN}) as indicated in equation 4.

$$B_{PEAK} = \frac{LI_{PEAK}}{NA_{MIN}} \quad (4)$$

The inductor energy storage equation and equation 4 can be combined to indicate that energy storage capability is directly proportional to the achievable peak flux density in the magnetic core as indicated in equation 5.

$$E \propto \frac{BNA_{MIN}}{2} \quad (5)$$

Thus, in order to reduce the volume of inductor, the inductor must be operated a close as possible to its saturation flux density at the intended operating temperature, or a magnetic material with a high saturation flux density must be used.

One consequence of reducing the inductance value and allowing the peak to peak ripple current to approach 75% of the maximum intended load current, and to operate the magnetic core as close as possible to its saturation flux density as design margin allows, is that dynamic flux density swing in the magnetic core will become very large. The AC power loss in a magnetic core is given by equation 6.

$$P_{AC} = K * \left(\frac{\Delta B}{2} \right)^a * f^b * V_e \quad (6)$$

The typical value of a in equation 6 is in the range 1.7 through 2.3, and the typical value of f is in the range 0.9 to 1.3. Increasing the value of the flux density swing in magnetic core by a factor of greater than 10 increases the power loss density by a factor of 100. The volume of the magnetic core is not decreasing at as

great as a factor so, in order to maintain low AC power losses, magnetic materials with inherently low AC power losses must be used. Operating at high dynamic flux density swings and frequencies above 1MHz would tend to eliminate powdered iron and sendust materials, since they would become power loss prohibitive if utilised to their full saturation flux densities. Thin metal films are preferred to ferrite materials if the appropriate number of thin layers can be economically fabricated. The trade-off for the use of metal films becomes the use of the most appropriate individual layer thickness from an AC power loss standpoint, and the number of thin layers required to meet saturation criteria, while maintaining economic feasibility.

The discrete inductors used in non-integrated DC/DC converter solutions typically consume less than 2 power efficiency points or less than 10% of the overall power loss of the circuit. Decreasing the size of the size of the inductor by several orders of magnitude will inevitably increase the consumption of power efficiency of the inductor, as well as its share of the overall power loss of the circuit. Volt-ampere circuits are typically used to characterise the AC power loss of inductor as a function of volt-second stress and frequency. The collection of data over multiple frequencies and levels of volt-second stress can typically be curve fit to an equation such as equation 7, which indicates AC power loss as a function of the input voltage, output voltage, and operating frequency of a synchronous buck DC/DC converter.

$$P_{AC} = K * \left((V_{IN} - V_{OUT}) * \frac{V_{OUT}}{V_{IN}} \right)^{a} * F_{SWITCH}^{b-a} \quad (7)$$

The typical value of a in equation 7 is in the range 1.7 - 2.3 and the typical value of f is in the range 0.9 - 1.3.

Curve fitting empirical AC power loss data to the form of equation 7 does not require the user to know the specifics of the magnetic core or the coil construction geometry. It simply provides an AC power loss based on empirical volt-second stress conditions applied to the inductor at specific operating frequencies. However, the designer can always analyse and optimise the specific components of the AC power loss on an individual basis, in an effort to meet specific power loss requirements.

As inductor devices are required to shrink to fit into semiconductor packages and processes, the amount of volume consumed by air, the spacing between conductors and the thickness of insulation all decrease. The decreasing values of these parameters will result in higher shunt capacitance for the inductor. The smaller value of interface area of the inductor's internal conductors counteracts these decreases to some extent, to keep the shunt capacitance in check to some extent.

The value of an inductor's shunt capacitance is typically derived from the measurement value of the series inductance at a low frequency and the measurement value of the self-resonant frequency using equation 8.

$$C_P = \frac{1}{4 * \pi^2 f_O^2 L_S} \quad (8)$$

The self- resonant frequency is typically taken as the frequency at which the phase angle of the impedance of the inductor passes through zero. A graphical representation of phase angle as a function of frequency for a typical 1100nH inductor used in a DC/DC buck converter delivering less than 1ADC is illustrated in Figure 4.

Inductors with shunt capacitance values below 10pF should still have a self-resonant frequency high enough to allow the low pass output filter section of a DC/DC converter to continue to operate as a low pass filter and suppress higher order harmonic signals of a converter switching between 1 and 10MHz. A transition of a LC low pass filter to band pass filter and ultimately to a high pass filter, as seen by the harmonic frequencies above the respective self resonant frequency of the capacitor and the inductor, occurs at higher frequencies.

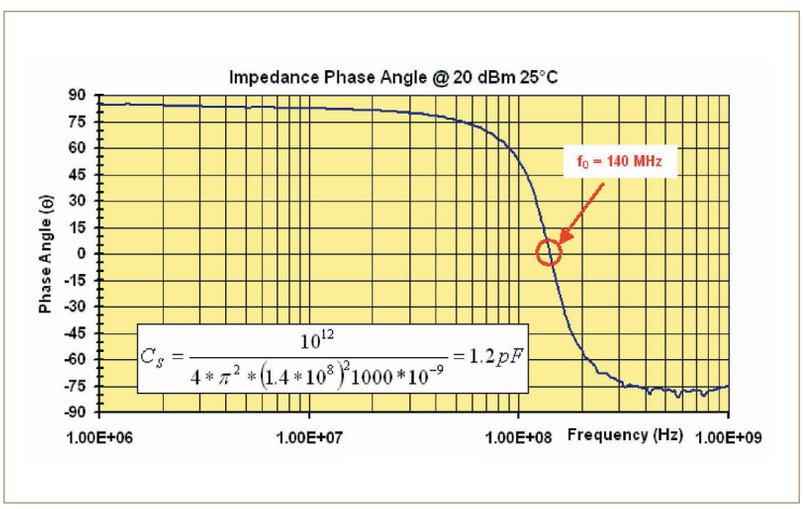
Packaging process constraints for integrated inductors

The required physical profile of a semiconductor package is typically less than 1.2mm, if the package contents are limited to the die and its wire bonds. The physical profile of passive components used in module type packages can drive package profile upwards to 2 or 3mm. In addition to requiring a thickness of moulding compound greater than necessary over the lower profile components in the package compound, the use of a greater thickness of moulding compound places greater physical stress on the components and interconnections within the package.

The performance characteristics of inductance permeability and AC power loss of most magnetic materials are negatively affected by physical stress. The negative affects of the physical stress can be addressed in several ways. The methods to address physical stress include protection of the sensitive magnetic material from transgressing thickness of moulding material; utilisation of magnetic core structures that are less vulnerable to stress induced by the moulding compound; utilisation of magnetic core structures that are less sensitive to decreases in inductance permeability and increases in core loss; and utilisation of design margins in the inductor design based on empirical characterisations of the effects of stress in specific moulding configurations.

Inductors that are less sensitive to the stress of moulding compound typically utilise magnetic cores that have a significant physical air gap or a distributed air gap. Magnetic cores that have a distributed air gap may be self-shielding, whereas magnetic cores with a significant physical air gap will exhibit more fringing of magnetic fields of the air gap. If the latter is

Figure 4: Phase angle as a function of frequency for a 1100nH inductor suitable for use in a DC/DC converter delivering 1ADC switching between 1 and 10MHz



chosen, the sensitivity of surrounding components both internal to and external to the semiconductor package to the magnitude and orientation of the fringing magnetic fields must addressed by layout.

For a side-by-side and stacked die packaging strategies, chip inductors, bead inductors, low profile vertical drum core inductors or windings embedded in a magnetic media with suitable electrical performance characteristics can be considered. However, these types of inductors present challenges to surface mount solder processes, as well as wire bonding processes.

For the side-by-side construction strategy the required interconnect between the CMOS die and the inductor, as well as between the output inductor and the output terminals of the device, can be either though solder connections, wire bonds, conductor paths through the trace of a PWB type substrate, or through the metal of a lead frame or a some combination of these interconnect schemes. For a stacked construction strategy, the interconnection between the CMOS power devices and the output inductor is typically limited to a solder joint or to wire bonds, whereas the interconnect between the output inductor and the output terminals can be any of the previously mentioned interconnect schemes. For an integrated power device inductor the interconnection is typically achieved by the conductive via between the power device and the inductor, as part of the wafer fabrication.

In devices designed to deliver less than 1ADC, the combined DC resistance of 35 microns copper PWB traces and a limited number of parallel 25 micron diameter wire bonds between the die and the inductor could easily approach tens of milliohms, which would be less than 15% of the R_{DSON} value for the CMOS power devices, and less than 30% of the value of DC resistance for the inductor required to achieve respectable efficiency values.

In order to maintain to maintain insignificant values relative to the R_{DSON} of the power device and the output inductor for the wire bond and circuit trace interconnects, the combined resistance is restricted to several milliohms for modules required to deliver currents greater than 6ADC. This requires thicker and wider circuit traces, as well as a larger number of parallel wire bonds. For solder connections, a trade-off of trace width must be made relative to the volume of solder required to maintain MSL integrity. The conductor thickness of typical lead-frames is in the range of 150 to 200 microns is more suitable than the 25 micron conductor thickness of PWB substrates. A trade-off of wire bond diameter and the number of wire bonds is required, to limit the size of the metalisation pad required to accept the wire bonds on both the CMOS die and the inductor, while maintaining a reasonable value of DC resistance for the interconnection.

Conclusion

Placing an inductor inside the package with a switching regulator is a complex process with many trade-offs. The switching frequency should be chosen to permit miniaturisation, and the core material and winding format have to exhibit low loss and reduced parasitics at that frequency. Furthermore, the encapsulation process may change the electrical properties of the inductor, particularly if the core has a discrete gap. Depending on the packaging strategy, different bonding and interconnect options are available; each has its pros and cons. The ultimate aim of this process is to manufacture a chip-scale co-packaged inductor in the wafer fabrication plant.

UK Sales Partner for World's Smallest Silicon-Based Power Systems

UR Group has been appointed by Empirion as its UK sales partner. Empirion produces the world's smallest Power System on Silicon (PSoS) – the first and only all-silicon, switch-mode DC/DC converter with an integrated inductor that incorporates a PWM controller, power FETs, and compensation circuitry in an IC package.

"Empirion's technology represents the first major innovation in integrated power technology for over a decade. With the need to pack more and more functionality into ever shrinking space, chip-level integration frees up vast amounts of precious real estate. Empirion solves a multitude of power design problems. The technology is stunning and the benefits are enormous", comments Joe Matano, Managing Director of UR Group. "Applications include a wide range of high-volume consumer products such as mobile phones, portable game players, set-top boxes, MP3 and personal media players, PDAs, notebooks and PCs. Business and industrial applications include servers, point-of-sale equipment, telecoms and data communications systems, medical equipment and military and aerospace systems".

The layout and placement of the inductor is one of the most common reasons for power IC-related failures. According to UR Empirion products not only solve this problem, but also reduce board footprint by up to 70% and component count by up to 60%, as well as reducing noise and ripple associated with switch-mode power conversion. At the same time, they achieve up to 92% peak efficiency, deliver best-in-class transient response and enable a ten-fold switching-frequency improvement over solutions that were, until now, considered state of the art – output supply voltage can be scaled in a blistering 10 microseconds. In terms of output current, the product line currently ranges from 500mA to 9A and is continuing to expand.

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