Advantages of NPC Inverter Topologies with Power Modules

Efficiency is becoming increasingly important in power electronics. Many applications are driven by the initiatives for reduced energy consumption. The technology leaders are inverter applications in the solar market, but uninterruptible power supplies and motor drives also have new targets for improved efficiency. This article shows alternatives for 3~ inverters with 700V DC-link voltage. **Michael Frisch and Temesi Ernö, Vincotech Germany and Hungary**

The sinusoidal output current and voltage is the same for NPC (neutral point clamped) and half-bridge topologies. The difference is the way to generate the signal.

An inverter with 700V DC-voltage (+/-350V) generates a three-phase output signal with 400VAC phase to phase. The standard configuration with three half-bridges will switch the voltage from 350 to -350V. For this operation 1200V components are needed. The disadvantages in this case are the following:

- The switching losses are the product of the total 700V and the output current.
- 1200V components are slower than 600V components.
- The output voltage ripple is higher.

Operation modes of NPC

The NPC inverter with three NPC-bridges will switch either 350 to 0V (positive half- wave) or -300 to 0V (negative half-wave). Here, only 600V components are needed. This generates the following advantages:

- The dynamic losses are significantly reduced, only 350V are switched.
- 600V components are faster and there are many ultrafast components available.
- The output ripple is reduced.

T3 is switched on during the positive half-wave of the output signal. T4 is switched on during the negative half-wave. The PWM is modulated with T1 and T2 (see Figure 1). When T1 is switched off during the positive half-wave, the current will commutate from the neutral point through D1 to the output. The negative path is completely inactive. At the negative half-wave, we have the same procedure with negative current, but here T1 and T3 are inactive.

The NPC topology offers advantages such as reduced switching losses, smaller output current ripple, and total +/- supply voltage is split. Only half of the voltage has to be switched, and this also cuts the switching losses in the transistor by half. In the shown NPC topology, we are able to use 600V components instead of 1200V types. On top of that, in 600V technology much faster components are available than in 1200V. This will lead to further reduction of the switching losses. The NPC topology will have lower ripple in the output current and half of the output voltage transient. This will reduce the effort for filtering and isolation in the filter inductor. The DC voltage is divided into a positive and

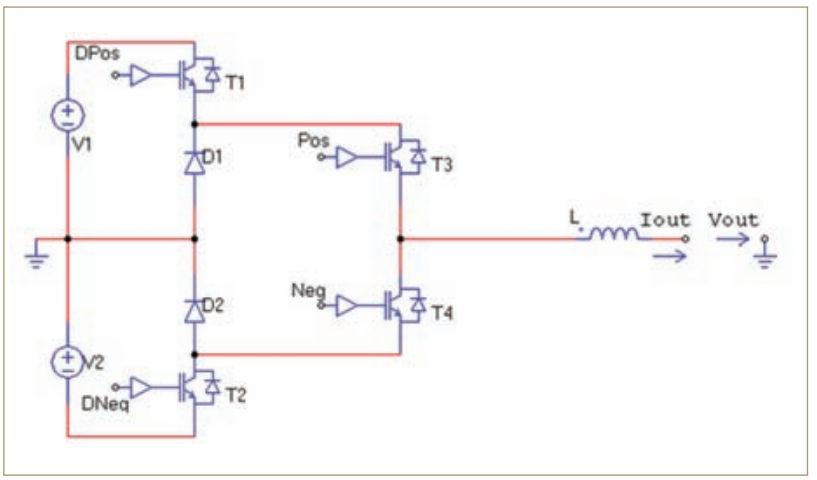


Figure 1: **Gate signal of a three-level inverter at real power**

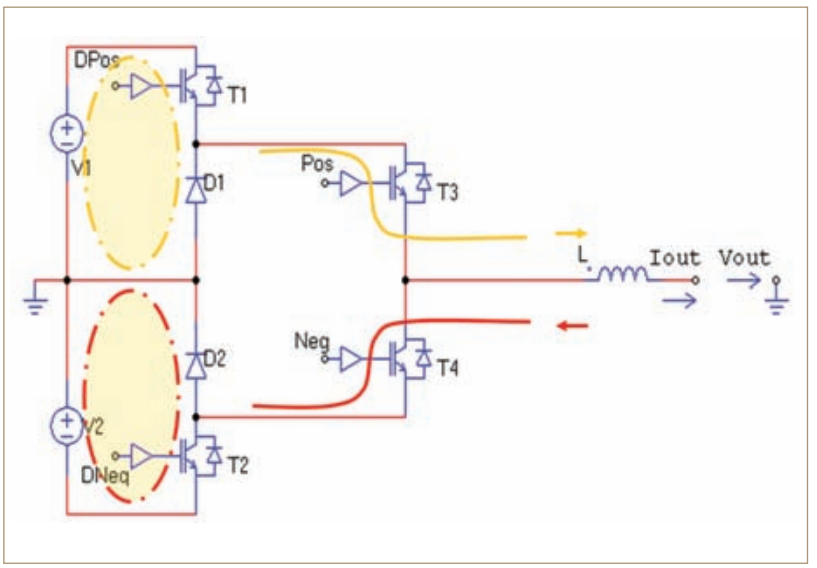


Figure 2: **Current and commutation loops at real power**

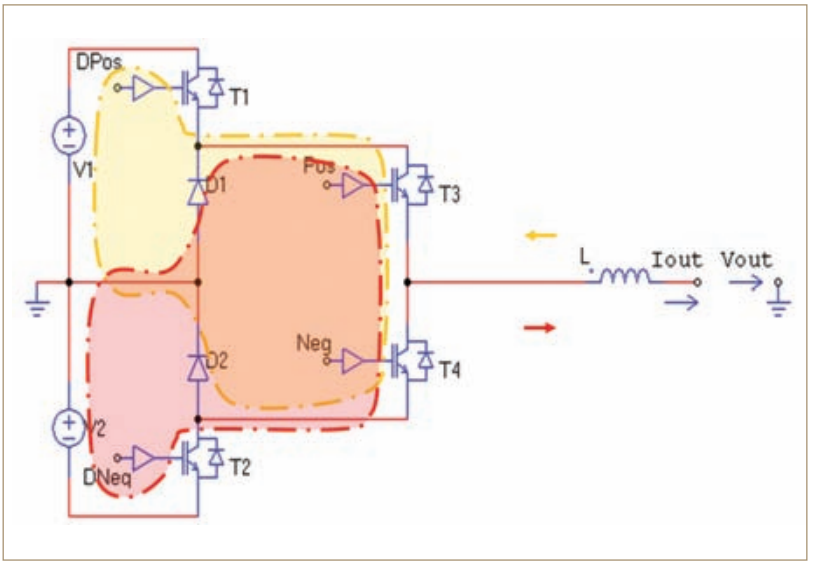


Figure 3: **Current and commutation loops at reactive power**

negative voltage, which supports the serial connection of DC capacitors without the need for leakage current compensation.

These advantages have to face the drawback of a higher complexity. More components have to be handled (10 instead of four) and the NPC topology requires four independent gate drives instead of two in the standard half-bridge topology.

Challenges for NPC power modules

The NPC topology is distinguished with a higher complexity, which makes the circuit more sensitive for parasitic effects. To avoid such disadvantages, the power module has to be designed more carefully.

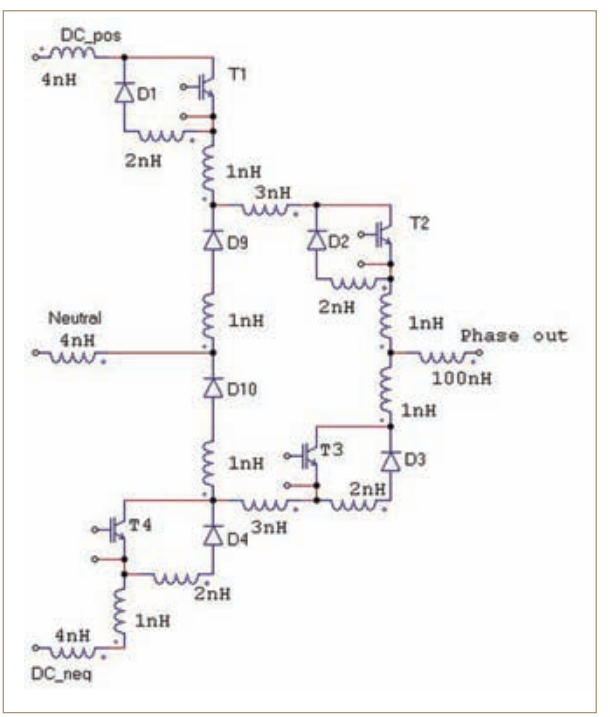
The low inductance between DC+ and DC- in half-bridge topologies is decisive. For the NPC topology the same is valid. Additionally, a low inductance between both DC voltages and the neutral point (NP) is important. This task is hindered by the fact that more components are included.

The inductance of power module based circuits is mainly influenced by the wire bonds of the semiconductors and the external interconnection. The inductive loops inside the power module are largely canceled by the eddy current induced into the backside metallisation of the module. The current and commutation loops in real power mode are shown in Figure 2, and at reactive power in Figure 3.

The parasitic wiring inductance will increase the switch-off losses of the transistors. Therefore, the target is to minimise the inductance between DC+, DC- and NP. In Figure 4, the parasitic inductances of a NPC power module are shown.

The pinout of the module is the key for a reduction of the parasitic inductances outside of the module. In Figure 5, a pinout of a low inductive NPC module is shown. Here, the NP can be built on both sides; on one side a low inductive pair with DC+, and on the other side with DC-.

Figure 4: **Parasitic inductances of a 1200V/300A NPC module**



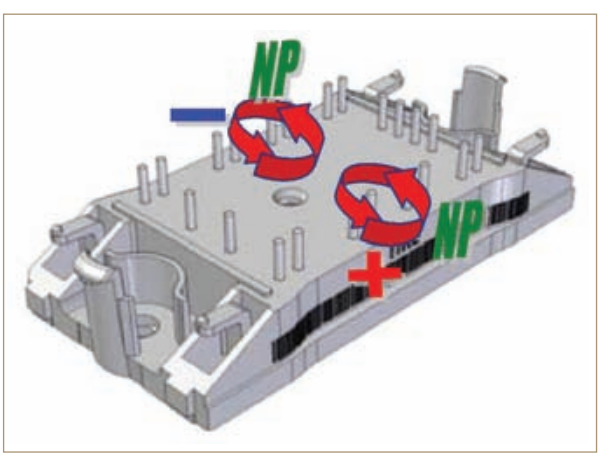


Figure 5: **Pinout of a low inductive 1200V-75A NPC module**

Benchmark of different topologies

In the following, we made a benchmark of different topologies. Here, the standard half-bridge (Figure 6) is compared with the previously discussed NPC topology (Figure 7) and with a mixed voltage three-level topology (Figure 8).

The conditions of the comparison are

- 4.6kW static load (25A) per phase
- 700V DC voltage (2*350V for three-level)
- output frequency 50Hz
- modulation frequency = 16kHz
- hard switching environment
- sinusoidal output voltage waveform (230VAC)
- $\cos\varphi = 0.8$
- 17.2kVA three-phase power.

The effort or chip area is given as the

product of voltage rating and nominal current of the power semiconductor, which is in line with the cost of the semiconductors.

The standard configuration for a three-phase inverter is three half-bridges. The components are 2nd generation of 1200V trench field-stop IGBTs with the corresponding free-wheeling diodes. The result is:

Conduction losses	36W
Switching losses	118W
Total losses	154W
Efficiency	96.65%
Total rating of Si	540kVA.

The NPC topology is the next circuit to compare. The components are the first generation of 600V trench field-stop IGBTs with the corresponding free-wheeling diodes. Here are the results:

Conduction losses	62W
Switching losses	28W
Total losses	90W
Efficiency	98,04%
Total rating of Si	630kVA.

Furthermore, the mixed voltage three-level topology circuit combines the low conductive losses of the half-bridge solution with the advantages of switching only between DC+/- and the NP. Here, we have the disadvantage that the outside transistors have to be rated with 1200V; this limits the switching performance to the level provided by 1200V components.

The components used in the benchmark are high speed 1200V IGBTs and free-wheeling diodes for the outside switches, and the first generation of 600V trench field-stop IGBTs with the corresponding free-wheeling diodes for the NP-switches. However, here are the results:

Conduction losses	50W
Switching losses	40W
Total losses	90W
Efficiency	98,04%
Total rating of Si	810kVA.

Conclusion

The comparison shows that with both three-level topologies an efficiency of 98.04% is achievable, compared to 96.65% for the standard three-phase bridge. The effort in semiconductor cost is 550kVA, compared with 630kVA for the NPC, but the components of the NPC will stay cooler so that they could be used at higher currents. In a comparison of maximum output power at 16kHz, the NPC module will be lower in cost than the module for a standard half-bridge. The mixed voltage three-level topology achieves the same efficiency as the NPC topology, but with the need for a total semiconductor rating of 810kVA compared to 630kVA

Figure 6: Standard inverter with three half-bridges

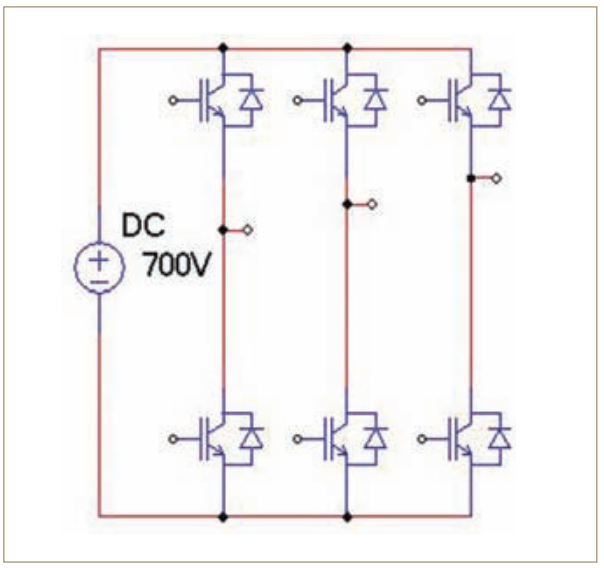


Figure 7: NPC topology

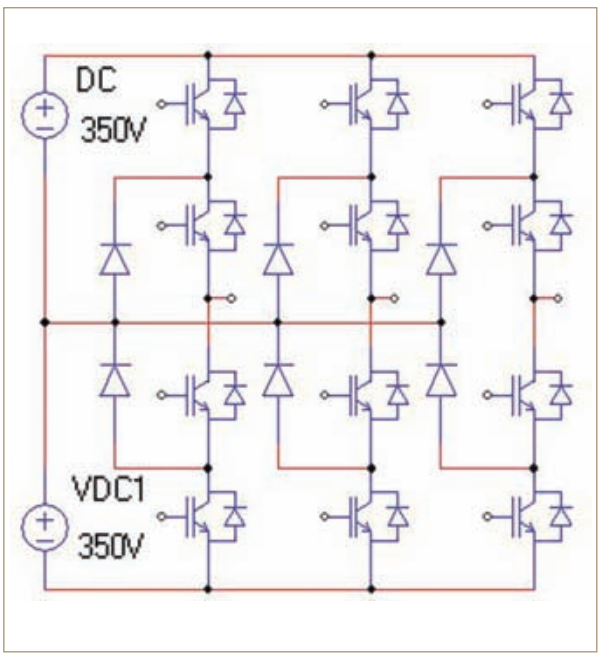


Figure 8: Mixed voltage three-level topology