Analysing the Hot Spots in Automotive Circuits

Automotive electronics have to perform in temperatures up to 140°C and to avoid thermal issues or, even worse, potential system failure under extreme operating conditions. Thus, it is vital to simulate the operational environment and analyse thermal performance of power devices in transient and worst case scenarios prior to implementing system design-in. **Sanmukh Patel and Gerry Balanon, Mixed Signal Analog – Automotive Group, Texas Instruments, Dallas, USA**

The increasing integration of circuitry that is taking place to satisfy the ever greater functionality and performance expected by modern automotive electronics, and the smaller packages that result, are introducing complex thermal challenges. These have to be successfully addressed and understood if changes are to be made to power load control, power supplies themselves and heat management methods.

The use of copper plane-based printed circuit board (PCB) thermal management, for example, instead of the traditional metal heatsink means that ICs have to be partitioned to optimise efficiency and cost. However, today's modules use lower switching frequencies for switch mode power supplies, large passive components, have linear regulators with inefficient voltage conversion for specific regulators, and quiescent currents to drive the internal circuitry.

Getting heat out of the system

Since a smaller package size leads to a high concentration of heat producing elements, the result is very high heat flux. Not only that, but there are other power devices on the printed circuit board, which may influence the temperature of the device under analysis, as well as system space and airflow constraints that must be considered. Figure 1 shows the three levels of thermal management to be considered in a typical package.

With optimal efficiency, size and cost as key objectives, lead frame-based thermally enhanced packages, such as heat slugs or exposed pad and heat spreader types designed to improve thermal performance are now being used more frequently. In some surface mount packages, special lead frames are employed, which fuse several leads on each side of the package to ensure a good thermal path to transfer heat from the die pad.

Accurate models of the silicon design

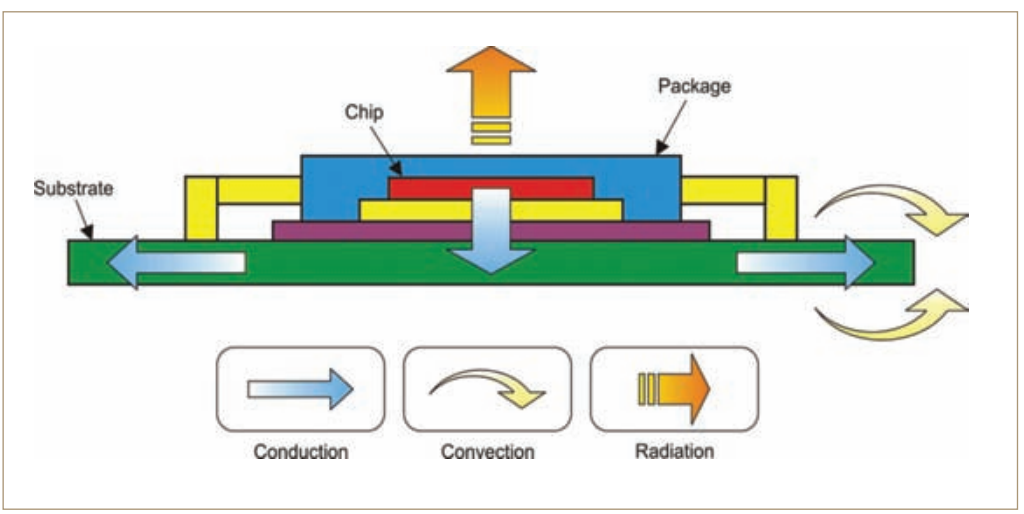

Figure 1: **Typical heat transfer path in an IC package**

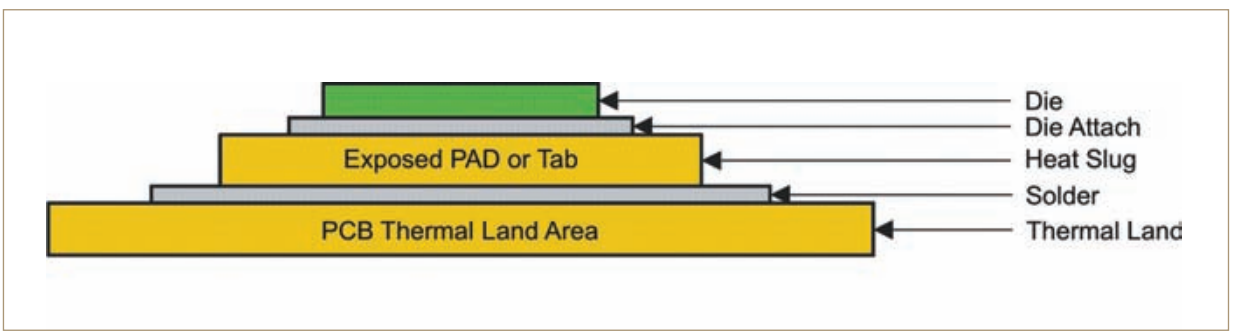

Figure 2: **Cross-section of the interface materials**

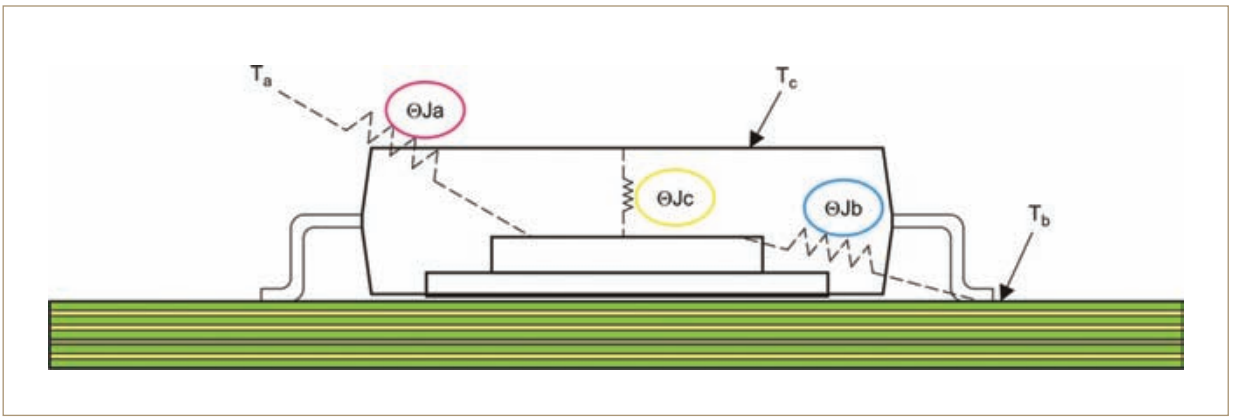

Figure 3: **Thermal resistive path for heat transfer**

package used and the thermal properties of the casing are essential requirements in order to carry out precise thermal analysis. This involves close collaboration between the semiconductor vendor and the OEM, with a full understanding of the end use or application. Since power FETs account for a large percentage of the die area, IC designers need to be armed with a proper analysis to choose the optimum size of device to handle normal and worst case power dissipation scenarios.

Establishing an accurate model for the silicon design package in power applications involves several key parameters, and will typically rely on a metal tab being exposed on one side to provide a low thermal resistance path to the heat extraction plane. The first parameter to be considered is the aspect ratio of the silicon die size to the die thickness. The area and location of the power device in the package plus, of course, any supporting drive circuitry that may contribute to heat is also important.

Then power diffusion within the silicon thickness of X-µm has to be taken into account. Next, there is the question of the interface of the silicon with the exposed metal pad or tab, which is affected by the die's attachment area and thickness. This parameter may include specifications such as percentage voiding of the die adhesive material, typically epoxy. In this case, and if desired, the simulation can place this under the power structures for worst case analysis.

Finally, the area and thickness of the exposed metal pad or tab, as well as the size of the package complete with mould compound and connection leads, must be taken into account, along with the thermal conductivity of the materials employed and any temperature dependency variations.

Thermal resistance affecting heat transfer

Accurate simulation also involves determining the thermal resistance affecting heat transfer from the pad to the heatsink material. There are several options here depending on the module and heat generated. These include multilayer FR4 PCBs, single-sided PCBs, or top and bottom layer PCBs.

The methods of heat extraction and resistance path can also vary depending on which of the following three alternative techniques is used: 1) thermal vias from the heat pad or tab attached to the inner heat sink plane, with the exposed pad or tab being soldered to the top layer of the PCB as shown in Figure 4; 2) an opening on the PCB underneath the exposed pad or tab for contact with a protruding heat sink pedestal connected to the module metal case; or 3) a heatsink copper (Cu) plane on the top or bottom side of the PCB board connected to the metal case by means of a metal screw, with the exposed pad or tab being soldered to the top layer of the PCB, as shown in Figure 4.

The weight or thickness of copper plating used on each layer of the PCB (typically either 28.38g/35µm on the inner layers and double that on the outer layers, or 28.38g/35µm on all) is another parameter to be considered for thermal resistance analysis, especially those layers that are attached to the exposed pad or tab – usually the top, heatsink and bottom layers in a multi-layer board.

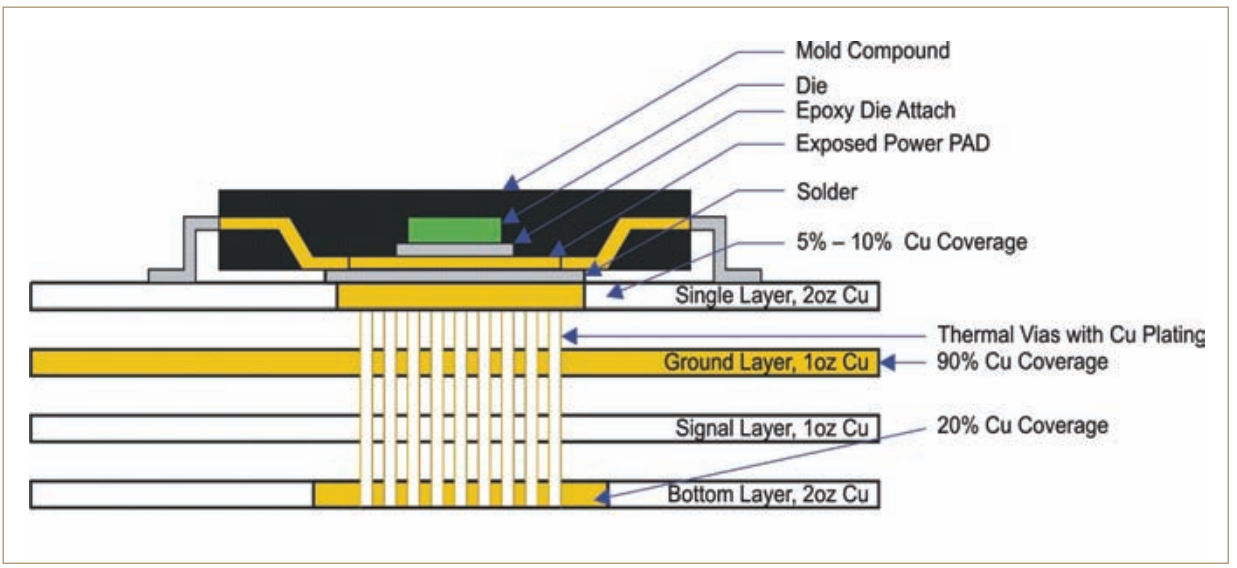

Figure 4: **Example of cross-section of implementation (thermal vias to Cu heatsink plane)**

The simulation model

In order to simulate die temperature, a layout of the IC is of course needed. As already indicated, the size of each FET and the aspect ratio of the silicon die size to its thickness for heat distribution are important parameters to be taken into account. The location of the FETs on the silicon die is influenced by whether or not these devices are powered simultaneously or sequentially.

Static or average power dissipation analysis in the model requires less computation time and converges once the highest temperatures are recorded. Transient analysis, however, requires a power versus time profile. The data is recorded with much finer resolution steps than the switching power profile to capture the peak temperature rises accurately during a fast power pulse. This analysis generally takes longer and requires much more data input than a static power simulation.

Figure 3 illustrates the different thermal resistances, which influence heat transfer in the package. Die junction to ambient resistance θja is generally used for thermal package performance comparisons, but is not a good reference to predict die junction temperature. Die junction to exposed pad resistance θjp is generally used as a good reference to predict die junction temperature. Die junction to case top resistance is indicated by θjc and θjb represents the die junction to board below one lead resistive path.

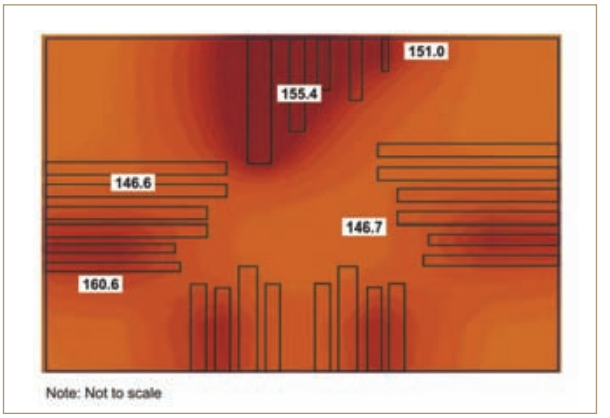

Figure 5: Example of a result from the thermal simulations

Data attained from the simulation model might indicate that minor adjustments are necessary in order to reduce the power FET's maximum temperature on the die near the top to prevent the hot spot from exceeding the T-junction of 150°C shown in Figure 5. Furthermore, controlling the power profile for this particular sequence to reduce the power temperature on the die might be an option.

Conclusion

Effective automotive power product development is, among other considerations, dependent upon a thorough understanding of the materials of manufacture and their thermal properties. The data gained from accurate simulation, enabling the different thermal resistive paths and heat transfer characteristics to be properly taken into account, is vital in order that systems can be optimised.

Although not specified in data sheets, it can also be used to provide a reference point when correlating any de-rating factors for any increase in ambient operating temperatures.

Literature

For more information about Packaging and Thermal reference information: http://www-s.ti.com/sc/techlit/slma002.pdf