Novel 3.5kV Low Loss Rectifier Diode

IXYS introduces a 600A 3 to 3.5kV diode with a low forward voltage drop, low leakage current and with an extremely high surge current rating. The experimental findings are consistent with numerical modelling results and show that by using Aluminium isolation diffusion, it is possible to get an ideal plane parallel breakdown voltage of 3500V. The diode utilises standard glass passivation and demonstrates stable blocking characteristics with low reverse current after High Temperature Reverse Bias (HTRB) and Humidity testing. **J.V. Subhas Chandra Bose and Peter Ingram, IXYS Semiconductor, Lampertheim, Germany**

The new diode is manufactured on 5in diameter silicon wafers and is available in chip (DWN344-35) and also in module form (MDD175-28/34), having a maximum voltage rating of 3.5kV and a current rating of 600A, with a maximum operating junction temperature of 150°C.

These devices have specially designed internal construction to prevent plasma escape under catastrophic failure conditions. The robust high reliability construction and the option for enhanced rupture capability, make these devices well suited for demanding applications such as the chemical industry, power supplies or track-side equipment for rail systems, supplies for DC power equipment, DC supply for PWM inverter, field supply for DC motors, battery DC power supplies, industrial drives, wind power converters and all rectifier and power conversion in the multi 100kW range. Futhermore, the devices are suited to any rectifier application which requires a diode with the combination of both high voltage and current rating, reducing cost in the mechanical sub-assembly over solutions using multiple lower power devices.

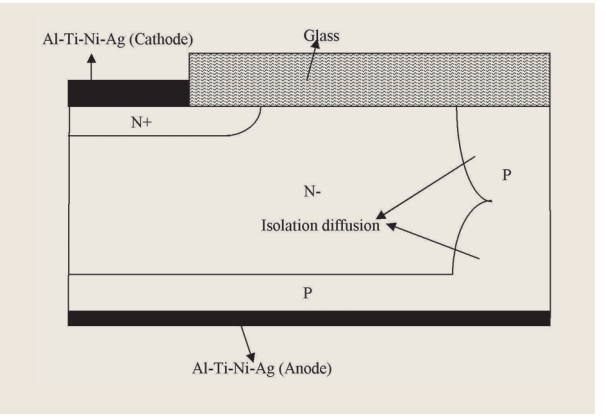

Figure 1: Schematic of novel 3500V diode

Table 1: Parameters used for DWN344-35 diode

N- thickness	460µm
Boron junction depth	39µm
N surface concentration	1E19cm-3
N- resistivity	150Ω-cm
Boron surface concentration	5E18cm-3

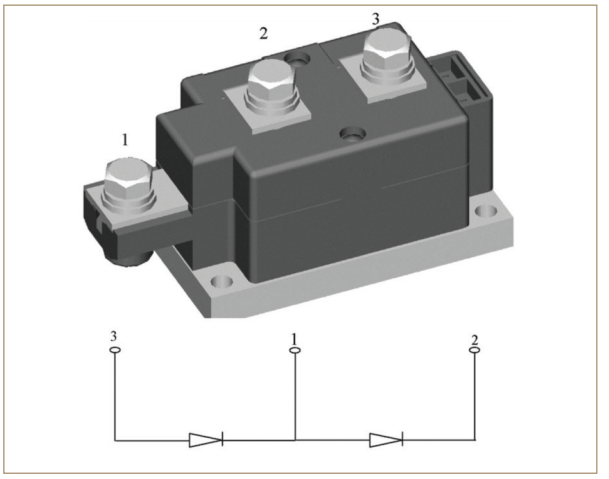

Figure 2: MDD175-34 module and internal chip assembly of MDD175-34 module

High-voltage diode technologies

In a planar diode, the use of guard rings as edge termination are used to increase the avalanche breakdown voltage, and to improve the reliability of a diode it is necessary to shift the maximum electric field from the surface to the semiconductor interior [1-10]. The blocking voltage is limited by the region of junction curvature where maximum electric field occurs. The blocking voltage of a diode can be increased by reducing the curvature effect either by using floating field limiting rings (FLRs), metal field plates or a combination of both. It has been shown that the FLR technique is sensitive to oxide charges and process variations. Optimal field plate designs involve multiple dielectric layers and gaps between metal field plates. Furthermore, using a forward diode it is possible to obtain 85 to 90% of plane parallel breakdown voltage.

In an Aluminium or Boron isolation diode, it is possible to obtain 100% plane

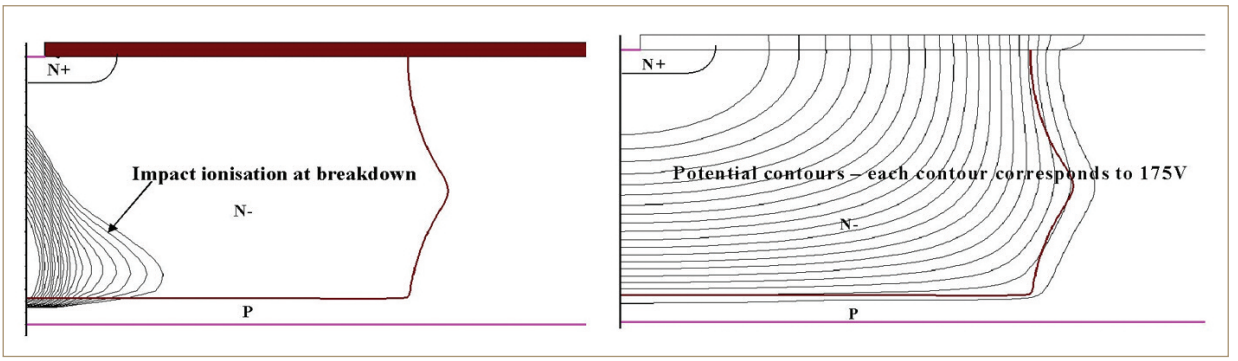

Figure 3: **Forward diode impact ionisation (left) and reverse diode potential contour at a breakdown voltage of 3500V**

parallel breakdown voltage because of absence of junction curvature. The diode consists of an N- type Si region with low doping concentration. The backside is deep diffused boron wafers in contact with the anode metal, and the front side has a phosphorus-doped region which is in contact with a cathode metal. The final passivation layer can be glass or metal field plate passivation. However, we used IXYS standard glass passivation for the reverse diode.

3500V diodes have been investigated which are insensitive to surface charge during processing and after High Temperature Reverse Bias (HTRB) and humidity test. Optimisation of the structure and analysis of the breakdown voltage characteristics is carried out using ISE TCAD software [11].

Numerical computations and experimental results

The cross-section of the 3500V diode is shown in Figure 1, and the diode parameters used for simulation as well as for processing are shown in Table 1. Figure 2(a, b) shows the MDD175 module and internal chip assembly. Figure 3(a, b) shows simulation results of impact ionisation and the potential contour of a diode at breakdown voltage. Impact ionisation occurs at the main junction and the device breaks down at 3500V, which is 100% of plane parallel breakdown voltage.

A diode with chip size of 12.5 x 12.5mm was designed and fabricated using 5in starting Si wafers. For isolation diffusion aluminium is used as a source, because solid solubility of Al to the Si is higher than boron. Influence of forward voltage drop on temperature is shown in Figure 4 and leakage current can be seen during reliability test results. Practical results clearly show that devices have less negative temperature coefficent with respect to temperature. Therefore, more devices can be connected in parallel.

Surge current tests were conducted on five chips with an increase in steps of 200A. Devices passed till 8.8kA and from 9kA chips began getting destroyed.

Reliability

Reliability is defined as the ability of a device to conform to its electrical and visual/mechanical specifications over a specified period of time, under specified conditions, at a specified confidence level.

Prior to the official release of a new device for mass manufacturing, it must undergo full qualification test. New device qualification most often requires several sets of samples for different reliability tests. The actual reliability of a device cannot be accurately determined with standard visual and electrical measurement techniques. The most important reliability tests for the electrical stability of the chip are High Temperature Reverse Bias (HTRB) and Humidity test.

HTRB: This test checks the ability of the samples to withstand a reverse bias, while being subjected to the maximum ambient temperature that the parts are rated to withstand.

Humidity: This test checks the ability of the package and chip to resist moisture penetration. The sample is loaded into an environmental chamber. The relative humidity is then increased from 85 to 100%, and the temperature is also elevated.

HTRB and Humidity test samples are randomly selected from 25 processed wafers. The condition used for HTRB test is 80% of rated voltage at 125°C. The breakdown voltage and leakage current were measured before starting the test. Devices were assembled into the plastic package with Sylgard 567. The test was conducted for up to 168hr and readings were taken once every 4hr. Figure 5 clearly shows that leakage currents are below 500µA. Furthermore, there is no increase in leakage current between pre and post measurement results.

The device characteristics are measured before starting the test. The humidity test was conducted at 85°C and at 85% relative humidity for 168hr. The device characteristics are re-measured after cooling down for two to three hours.

Pre and post measurement results show that there is no increase in leakage current. The maximum leakage current at room temperature is 200µA, and at 125°C it is 450µA.

Conclusion

Simulation analysis and practical results show that by using aluminium isolation diffusion and glass passivation for 3500V

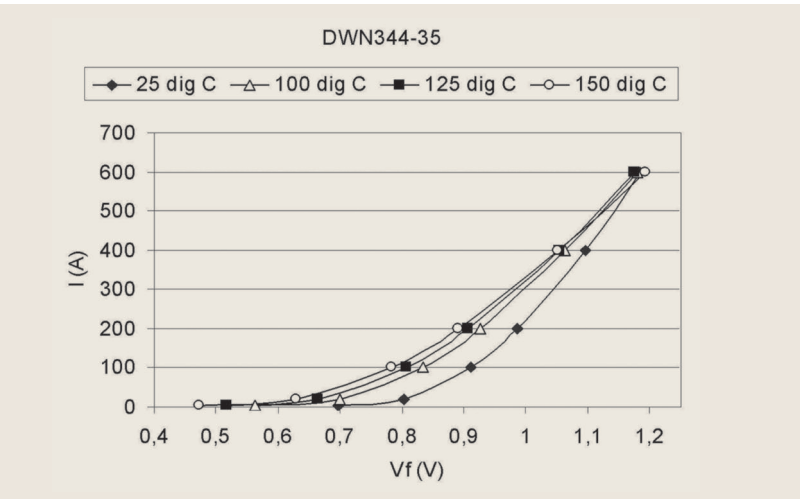

Figure 4: **Forward voltage drop with respect to temperature**

diodes, it is possible to obtain ideal plane parallel breakdown voltage. Experimental results show that the device guarantees low leakage current at 25 to 125°C conditions, plus long-term stability of the blocking characteristics, even in plastic packages.

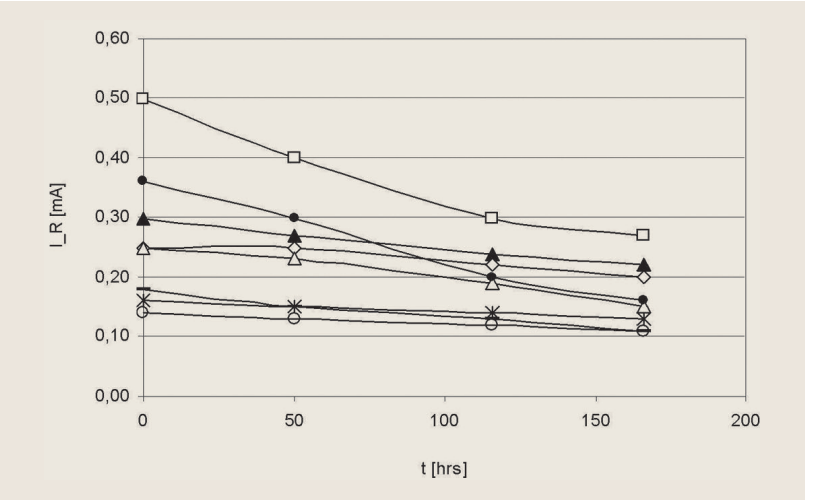

Figure 5: **HTRB test results**

Literature

[1] H. Yilmaz, 'Optimization and surface charge sensitivity of high-voltage blocking structures with shallow junctions'. IEEE Trans. Electron Devices, Vol. ED-38, pp. 1666-1675, 1991.

[2] D. Jaume et al., 'High-voltage planar devices using field-plate and semiresistive layers,' IEEE Trans. Electron Dev., Vol.9, 1993.

[3] T. Stockmeier, P. Roggwiller, 'Novel Planar junction termination technique for high voltage power devices,' pp.236-239, ISPAD 1990.

[4] S.Yasuda and T. Yonezawa, 'High voltage planar junction with a field limiting ring,' Solid State Electron., Vol. 25, p. 423, 1982.

[5] V. Anatharam and K.N. Bhat, 'Analytic solution for the breakdown voltage of punchthrough diodes having curved junction boundaries at the edges,' IEEE Trans. Electron Devices, Vol. ED-27, p. 939, 1980.

[6] M.M. De Souza, J.V. Subhas Chandra Bose, M. Sweet, O. Spulber and E.M. Sankara Narayanan, 'A Novel, Area Efficient Floating Field Limited Ring edge termination technique,' Solid State Electronics, Vol. 44, pp. 1381-1386, 2000.

[7] J.V. Subhas Chandra Bose, M.M. De Souza, E.M Sankara Narayanan, G. Ensell, T.J. Pease, J. Humphrey, 'A novel metal field plate edge termination for power devices', Microelectronics Journal, Vol. 32, No. 4, pp. 323-326, 2001

[8] F. Conti and M. Conti, 'Surface breakdown in Silicon planar diodes equipped with field plates', Solid State Electron., 15, pp. 93-105, 1972.

[9] Yuming Bai, Alex Q. Huang and Xuening Li, 'Junction Termination Technique for Super Junction Devices', ISPSD 2000., pp. 257-261.

[10] B.J. Baliga, Power Semiconductor Devices, PWS publishing, 1996.

[11] ISE TCAD Release 10.0, Zurich, Switzerland, 2004.