New 1200V SPT+ IGBT and Diode for High Temperature Applications

The application spectrum for the 1200V voltage class chips and modules is increasing worldwide due to the constant increase of power electronic systems present in various fields like automotive, industrial, regenerative power sources etc. Higher demands for improved electrical performance and reliability due to the increased levels of power and switching speeds in modern applications have resulted in development efforts for more optimised devices capable of withstanding such conditions. Moreover, a common trend of operating the devices under junction temperatures up to 175°C is present. **Bulent Aydin and Marta Cammarata, ABB Switzerland Ltd, Semiconductors, Lenzburg, Switzerland**

The SPT+ Enhanced-Planar technology was introduced in 2005 and covers voltage classes ranging from 1.2 to 6.5kV. During the current development of an improved SPT+ 1200V chipset, the IGBT was further optimised for higher reliability at higher temperatures, while keeping the electrical performance. Furthermore, a newly developed diode is designed for high reliability, soft recovery and low forward voltage drop.

1200V SPT+ IGBT and diode

The SPT+ IGBT design is shown in Figure 1. Its development target was to reduce the on-state losses by introducing an N-enhancement layer surrounding the channel P-well. This improves the plasma concentration at the emitter side and therefore lowers the on-state losses. On the other hand, the newly developed diode is based on a pin-diode design utilising a combined local and uniform lifetime control. A schematic cross-section is also shown in Figure 1. The optimised shape of the stored electron-hole plasma ensures a low forward voltage drop and soft reverse recovery performance.

Additionally, a state-of-the-art passivation design was developed for the new chipset including Silicon-Nitride and Polyimide layers ensuring high mechanical and environmental robustness and reliability, especially important when operating at higher temperatures.

The static and dynamic performances were extensively measured and evaluated to ensure matching the outstanding turn-off ruggedness even at high temperatures. Also the high levels of IGBT short-circuit capability are proven, despite the low on-state and switching losses.

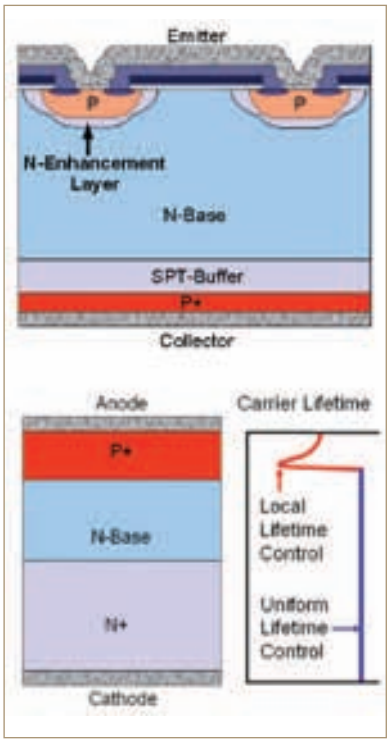

Figure 1: Schematic cross-section of the SPT+ IGBT (top) and diode (bottom)

Static and dynamic performance

The measurements presented here are performed on IGBT and diode chips rated for 100A nominal current, with an active area of 104mm² for the IGBT and 50mm² for the diode.

The IGBT electrical characteristics include low on-state losses with a strong positive temperature coefficient, as shown in Figure 2. This is a very important feature for ensuring safe paralleling when chips are mounted in high current modules. At 125°C the IGBT shows a $V_{CE\,sat}$ value of 2V at 100A. The diode low forward losses with a positive temperature coefficient are also shown in Figure 2. At 125°C the diode VF shows a value of 1.8V at 100A.

Figure 3 shows the turn-off and turn-on switching characteristics under nominal conditions at 125°C for the 100A IGBT chip. In both cases, the current transients during switching are very smooth and soft with short-current tails resulting in low losses, low overshoot voltages and low EMI levels.

Under nominal conditions of I_C = 100A, V_{DC} = 600V and with a stray inductance

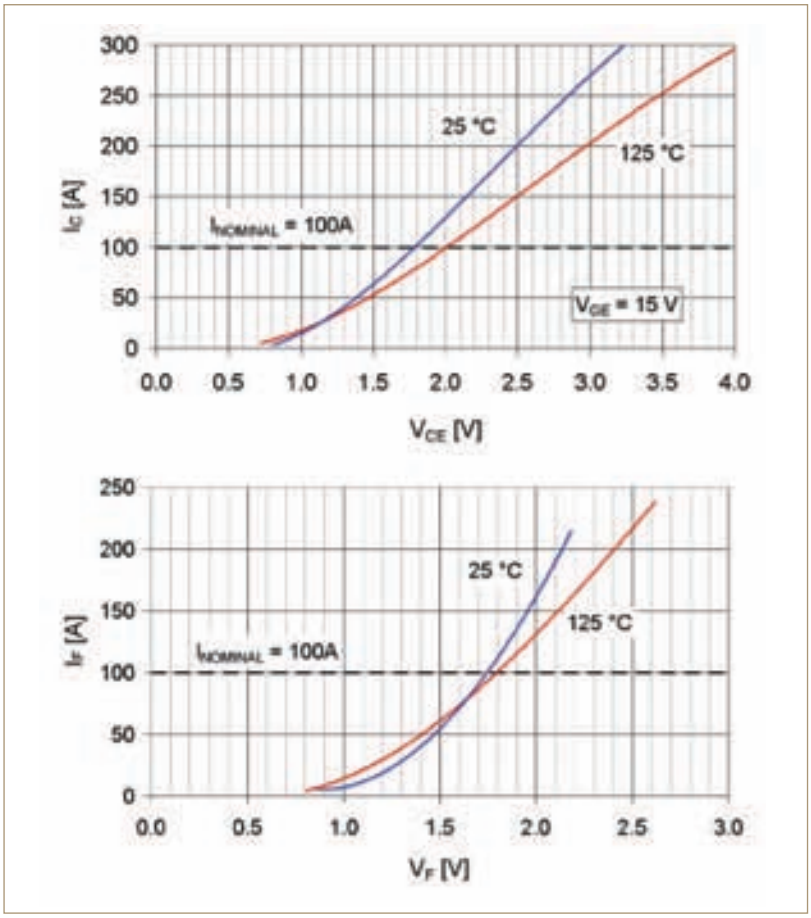

Figure 2: **On-state characteristics of the 100A IGBT (top) and diode (bottom)**

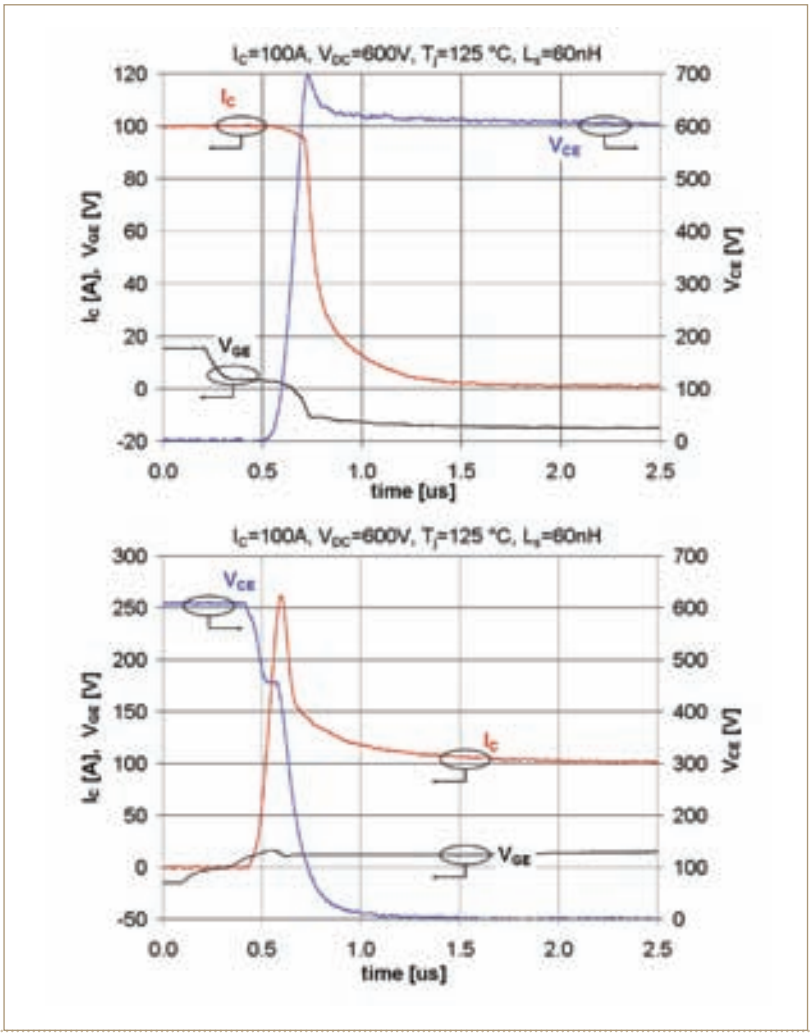

Figure 3: **100A IGBT turn-off (top)and turn-on (bottom) characteristic**

L_S = 60nH, the fully integrated switching losses at 125°C are: IGBT turn-off energy E_{OFF} = 11.9mJ and IGBT turn-on energy E_{ON} = 14.7mJ. The diode reverse recovery current behaviour is mirrored in the IGBT turn-on waveform. Also, for the diode the current transients during switching are very smooth and soft. Under nominal conditions of I_F = 100A, V_{DC} = 600V and with a stray inductance L_S = 60nH, the fully integrated reverse recovery energy is E_{REC} = 12.6mJ.

SOA performance

The excellent safe operating Area (SOA) ruggedness of the SPT+ technology is confirmed for the IGBT turn-off in Figure 4. A successful turn-off of 800A i.e. eight times the nominal current with a DC-link voltage of 1000V at 175°C, and a higher than standard stray inductance of 200nH is shown. The peak-power reached in this test was 800kW, while clearly surviving dynamic avalanche conditions and also successfully withstanding Switching Self Clamping Mode (SSCM) of operation. The measurement was done using a gate-emitter voltage of 20V. In the subsequent test-step of 850A, the IGBT went into current saturation and turned off in a short-circuit type mode. This shows that the IGBT has an excellent robustness being able to turn off all currents up to saturation at V_{GE} = 20V.

This test confirms the suitability of the IGBT for operating at higher temperatures since the SOA represents a main limitation towards operating silicon devices under such conditions.

The short-circuit capability of the new 1200V SPT+ chip is shown in Figure 5. The waveform shows how a 16µs short-circuit pulse was withstood at 175°C and with a DC voltage of 900V. The corresponding short circuit current is 400A and the total energy dissipated is 5.9J. The devices were also verified at a wide range of temperatures showing rugged performance under all short-circuit test conditions.

In Figure 6, the SOA ruggedness of the diode is demonstrated. The reverse recovery at 200A i.e. double the nominal current, with a DC-link voltage of 1000V at 175°C and with a switching speed of dI_F/dt=4900A/µs, i.e. twice the nominal switching speed, is shown. The resulting total peak power is 400kW, with the device withstanding clear dynamic avalanche conditions.

The softness reverse recovery test performed at 1/10th of the nominal rated current and at a higher-than-standard stray inductance of L_S = 200nH is shown in Figure 7. It confirms the diode very soft recovery behaviour with small oscillations at a peak overshoot voltage of 1050V.

The rugged design and improved passivation have enabled the new chipset

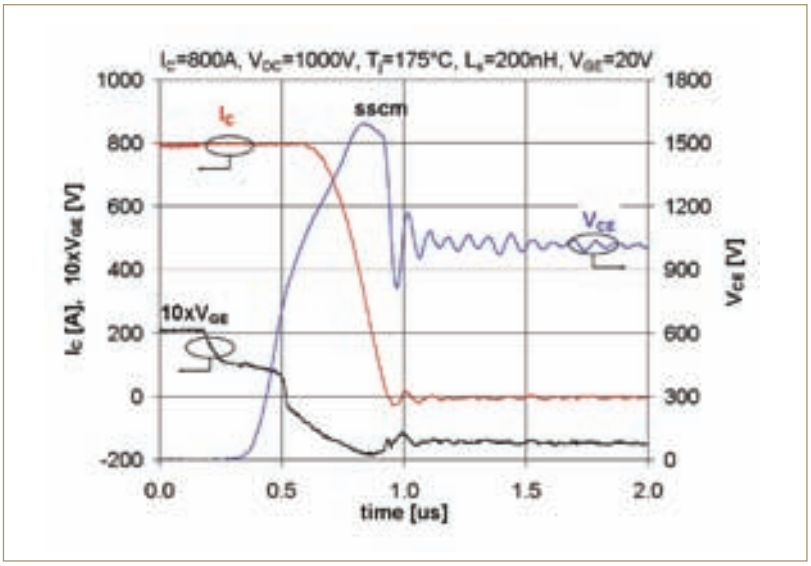

Figure 4: **IGBT turn-off under extreme conditions demonstrating the high ruggedness of the newly developed chip**

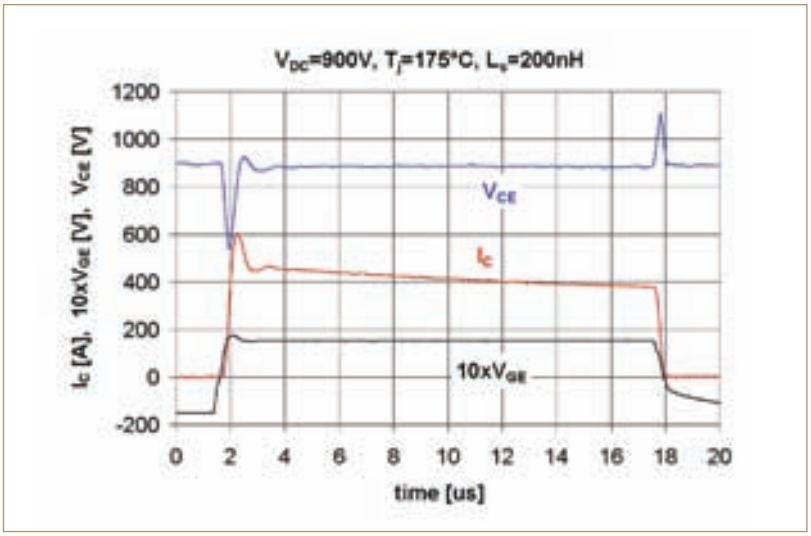

Figure 5: **Short circuit SOA waveform of the 1200V SPT+ IGBT**

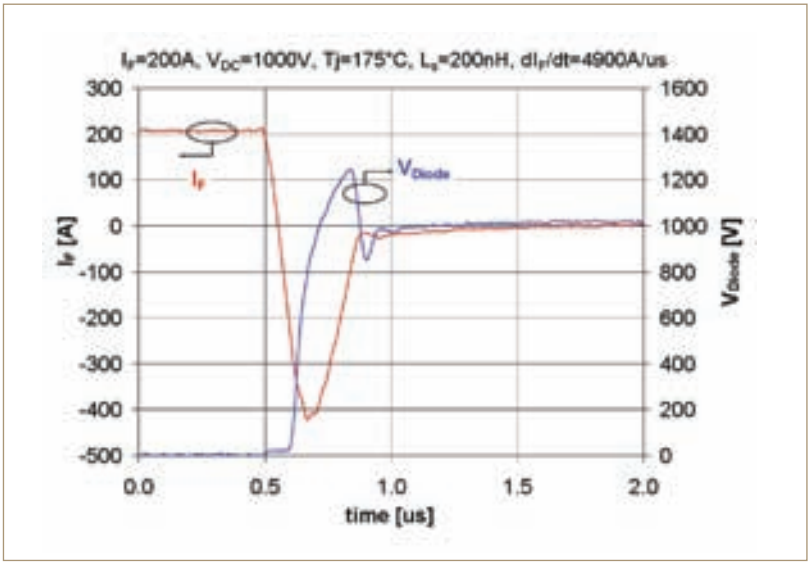

Figure 6: **Diode reverse recovery under SOA conditions**

to be seriously considered for the future applications targeting 175°C as a maximum operation junction temperature.

High reliability performance

The reliability of the new chip-set was qualified using a combination of standard tests including HTRB (High Temperature Reverse Bias), HTGB (High Temperature Gate Bias), THB (Temperature Humidity Bias), Cosmic Ray test and a newly developed test which combines high temperature, high humidity and high voltage.

More precisely, in this new test the IGBTs are switched with a frequency of 1kHz at an ambient temperature T = 85°C with relative humidity RH = 85%. The switched voltage is V_{DC} = 750V with an overshoot at the turn-off transient that reaches a peak value of 900V. The test is carried out at a

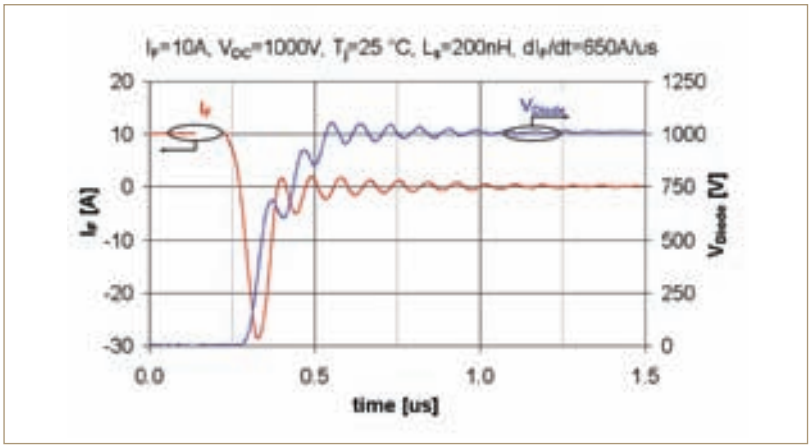

Figure 7: Softness reverse recovery for a 100A rated diode

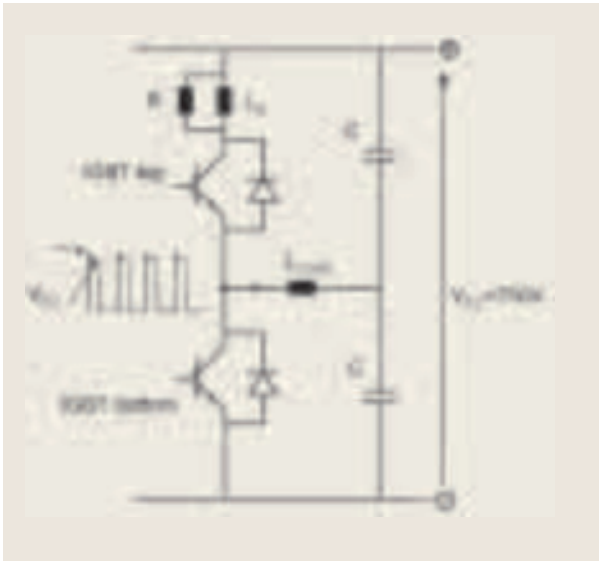

Figure 8: Circuit scheme used for the THB-V_{DCsw} test

relatively low current level. We called the test THB-V_{DCsw} (Temperature-Humidity-Bias, performed at the DC-link voltage and switched). The test circuit is shown in Figure 8.

It is evident how the switching at the nominal DC-link voltage imitates biasing conditions very close to those the device experiences in real field applications, while the acceleration property of the test is given from the high temperature and high humidity values.

Outstanding performance of the new chip-set was proven by testing over 1000hr without any failure. By comparing the measurements performed after test with the measurements done before test, the chips show very stable electrical characteristics and values. Further investigations are planned to obtain the chips' lifetime limits under nominal conditions, and also to provide a further acceleration factor by increasing the DC-link voltage levels.

Future developments

Current development efforts are targeting design parameters of the N-enhancement layer to exploit its development potentials. This investigation focuses on the presence of the N-enhancement layer which brings forth a reduction in the avalanche blocking capability of the device. Hence, the shape of the enhancement layer doping profile can be optimised, in order to maximise the enhancement feature and minimise the loss of blocking performance.

As shown in Figure 9, this is possible if the layer is narrow but with a higher concentration (red profile in the figure). A narrow N-layer has the advantage of generating a small modification of the electric field shape, and therefore less blocking capability reduction. The higher doping concentration of the N-enhancement layer has the advantage of increasing the enhancement effect and therefore lowering the on-state losses. Experimental results from fine optimisation of the enhancement layer have resulted in an increased enhancement effect and between 5 to 10% lower on-state losses for the same blocking capability.

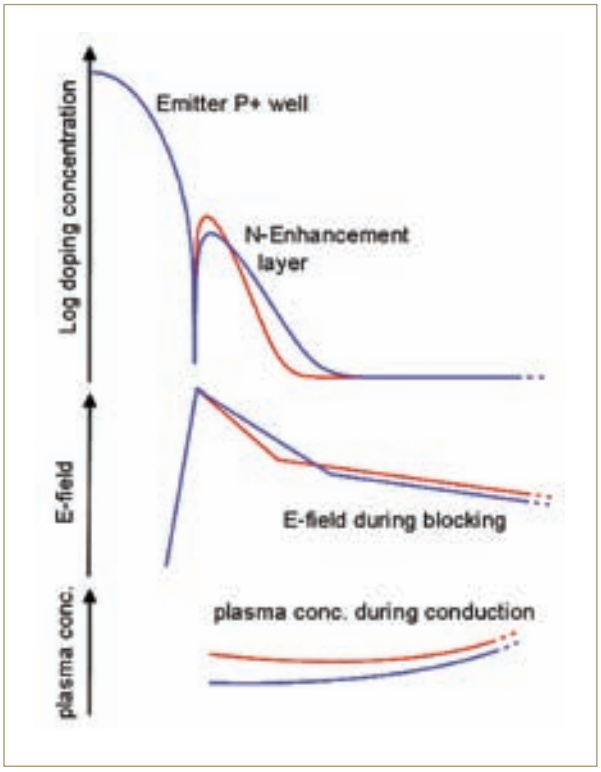

Figure 9: IGBT cell emitter doping profile and related electric field and plasma concentration for the enhancement layer