Integrated Gate Driver Circuit Solutions

Power electronics systems are commonly used in motor drive, power supply and power conversion applications. They cover a wide output power spectrum: from several hundred watts in small drives up to megawatts in wind-power installations or large drive systems. Inside the system the gate driver circuit with its extensive control and monitoring functions forms the interface between the microcontroller and the power switches (IGBT). This article provides an overview of different gate driver topologies for different power ranges and shows examples for monolithic integration of the driver functionality. **R. Herzer, J. Lehmann, M. Rossberg, B. Vogler, SEMIKRON Elektronik, Nuremberg, Germany**

Today's power conversion architectures are based on pulse width modulation (PWM) to control the power, the frequency and the voltage supplied from the mains to a given or unknown, fixed or variable load [1]. Switches, controlled by a driver, repeatedly connect the load either to a supply voltage or to ground. Depending on the switching pattern, many implementations of the basic principle are employed. For instance, current continuity can be ensured either by turning the switches on and off interchangeably or by switching only one of them and using the free-wheeling diode of the other. Generally, it will be possible to alter the shape of the current waveform passing through a load by varying the PWM high/low ratio [2].

Basic gate driver functionality

In power conversion systems using IGBTs (or MOSFETs) as semiconductor switches, the topology shown in Figure 1 is often adopted for each half bridge. The appropriate PWM patterns for the switches are generated by a microcontroller. The gate driver circuit with its extensive control and monitoring functions forms the interface between the microcontroller and the switches. The driver can be divided into a primary and a secondary side. The main functions of the primary side unit are shown in Figure 1.

A potential separation (insulation) between both sides is necessary because the primary side is normally related to the logic level and the secondary side to the emitter potential of the power device. Any control signals, and power supply to the secondary side gate driver circuits of both the high side and low side have to be transferred via this electrical insulation. Today there are many cases in which information (status or sensor information etc.) are also sent back via the insulation.

The secondary side gate driver circuit is mainly responsible for the optimal control of the active switches. The driver should utilise the potentials of the device in terms of current and voltage capability, losses and temperature. Furthermore sensor and monitoring functions are implemented to handle critical operation modes and to keep the device within the specified safe operating area (SOA). If a critical mode is detected by the gate driver or the additional sensor monitoring circuits, the driver circuit normally reacts independently of the supervising system (MC). To establish a 3-phase motor control, three branches on similar lines to those depicted in Figure 1 are needed. Additionally, a seventh switch is often employed to perform power factor correction. This low side switch could also be used as a brake chopper.

Gate driver topologies and insulation principles

In the range of 600V to 1700V (6,5kV) IGBT switches are commonly used in motor drives, power supplies and other power conversion applications. They cover a wide output power range from several hundred watts in small drives up to megawatts in wind power installations or large drive systems. The topology of the power system and the voltage and power range of the specific application are what determine the choice of the potential separation (insulation) between primary

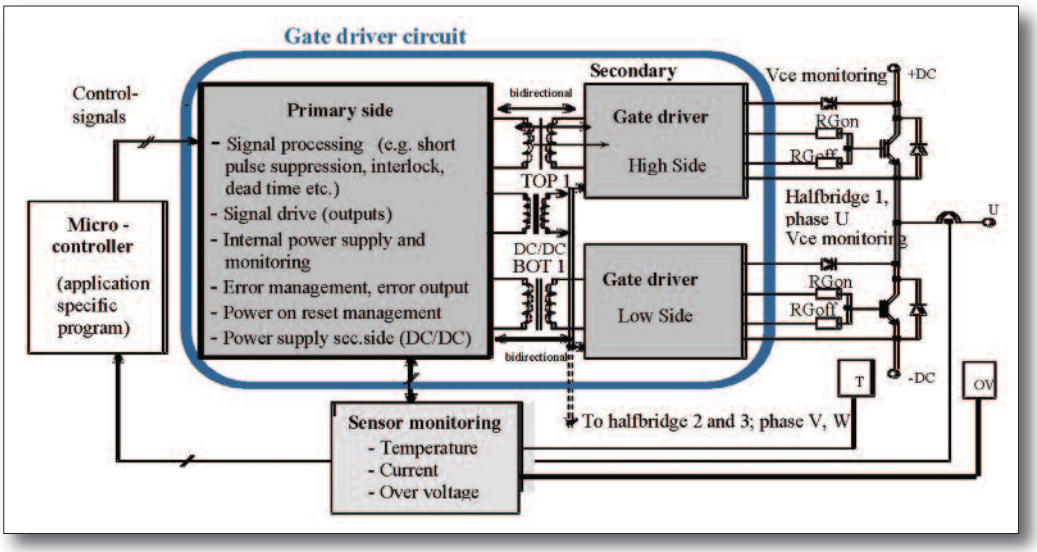

Figure 1: Basic topology of a power electronic system

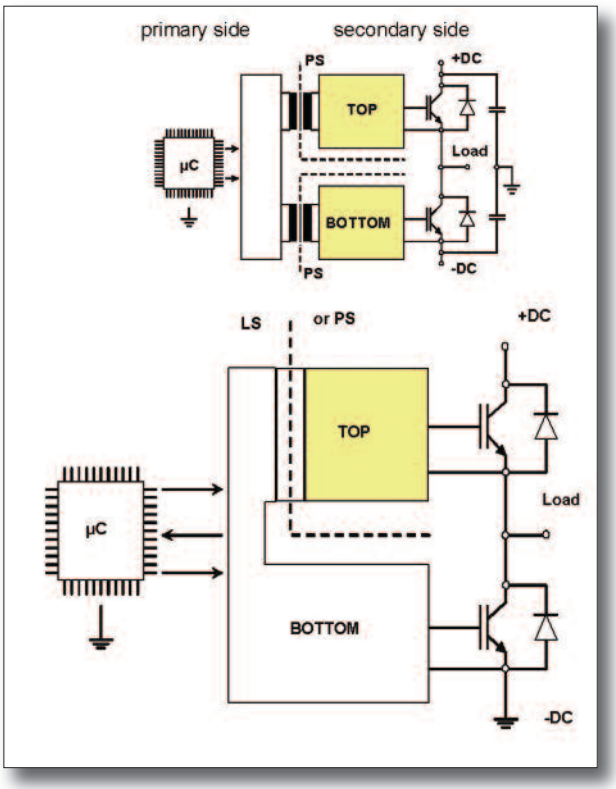

Figure 2: Example of symmetric (a) and asymmetric (b) grounded DC link and different potential separation (PS)

and secondary side. On the other hand, the form of potential separation selected has a significant influence on the driver circuitry, the reliability, noise immunity and the costs of the driver.

In a symmetrically grounded DC link circuit (Figure 2a) for medium and high power applications, external devices such as optocouplers, transformers or fibre optics are used for the galvanic insulation and the signal transfer. For an asymmetrically grounded DC link (Figure 2b) and low power applications, it is in principle possible to realise the potential separation only for the high side switch (TOP). The easiest way is an integrated level-shifter (LS, no galvanic insulation). In this case the microcontroller, the primary side, the emitter and secondary side gate driver of the low side switch (BOT) have to be on the same ground potential. Table 1 summarises the different techniques for insulation, signal and energy transmission in dependence on the application range.

IGBT gate driver solutions and ICs for high power applications

For some time now, effective system integration solutions have existed in the low power sector, [e.g.3-6]. In this mass-market environment, it is the ever-present need to cut costs which acts as the main impetus towards monolithic integration. State-of-the-art designs in the high power range, however, rely much less on dedicated ICs, because production quantities are smaller and the variety of product customisations, even for a relatively small number of units, is wider. Yet it is the conceptual difference between low power and high power designs which is actually most important. Only ICs specially developed under high power criteria [7 - 9] can adequately replace existing discrete solutions. But such ICs are necessary to reduce the number of discrete components at increasing functionality and lead to higher reliability, smaller volume and lower costs.

Primary and secondary side IGBT driver ICs for pulse transformer

A system structure particularly suited for coping with high currents has already been shown in Figure 1. The concept is centered on physical potential separation by pulse transformer (signals) and DC/DC converter (power supply) to divide the gate driver into one primary (per system) and one secondary side IC (per switch).

The SIXPACK configuration suggests that it is straightforward to merge all control functionality into a single IC. A six-channel primary side controller has thus been designed following the principle depicted in Figure 3.

Three TOP and three BOTTOM input signals come from the microcontroller. All incoming signals are synchronised with the clock generated on-chip. They are subjected to short pulse suppression and checked for potentially hazardous patterns. An interlock time digitally adjustable by the user is inserted between TOP and BOTTOM signals of each channel (TD1, TD2). Alternatively, a freely overlapping operation can be programmed (SELECT). The three main digital cores perform most of the functional signal processing. Several different modes of operation can be selected. A dedicated high power configuration is activated by the GBSYNC signal, allowing all three channels to be operated synchronously. By this means, IGBT half-bridges are driven with minimal mutual delay, whether they are connected in parallel for high output currents or in series for high voltage operation. The result is enhanced reliability and performance.

The logic signals to be transmitted to pulse transformers pass through level shifters and are then amplified by CMOS output driver stages.

Fault events such as supply voltage monitoring being triggered, or error flags being fed into the IC, are stored in an error memory. Errors specific to each half-bridge (e.g. short circuit) are preprocessed in the relevant main core. Depending on the error type, a characteristic pattern is generated by the error-coding unit.

A chip photograph of an IC realised in 1µm CMOS technology is shown in Figure 4. In the internal design, great emphasis has been placed on fault-insensitive, rugged design. As a part of the complex power-on-reset management, signal paths are safely blocked with supply-independent structures. Six 1A drivers serve to transfer the output patterns onto pulse transformers. Additional DC/DC control circuitry and output stages (2x 1A) are present for the secondary side power supply.

On the secondary side, single gate driver ICs are utilised. The functional block diagram of the IC selected is given in Figure 5. Any incoming signal is recognised

Driver type	Insulation	Signal transmission	Energy transmission	Application
Driver IC (Single, Halfbridge, Sixpack etc.)	no galvanic insulation	Level shifter (mainly for high side)	Bootstrap-circuit (for high side)	low power < 5kW
Hybrid driver (Single, Halfbridge, Sixpack etc.)	galvanic insulation	Opto-coupler Pulse transformer Fibre optic	DC/DC converter	medium power (5 ...100 kW) high power (> 100kW)

Table 1: Gate driver topologies, insulation and transmission principles depending on the power range

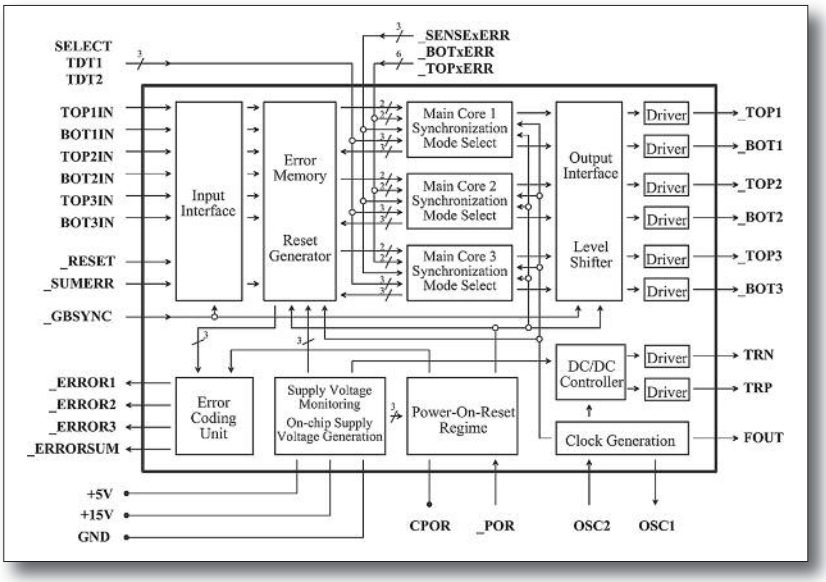

Figure 3: **Primary side IC block diagram [10]**

by the input interface. Depending on the system configuration, the signal patterns will be differently transformed for internal use. They are then fed into the central logic and error-processing unit. Finally, level shifters send them to the main output drivers, which deliver up to 3A of peak current to the IGBT gate. Thus, the IC is able directly to control IGBT modules up to 300A. If higher system power is required,

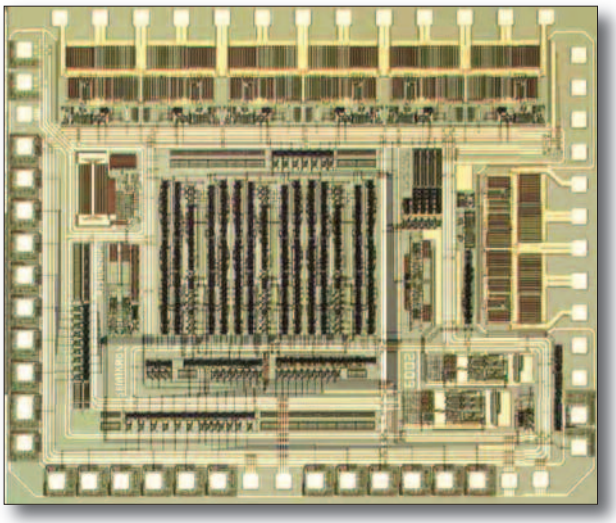

Figure 4: **Chip photograph, primary side controller (approx. 5.2mm x 4.3mm)**

external post amplifiers can be applied.

It was essential to design the input interface for high flexibility. Fig. 6 illustrates typical operating conditions at the input. Signal patterns transferred from the primary side are either optically coupled square waves with the IGBT turn-off voltage (DC-) as reference, or characteristic pulse transformer waveforms.

While the normal input IN recognises square waves, a pulse edge storage block (PES) connected to IN sets up the chip for pulse transformer environments. In this configuration, pulses are reliably latched by a feedback loop, ensuring high back swing immunity. There is an additional complication possible which will make it feasible to drive negative turn-off voltages at the output. For optimised turn-off losses and noise immunity, it is desirable to draw the IGBT gate potential below common ground. Internally, however, all circuits have to refer to the lowest potential on-chip. The required level shifting also takes place inside the input interface. As far as the negative turn-off voltage is concerned, system designers can choose freely between 0V and -8V.

The central logic is responsible for filtering out all signal patterns that could jeopardise the power semiconductor switches. External and internal voltages are monitored to identify threatening conditions. If the driver supply voltage were not monitored, the IGBTs might be switched on with too low gate voltage, thus leading to excessive power dissipation in the system. Likewise, any failure of the on-chip 5V supply requires to be handled to keep the system controllable.

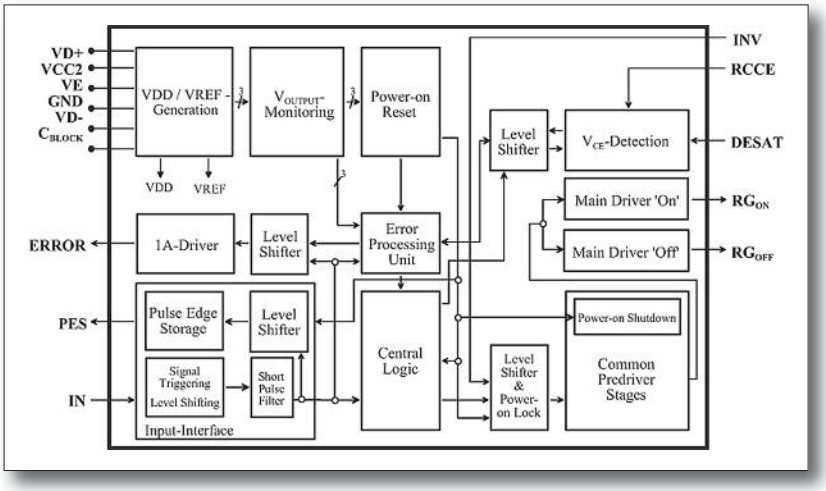

Figure 5: **Secondary side IC block diagram [11]**

to 100kHz. The theoretical maximum frequency was determined using 15V output swing and a load of 4.75Ω in series with 33nF capacitance. If power dissipation issues are disregarded, the peak current is not internally limited by driver delay until >180kHz.

IGBT driver ICs with digital core

In order to get a higher functionality and flexibility of IGBT driver for different

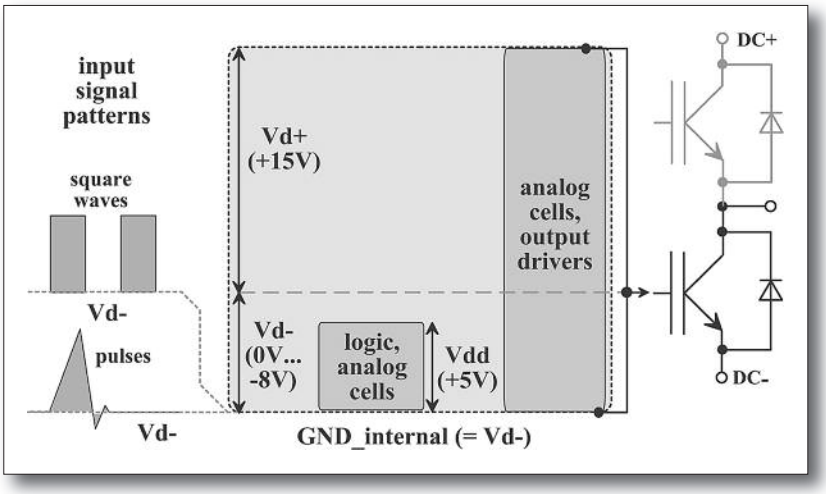

Figure 6: Typical waveforms and potentials at the interfaces

applications and/or to achieve sophisticated and repetitive signal transmission for all signals, including sensing signals, a fully digital driver is the most favourable and universal solution in the high power range [12]. Figure 8 shows the block diagram of such a new and innovative concept with the main features of the primary and secondary side control IC.

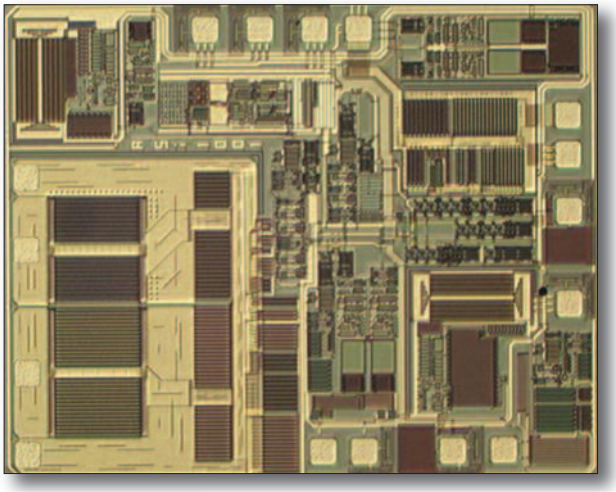

Figure 7: Chip photograph, secondary side IC (approx. 3.2mm x 2.6mm)

The principle block structure is similar to Figure 1 but the functionality of the primary and secondary side control IC is much higher and more flexible (programmable). The insulation and signal transmission between both sides is realised in both directions by modems. The digital-based signal transmission uses pulses with a defined length and shape generated by an internal digital logic. The pulses are almost independent of component parameters and are, in additional, evaluated differentially. Transmission reliability is achieved with high transformer currents and the far lower terminating impedance of the receiver. As a result of this and also of the relative independence from component parameters (modem), a high supply voltage for pulse generation is no longer necessary (3.3V is used).

On the primary side a bidirectional data transfer with the microcontroller is implemented (3.3V or 5V interface). Input signals from µC are monitored for critical frequencies. Short pulse suppression, interlock and dead time etc. are user configurable. Further features are listed in Figure 8. On the secondary side, the transferred signal is received by a differential windows comparator and transmitted to the digital logic for the secondary-side encoding and signal processing. By modulating the repetitively transmitted pulses, communication forth and back between the primary and secondary side can be achieved. Differentiated status or error signals, data and furthermore sensor signals (e.g. temperature of IGBT module) can be transmitted continuously.

Powerful 15V output stages are implemented to drive the gates of external post amplifiers (two MOSFET in a push-pull output configuration) separately, to avoid cross currents during switching. The output stage has two outputs for easy asymmetric gate control. This allows for the gate resistor to be split into two resistors for turn-on and turn-off, respectively. The main advantage, however, is that this solution allows for separate optimisation of turn-on and turn-off with regard to turn-on over-current, turn-off over-voltage spikes and short-circuit behaviour. Additionally, the digital logic core can be used to drive and control two output stages with different paralleled gate resistors. This allows for time dependency to be defined for effective gate resistor switching of the IGBT and, thus, for the IGBT switching

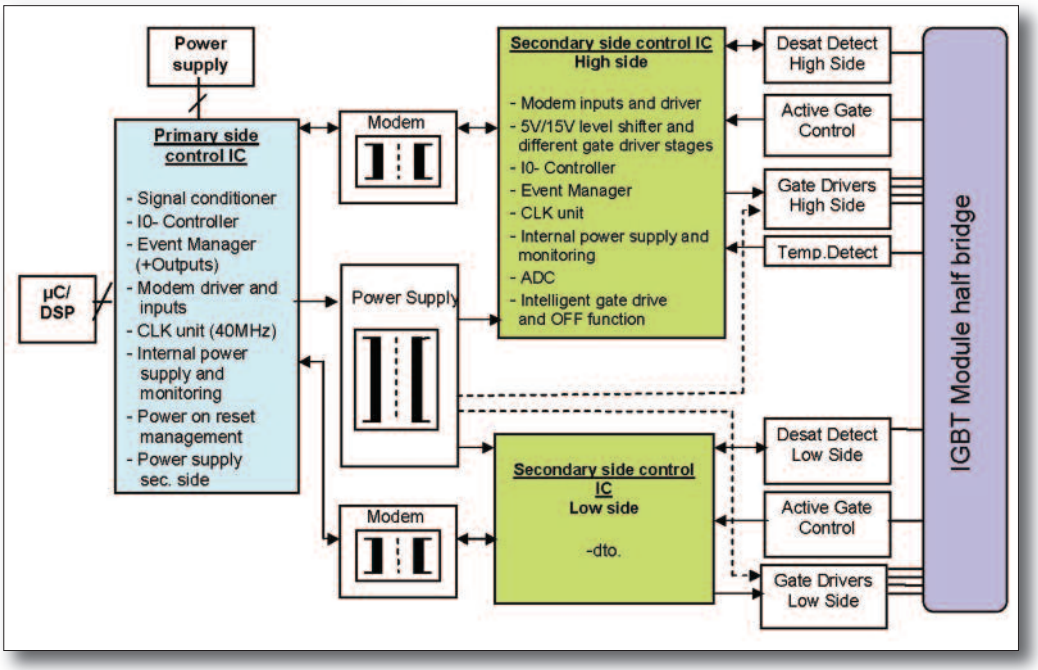

Figure 8: Block diagram and features of the digital driver concept

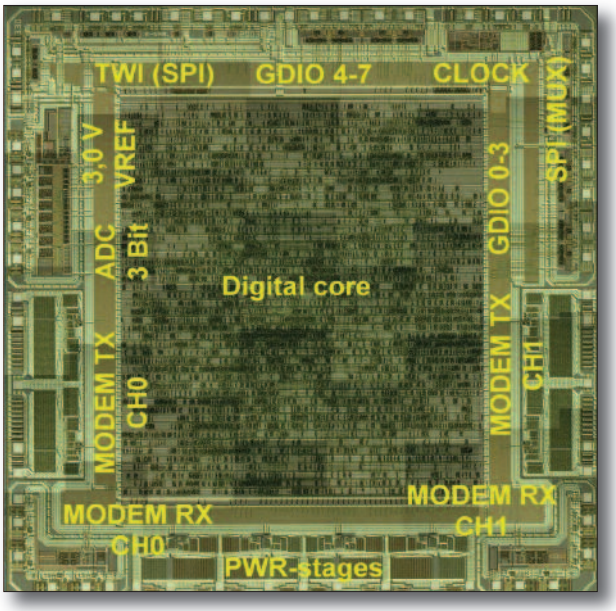

Figure 9: Chip photograph of digital driver primary side control IC (chip size 5.75mm x 5.9mm; digital core 3.5mm x 4mm)

time sequences to be modulated. This in turn means reduced switching losses and still allows for the over-voltage peak to be limited.

Starting the development with FPGAs on primary side and secondary side for digital signal processing [12], the complete digital and analogous functions of each side were integrated in a mixed-signal ASIC. Figure 9 shows the chip for the primary side control IC. The most important and visible circuit parts are marked. The ICs are realised in a CMOS technology which allows on the one hand synchronous design of the 3.3V digital core working at 40MHz and on the other the integration of powerful output stages (3.3V, 15V) and of circuit topologies suitable for +15V/-15V operation voltages. (To be continued in PEE 6/2010).

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