IGBT Gate Driver Solutions for Low and Medium Power Applications

Power electronics systems are commonly used in motor drive, power supply and power conversion applications. They cover a wide output power spectrum: from several hundred watts in small drives up to megawatts in wind power installations or large drive systems. Inside the system the gate driver circuit with its extensive control and monitoring functions forms the interface between the microcontroller and the power switches (IGBT). In this second part of the article fully integrated gate driver solutions for the low power range, their technologies, circuit aspects and specific designs are shown and discussed. **R. Herzer, J. Lehmann, M. Rossberg, B. Vogler, SEMIKRON Elektronik, Nuremberg, Germany**

IGBT driver solutions for low and medium power applications (600V, 1200V, <50A) are aimed at high volume markets, where system costs and geometric size per function are the most relevant parameters. IC-based designs are thus replacing conventional hybrid IGBT drivers [4, 14, 15, 16]. As already discussed in the chapter 'Gate driver topologies and insulation principles' [30] for an asymmetric grounded DC link and low power applications, the microcontroller, the primary side, the emitter and secondary side gate driver of the low side switch (BOT) can be placed on the same ground potential. In this case a potential separation is only necessary for the secondary side of high side switch (TOP).

System and high voltage IC design

Figure 10 shows a typical block circuit diagram of a 3-phase power conversion system with an additional 7th channel at the low side to support power factor correction schemes or to be used as a brake chopper. The topological blocks to be integrated into a gate driver HVIC are marked (orange). Depending on the different applications only high side- [17], half-bridge [14] and six-pack driver ICs [4] are also possible, as well as the integration of additional blocks such as bootstrap-diodes or charge pumps for power supply and VCE detection diodes and circuits.

The corresponding block diagram of a monolithic integrated 7-channel IGBT driver (Sevenpack) is given in Figure 11. Input interfaces (IIF) serve to process logic thresholds for direct connection to 5V or 3.3V microcontrollers. An interlock and dead time between TOP and BOT switch of a half-bridge is usually implemented in the external drive controller pattern but in many cases an additional hardware interlock and dead time is implemented in the gate driver as well as a short pulse suppression.

Three 600V (or 1200V) level-shifters transfer the signals to the fully insulated high sides, where the differential transmission signals are filtered and reconstructed. The signals are driven at the chip output by a CMOS stage. The output currents (sink/source) vary from several hundred mA up to 4.5A [19]. The driver operates normally at 15V ($V_{op,max}$ to 20V).

The branch delay times of the six main channels TOP/BOT1-3 are delay-matched to ensure synchronized switching. Logic and error management generate the appropriate internal signals. These take into account not only under-voltage lockout (UVLO, primary and secondary side) as derived from a bandgap-stabilized reference but also external analog sensor signals such as shunt current monitoring.

Complete integration of an IGBT gate driver exit demands the following technological requirements:

- Insulation technology for the certain electrical separation of low- and high-side circuit blocks. Here PN-insulation [4, 14], dielectric insulation (SOI) [6] and mixed technologies of both [20] are used today.
- High-voltage devices of the 600V and 1200V class respectively, which can be used as level-shifter (no galvanic insulation). The lateral DMOS-transistor

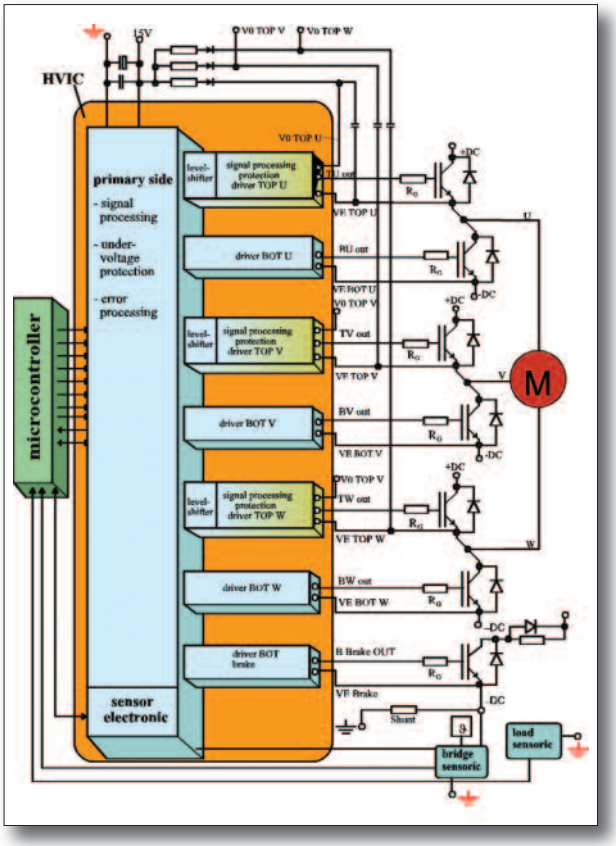

Figure 10: Power conversion system showing gate driver HVIC integration area

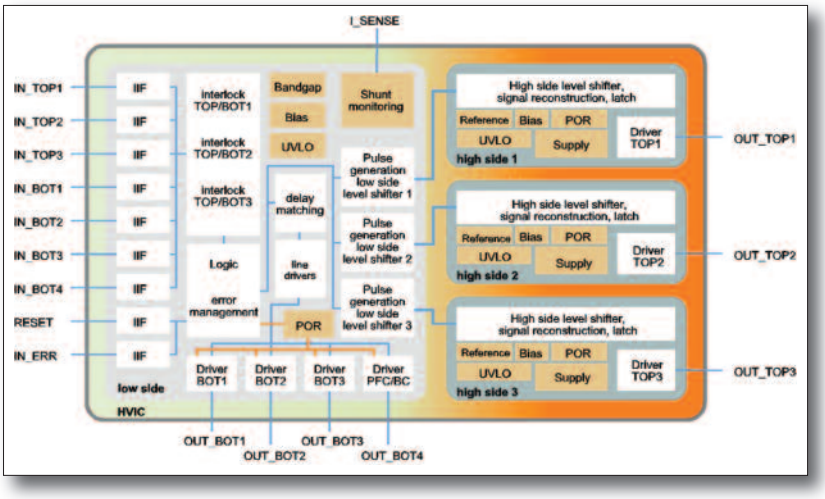

Figure 11: Typical block diagram of a monolithic integrated IGBT driver for seven switches (Sevenpack driver)

as classic RESURF (Figure 12) or as SOI-RESURF (Figure 14) device is the most common solution.

- Digital and analog circuits for operation voltages up to 20V for signal processing, control and driver functions on the low and particularly on the high side, where the ground potential is coupled on the emitter potential of the TOP switch and extreme voltage transients occur.

Gate driver in PN-insulation technology

The most important advantage of PN-insulation is that the device structures can be adjusted to the different voltage classes (600V, 1200V) by scaling of edge termination structure and doping concentration and depth of epitaxial layer, although of course the charges increase with the blocking voltage. This is shown in Figure 12 where the cross sections of the fundamental device structures are similar for the 600V and 1200V class, but the doping concentrations and distances are completely different. The full blocking voltage between high side and low side drops completely at the N- epitaxy / P-substrate junction and its lateral edge termination structure. Because of the large depth of N- region a parasitic coupling of the buried PN-junction on the active circuits on the surface can be avoided, especially at floating high side (Figure 12 middle). This makes the realization of sensitive analog circuits on the TOP-secondary side possible.

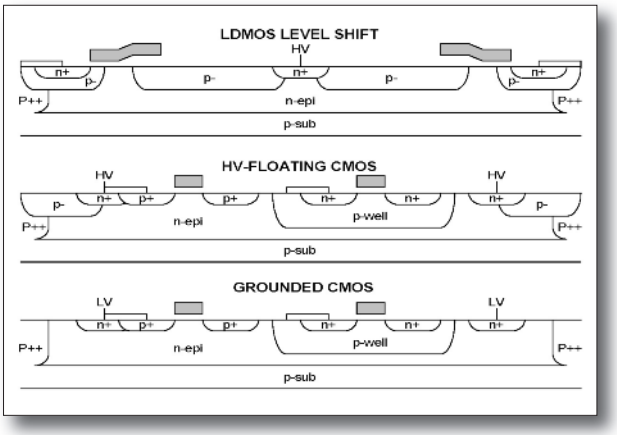

Figure 12: Fundamental device structures of a 600V/1200V PN-insulation technology [18]

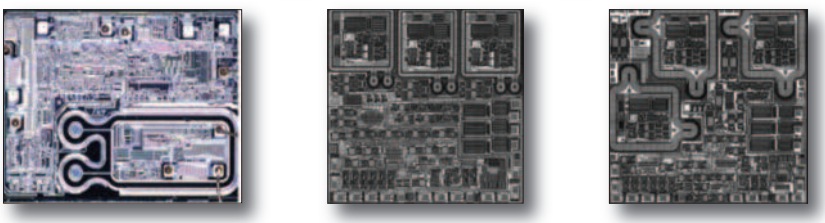

Figure 13: Chip photographs of different driver ICs in PN-insulation technology; left a 600V, 650/400 mA Halfbridge-driver [STM,14], in the middle a 600V, 500/250mA Sixpack-driver [IR,4,21], and right a 1200V, 500/250mA Sixpack-driver [IR,4,21]

Figure 13 shows chip photographs of different driver topologies, voltage and current classes of different manufactures. The insulated TOP secondary sides and their PN-edge termination structure around are clearly identifiable, as well as the driver output stages of every channel. In Figure 13 (left) and 13 (right) the differential level-shifters are embedded inside the termination structure while in Figure 13 (middle) the level-shifters are located separately.

Though the market has shown considerable interest in these compact and cheap high voltage driver ICs, the junction insulation has certain fundamental drawbacks. Negative transient voltages at the driver output can trigger internal parasitic thyristor structures, leading to latch-up. The problem can be somewhat alleviated by minority carrier suppression structures [22, 23] but it cannot be resolved completely. Also, PN leakage currents which increase with a factor of 4 per 10K temperature rise increase the losses and lead to an addition self-heating of the device which typically limits the operation temperature to 150°C.

Gate driver in SOI substrates

Appropriate high voltage silicon on insulator SOI-CMOS (600V) platform technology [24, 25] can provide complete latch-up immunity since all active devices are dielectrically insulated (see Figure 14). The regular CMOS circuits of the low side and the high side are based on quasi-bulk transistors in fully isolated silicon islands. This enables the operational temperature range to be considerably extended up to 200°C [6]. The active silicon is thick enough to prevent punch-through of the back side space charge region to the top side devices. The keys to the high breakdown voltages are the thick buried oxide layer and the selective layer thinning in the drift region of the high voltage devices.

Advanced level shifter concept

Even in low current applications and, yet more, in medium and high current applications, where high currents or high di/dt are switched, positive and negative voltage peaks may occur on parasitic elements in the power plane. These voltage peaks might cause a strong voltage drop between the primary and the secondary side of the gate driver (offset voltage). A negative offset voltage in particular is critical for junction-isolated HV-ICs [18, 14], commonly allowing only a few volts (typically -5V) below ground potential to prevent latch up [4]. Therefore the design goal for medium power applications is a significant extension of the

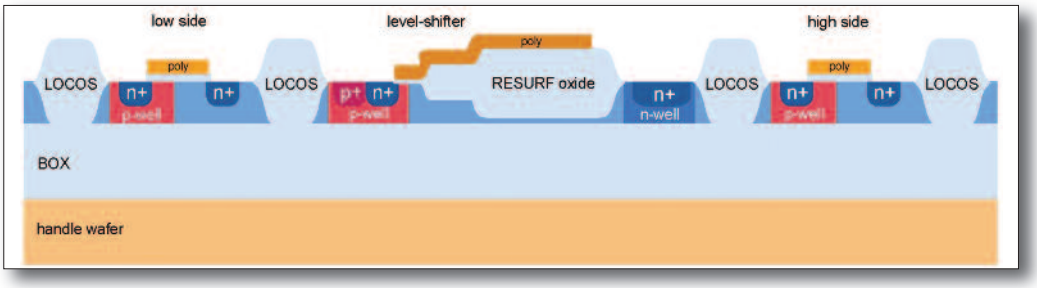

Figure 14: Schematic cross section of fundamental device structures of a 600V SOI-CMOS technology [24, NXP] [25]

range of the operational voltage shift between the primary side (control logic) and the secondary side (drivers). This requires an advanced level shifter concept for both the BOT and the TOP channel allowing "bipolar" operation.

The circuit principle of the BOT channel level shifter is shown in Figure 15. It consists of two independent transmission paths, an up-level shifter and a complementary down-level shifter. The configuration is that of a conventional static CMOS level shifter with additional diodes in each path. Both the up- and the down-level shifters use two cross coupled parallel branches with the function of a latch. Hence there are no cross currents under static voltage conditions. Because of the full dielectric insulation of each device, the circuit itself is latch-up free. For this reason and also that of the weak back gate effect

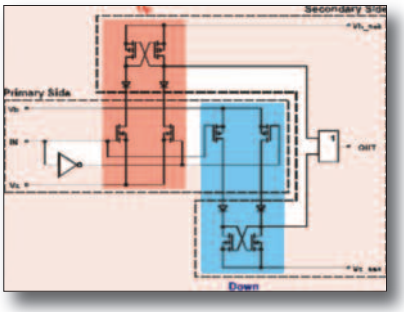

Figure 15: Circuit principle with up-/down- level shifter for the BOT channel

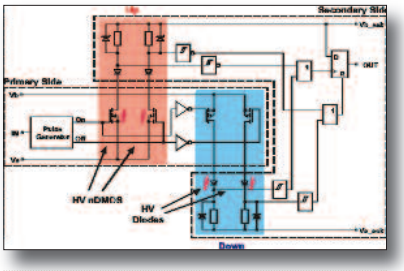

Figure 16: Circuit principle with up-/down- level shifter for the TOP channel

of the SOI technology used, every circuit part can carry any desired potential. The maximum allowable offset voltage is only limited by the breakdown voltage of the level shifter transistors.

Depending on the polarity of the offset voltage between the primary side and the secondary side ($V_{offset} = V_{vs\_sek} - V_s$) the up-level shifter ($V_{offset} \geq 0V$) or the down-level shifter ($V_{offset} \leq 0V$) transmits the applied input signal from the primary to the secondary side. The inactive path is blocked by reverse-biased diodes. To reconstruct the signal on the secondary side, a simple logic disjunction can be used.

The circuit principle of the TOP channel level shifter is shown in Figure 16. As in the case of the BOT channel, the level shifter consists of two complementary parts - the high voltage up-level shifter and the low voltage down-level shifter. Because there are no p-MOS devices available with a breakdown voltage extending to 600V, a pulsed signal transmission simply requiring high-voltage n-DMOS transistors and high-voltage diodes, to block the high reverse voltage in the down-level shifter, is used. A pulsed transmission is applied to minimize the cross current and power consumption but requires more complex signal generation and reconstruction in comparison to the BOT channel. The differential transmission with two branches per level shifter, a robust signal processing and reconstruction on the secondary side provide maximum immunity against parasitic coupling from the power plane.

Seven channel 600V gate driver design

Figure 17 shows the chip photograph of a 7-channel gate driver IC. It contains all the functionality needed for a 3-phase power system and a fourth independent BOT channel is implemented for PFC or brake chopper applications according to the power conversion system of Figure 10 and the block diagram of Figure 11. It is realized in a 600V CMOS-SOI technology [24] whose cross section is shown in Figure 14.

The three insulated TOP secondary sides with their HV-DMOS-transistors and HV-diodes of up-/down- level shifter circuit (regarding Figure 16) are clearly to recognisable, as are the output stages of the 3 TOP and 4 BOT channels with 1.4A/1.4A (source/sink) peak current at

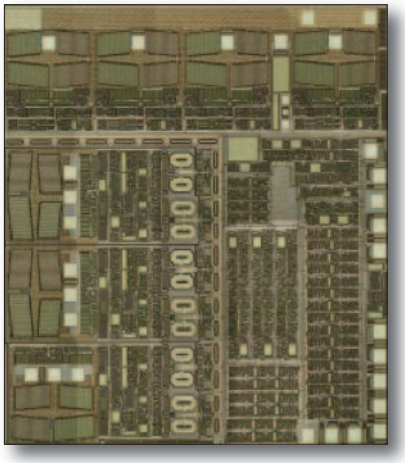

Figure 17: Chip photograph of a 600V/1.4A 7-channel gate driver IC in SOI-CMOS technology (chip size 4.6mm x 4.1mm)

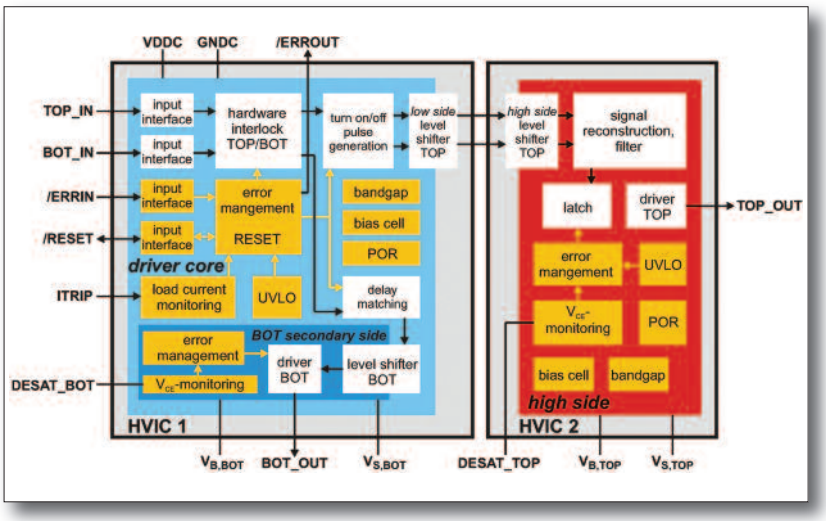

Figure 18: Block diagram of a two-chip 1200V SOI half-bridge gate driver

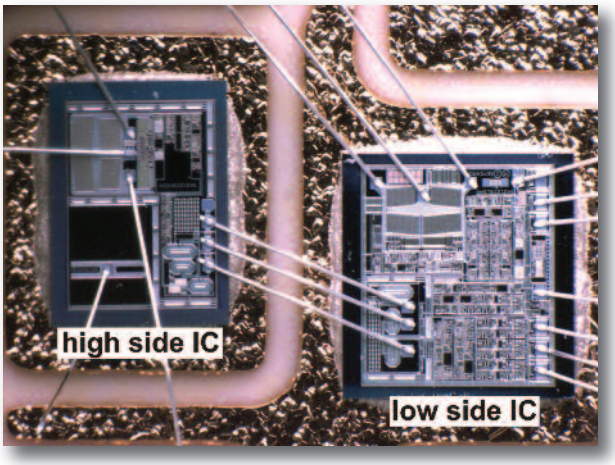

Figure 19: **Assembled two-chip 1200V, 1.4A/1.4A SOI half-bridge gate driver in a 1200V, 50A Sixpack-IPM**

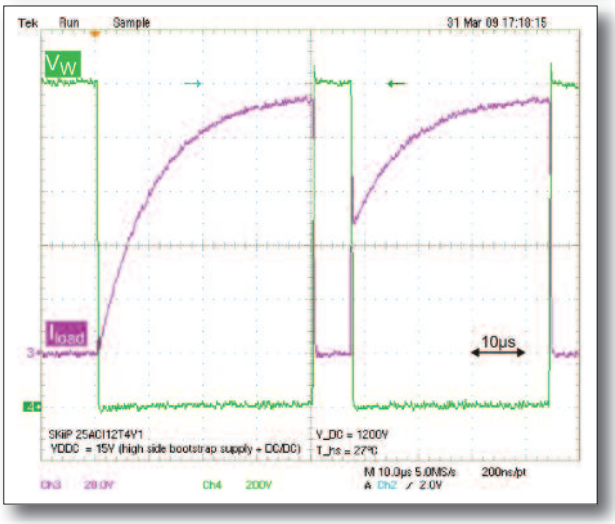

Figure 20: **Double pulse measurement (TOP-IGBT switched with load, V_{DC}=1200V, I_{load}=50A)**

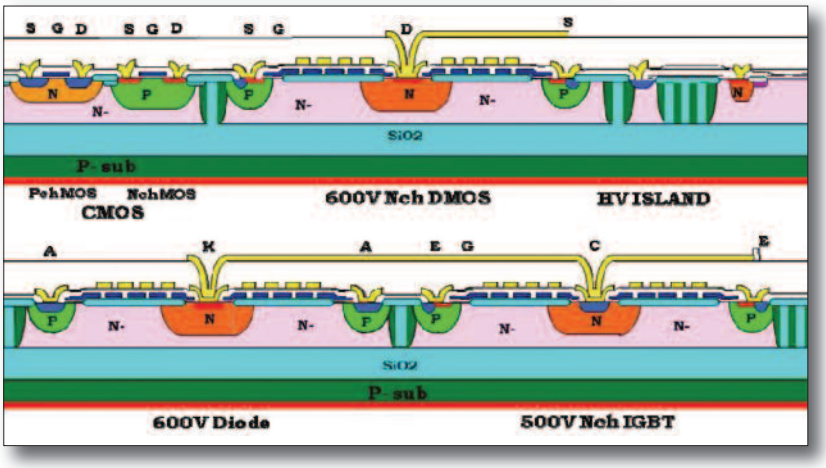

Figure 21: **Schematic cross section of fundamental device structures of a 500V SOI-CMOS technology [28]**

15V supply voltage and room temperature. In comparison to the PN-insulation driver designs in Figure 13, the insulation distances between low side and high side are very small due to the dielectric insulation. The design is extremely compact and the fully dielectric insulation of each device leads to low leakage currents and high latch-up ruggedness even at temperatures up to 200°C [6]. The capabilities of the level shifters are demonstrated experimentally in [13, 26]. The circuit remains operational for negative reference voltages down to -45V (bottom channel) and -20V (top channel) respectively. The powerful output stages of every channel can drive the gates of 600V/50A IGBTs directly in IPM configurations [13]. Each TOP channel has a separate bandgap reference and an UVLO circuit in order to monitor the high side operational voltage. This may be important if the TOP channels are powered by a bootstrap circuit.

Advanced level shifter concept for 1200V CMOS-SOI gate drivers

600V gate drive ICs based on 600V SOI-CMOS can overcome most of the disadvantages of gate drive ICs which rely on conventional junction isolation. Nevertheless, SOI technologies for the 1200V class do not currently exist. For this reason a new concept for 1200V signal transmission and high side insulation has been developed and was implemented in the half-bridge gate driver IC here presented. The transmission of the control signals to the high side is based on a new 1200V level shifter topology with cascaded 600V transistors and without further signal processing on the originating intermediate potential. A balanced voltage division across the HV transistors during switching is achieved by a balanced capacitive divider. The implemented active clamping circuitry prevents the exceeding of the maximum voltages. The limited breakdown voltage of the vertical dielectric insulation of the SOI substrate (BOX, Figure 14) requires the subdivision of the offset voltages on two physically separated dies and that, in turn, requires that all high side functions are integrated in a separate high-side IC.

Figure 18 shows the block circuit diagram and Figure 19 the chip photography of a two-chip 1200V half-bridge gate driver. Exemplarily for the performance reached, Figure 20 shows a double pulse measurement of a 1200V/50A IGBT at 1200V DC link

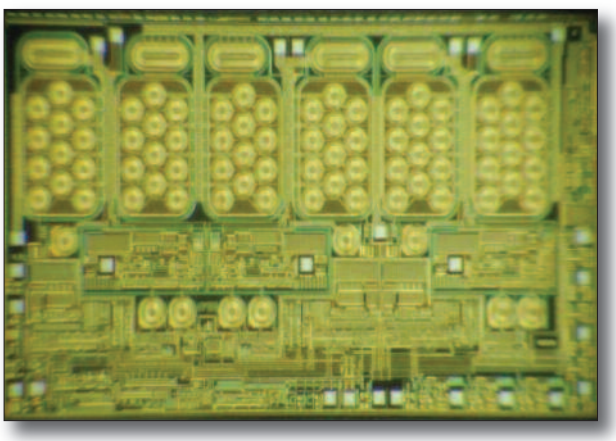

Figure 22: **Chip photograph of gate driver and 500V, 1A IGBT/FWD inverter in SOI-technology [28]**

voltage and rated current (50A) with inductive load.

Driver and inverter integration on a single chip

The fully dielectric insulation of every device in SOI-substrates enables also the integration of high-voltage bipolar devices like IGBTs and diodes together with driver and monitoring functions on the same chip. Figure 21 presents the cross section of the fundamental devices of this technology and Fig.22 the chip photograph of a 500V/1A inverter [27, 28 Mitsubishi]. For chip area and cooling reasons, such solutions are limited today on low power applications (several hundred watts).

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