Design of a High-Density Power Supply for FPGAs

Although the versatile and configurable nature of Field Programmable Gate Arrays (FPGAs) is attractive to system designers, the complex nature of design rules that govern the inner working of these devices and their outer interface protocols require extensive training, reference design evaluation, design simulation and verification. As a result, FPGA suppliers provide detailed hardware and firmware support to assist system architects with new challenges in the digital domain. However; obscure intricacies in the analog domain, specifically in the realm of delivering power and regulation voltages with DC/DC regulators for core, I/O, memory, clocks, and other rails, demand new solutions. **Alan Chern and Afshin Odabaee, Linear Technology Corp., USA**

To power each rail efficiently and in a smallest possible space requires a DC/DC regulator circuit that contains, on average, 10 components (inductor, MOSFETs, capacitors, DC/DC regulator, etc.). A 6-rail FPGA may require as many as 60 components to power it. Aside from the long list of components needed to power the FPGA, there are hidden costs of component insertion, reliability, circuit board complexity and more.

Managing multiple voltage rails

Prior generations of FPGAs required two or three power rails. Now, some of the high-end multiple-core devices require as many as seven rails; a mixture of 3.3V legacy power rails and recent lower voltages, ranging from 2.8V to 1.0V and below. Moreover, a mix of other voltage rails that are needed for devices other than FPGAs such as memory, network processors, graphics processors, digital-to-analog or analog-to-digital converters as well as op amps and RF ICs.

To ensure a "clean" start-up of a system with multiple voltage rails such that none of the rails conflict with each other requires a DC/DC regulator equipped with sequencing and tracking functions. Simply stated, each regulator must be able to track the output voltage of other regulators. The good news is that FPGAs no longer require any sequencing on their rails. However, sequential ramp-up or ramp-down of several voltages across different sections within a system are still required to prevent possible latch-offs that may occur when a voltage rail comes up too fast or too slow. In the past, tracking and sequencing of power rails was handled by a separate power management IC. Today, designers require that both the sequencing and tracking functions are embedded into the regulators, particularly when they must be located at different corners of the system.

Fast I/O nodes often demand the most power in FPGA-based applications. It's very usual to see 1.8V and 2.5V I/O voltages that create loads in tens of Amperes. The very high-end systems have requirements for 40A up to 80A I/O designs.

Due to the logistics of a board design, the DC/DC regulator must be placed at a distance from its load and requires a long PCB trace from its output to the point of regulation. At large load current levels, PCB traces introduce a voltage error equal to the value of the load current (I) multiplied by the impedance (R) of the trace. This IxR voltage error has become more problematic since the load voltages have been decreasing and load currents increasing. For example, a 200mV IxR drop for a 3.3V rail produces 6% error, whereas for a 1.2V rail it introduces a 17% error. Therefore, although the DC/DC regulator can be set to regulate a 1.2V output, the load will only see 1.0V due to IxR voltage drop.

With today's 90- and 65nanometer processes where Vt and performance of the FPGA are dependent on the precision of supply rails, an error of 17% can easily degrade performance. For example, a 100mV difference in Vt can scale the leakage current by factor of 10 or more.

Standard DC/DC regulators provide precise regulation but only if the load is very close to its output. It cannot compensate for the IxR voltage drop. The error correction must be handled with the help of a remote sense amplifier. The tightest regulation is possible with differential remote sensing of the load, which requires a precision op amp and precision resistors. An ideal regulator should provide better than ±1.5% regulation accuracy right-at-the-load even over -40°C to 85°C temperature range. This accuracy may be insignificant for a 3.3V rail where the digital ICs can tolerate ±0.5V variation, but a 90nm or 65nm device with 1.8V, 1.0V or 0.9V rails will require higher accuracy.

Once the output voltage of the regulator is set by the user, the differential remote sensing automatically adjusts the regulated voltage at the point of the load by compensating for any IxR voltage drop across the PCB trace for a wide range of load currents. As a result, the regulation is

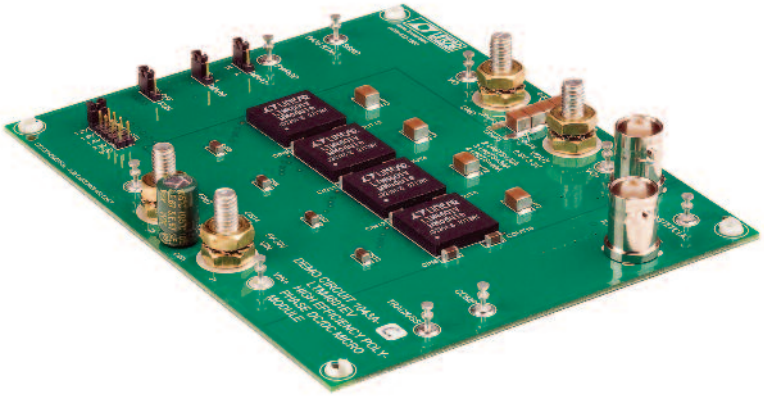

Figure 1: Four DC/DC µModule regulator systems current share to regulate 1.5V at 48A with only 2.8mm profile and 15mm x 15mm of board area

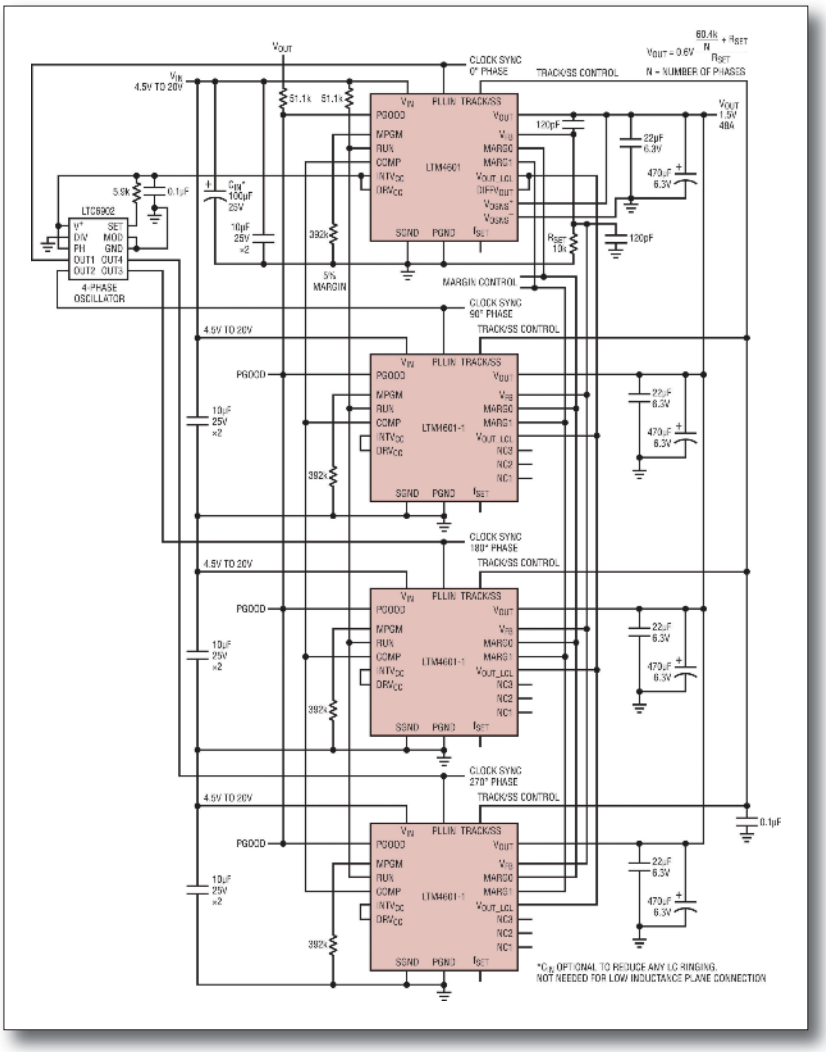

Figure 2: **Paralleling of multiple DC/DC µModule regulators systems to achieve higher output current**

very precise when the system is in standby mode, or at full speed when load current and IxR voltage drop are their peak.

Lowering voltage ripple noise and capacitor requirements

In non-portable applications, as the requirements for voltages drop and currents rise, heat dissipation and operating efficiency become more important factors in the selection of a DC/DC regulator. In portable applications, although load current per rail is less, the operating and standby efficiencies still play an important role in preserving a battery's energy and simplifying thermal management of the portable product.

A switchmode DC/DC regulator offers a higher performance solution than a linear regulator in either portable or non-portable applications, especially for high power requirements. For example, a switchmode regulator providing 1.2V at 5A from a 3.3V input supply at 90% efficiency compares to a linear regulator's 36% efficiency; furthermore, whereas the switchmode regulator dissipates 0.7W, the linear regulator dissipates 10.5W.

On the other hand, a switchmode regulator introduces switching noise and higher output ripple noise (output voltage peak-to-peak ripple) because of its inherent switching operation. Unfortunately, the lower voltage rails of new FPGAs and tighter eye-diagrams of faster I/O signals are less tolerant of power supply "noise".

To alleviate the ripple noise, more input and output capacitors can be added to the circuit to dampen peak-to-peak ripple voltage. However, dampening the switching noise is more challenging. One possible approach is to synchronize the DC/DC regulator's operating frequency to an external clock which forces the regulator to operate within a set frequency chosen to have minimum interference with other noise-sensitive parts of the system. This method is especially effective when several switchmode regulators are all synchronized to a clock frequency that is safe for the rest of the system.

These methods help with design of a less noisy switchmode point-of-load regulator; however the problem of noise can be greatly reduced if the DC/DC regulator is designed from the ground up with the proper architecture, functions and layout. Such a regulator minimizes its dependency on capacitors, filtering, and EMI (electromagnetic interference) shielding.

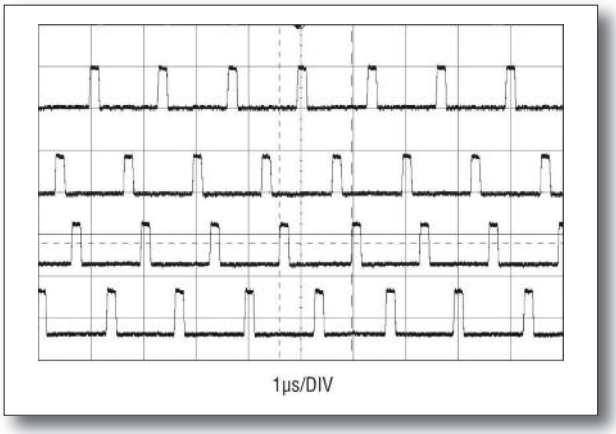

Figure 3: **By operating each DC/DC µModule regulator 90° out-of-phase, the input and output ripples are reduced, which also reduces the requirement for input and output capacitors (shown are individual µModule switching waveforms for Figure 2)**

Fine tuning voltages during system qualification and assembly

The performance of an FPGA or its supporting ICs can differ when they are assembled into a complete system versus when they are individually tested on a lab bench. Elements such as the type of solder, temperature, PCB layout, trace impedances and assembly process influence the performance of a component. For example, if the core of the FPGA is regulated at a voltage other than expected and this leads into a slower speed, the system's computational capability will be degraded. In some instances, the quality control personnel must reject a system that deviates from its expected performance.

For this reason, as engineers evaluate the performance during qualification or assembly, they need the ability to raise or lower the output voltage in small increments. This function is called margining. In the previous example, the core voltage could be increased so that the operating frequency of the FPGA reaches its desired level. The margining function can also help the system manufacturer increase the overall yield during production.

In a recent application discussion with a system designer, the requirement for his power supply was to regulate 1.5V and deliver up to 40A of current to a load that consisted of four FPGAs. This means that up to 60W of power must be delivered in a small area with lowest profile (height) possible to allow smooth flow of air for cooling. The power supply had to be surface-mountable and operate at high enough efficiency to minimize heat

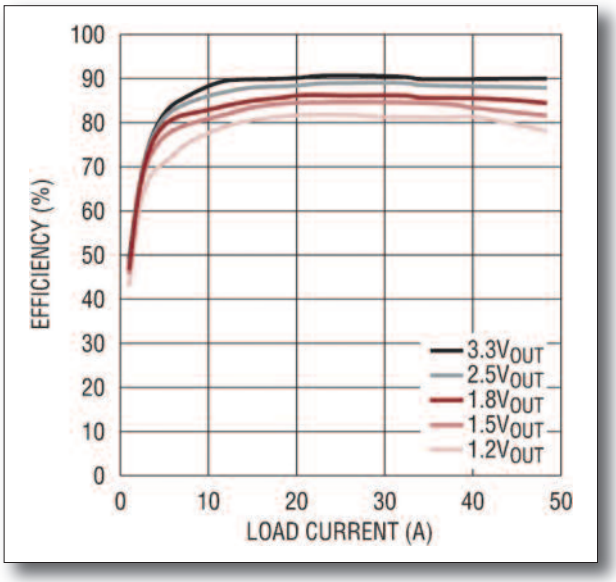

Figure 4: Efficiency of the four DC/DC µModule regulators in parallel remains high over a wide range of output voltages

dissipation. He also demanded the simplest possible solution so his time could be dedicated to the more complex tasks. Aside from precise electrical performance, this solution had to remove the heat generated during DC to DC conversion quickly so that the circuit and the ICs in its vicinity did not over heat. Such solution requires an innovative design to meet these criteria such as very low profile to allow efficient air flow and to prevent thermal shadow on surrounding ICs; high efficiency to minimize heat dissipation; current sharing capability to spread the heat evenly to eliminate hot spots and minimize or eliminate the need for heat sinks; and a complete DC/DC circuit in a surface mount package that includes the DC/DC controller, MOSFETs, inductor, capacitors and compensation circuitry for a quick and easy solution.

Innovation in DC/DC design

The innovation is a modular but surface mount approach that uses efficient DC/DC conversion, precise current sharing and low thermal impedance packaging to deliver the output power while requiring minimal cooling. Because of the low profile and power sharing among four devices, a system using this solution depends on fewer fans or slower fan speed as well as minimal or no heat sinks. These contribute to a lower cost system that consumes less power to remove heat.

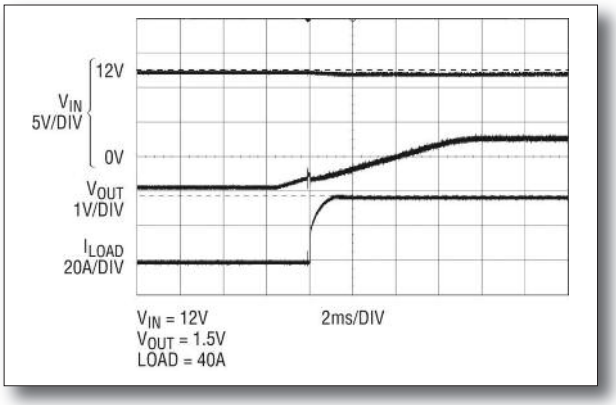

Figure 5: Controlled soft start is important in proper start-up of the FPGA or the system as a whole (soft-start current and voltage ramp for four DC/DC µModules in parallel)

Figure 1 shows a test board for such circuit. The design regulates 1.5V output while delivering 40A (up to 48A) of load current. Each "black square" is a complete DC/DC circuit and is housed in a 15mm x 15mm x 2.8mm surface mount package. With a few input and output capacitors and resistors, the design using these DC/DC µModules is as simple as shown.

The LTM4601 µModule DC/DC regulator is a high performance power module shrunk down to an IC form factor. It is a completely integrated solution, including the PWM controller, inductor, input and output capacitors, low RDS(ON) FETs, Schottky diodes and compensation circuitry. Only external bulk input and output capacitors and one resistor are needed to set the output from 0.6V to 5V. The supply can produce 12A (more if paralleled) from a wide input range of 4.5V to 20V. The pin-compatible LTM4601HV extends the input range to 28V.

A significant advantage of the LTM4601 over power-module or IC-based systems is its ability to easily scale up as loads increase. If load requirements are greater than one µModule regulator can produce, simply add more modules in parallel. The design of a parallel system involves little more than copying and pasting the layout of each 15mm _ 15mm µModule regulator. Electrical layout issues are taken care of within the µModule package, there are no external inductors, switches or other components to worry about.

Output features include output voltage tracking and margining. The switching frequency, typically 850kHz at full load, constant on time, zero latency controller delivers fast transient response to line and load changes while maintaining stability. Should frequency harmonics be a concern, an external clock can control synchronization via an on-chip phase lock loop.

Four parallel regulators provide 48A

Figure 2 shows a regulator comprising four parallel LTM4601s, which can produce a 48A (4 _12A) output. The regulators are synchronized but operate 90° out of phase with respect to each other, thereby reducing the amplitude of input and output ripple currents through cancellation (Figure 3). The attenuated ripple in turn decreases the external capacitor RMS current rating and size requirements, further reducing solution cost and board space.

Synchronization and phase shifting is implemented via the LTC6902 oscillator, which provides four clock outputs, each 90° phase shifted (for 2- or 3phase relationships, the LTC6902 can be adjusted via a resistor). By operating the regulators out-of-phase, peak input and output current is reduced by approximately 20% depending on the duty cycle (see the LTM4601 data sheet). This reduction in turn, reduces the requirement for input and output capacitors. The clock signals serve as input to the PLLIN (phase-lock loop in) pins of the four LTM4601s. The phase-lock loop of the LTM4601 comprises a phase detector and a voltage controlled oscillator, which combine to lock onto the rising edge of an external clock with a frequency range of 850kHz. The phase lock loop is turned on when a pulse of at least 400ns and 2V amplitude at the PLLIN pin is detected, though it is disabled during start-up. Figure 3 shows the switching waveforms of four LTM4601 regulators in parallel.

Only one resistor is required to set the output voltage. In a parallel setup, the value of the resistor depends on the number of LTM4601s used. This is because the effective value of the top (internal) feedback resistor changes as you parallel LTM4601s. The LTM4601's reference voltage is 0.6V and its internal top feedback resistor value is 60.4kΩ, so the relationship between V_{OUT}, the output voltage setting resistor (R_{FB}) and the number of modules (n) placed in parallel is according to equation 1:

$$V_{OUT} = 0.6V \frac{\frac{60.4k}{n} + R_{FB}}{R_{FB}}$$

n is the number of paralleled modules. **(1)**

Figure 4 illustrates the system's high efficiency over the vast output current range up to 48A. The system performs impressively with no dip in the efficiency curve for a broad range of output voltages.

Soft-Start and Current Sharing

The soft-start feature of the LTM4601 prevents large inrush currents at start-up by slowly ramping the output voltage to its nominal value. The relation of start-up time to VOUT and the soft-start capacitor (C_{SS}) according to equation 2 is:

$$V_{OUT(MARGIN)} = \frac{\%V_{OUT}}{100} \bullet V_{OUT}$$

$$t_{SOFTSTART} = 0.8 \bullet \left(0.6V - V_{OUT(MARGIN)}\right) \bullet \frac{C_{SS}}{1.5\mu A} \quad \textbf{(2)}$$

For example, a 0.1µF soft-start capacitor yields a nominal 8ms ramp (see Figure 5)

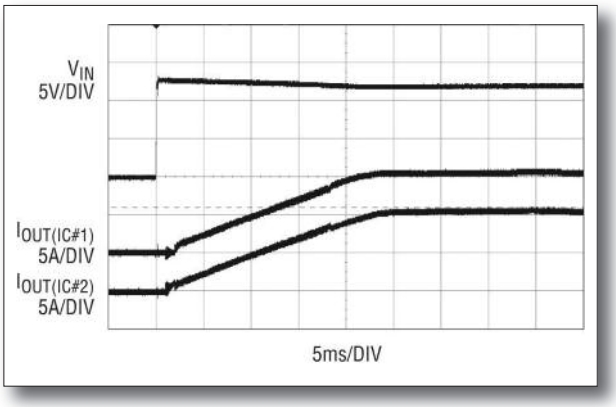

Figure 6: Each DC/DC µModule regulator starts and ends by sharing the load current evenly and balanced, a crucial feature to prevent one regulator from overheating (two parallel LTM4601s, as each rises to a nominal 10A each, 20A total)

with no margining.

Current sharing among parallel regulators is well balanced through start-up to full load. Figure 6 shows an evenly distributed output current curve for a 2-parallel LTM4601 system, as each rises to a nominal 10A each, 20A total.

In summary, the DC/DC µModule regulators are self-contained and complete systems in an IC form factor. The low profile, high efficiency and current sharing capability allow practical high power solutions for the new generation of digital systems. Thermal performance is impressive at 48A of output current with balanced current sharing and smooth uniform start-up. The ease and simplicity of this design minimizes development time while saving board space.

Thermal performance and layout

In the first portion of this article, we discussed the circuit and electrical performance of a compact and low profile 48A, 1.5V DC/DC regulator solution for a 4-FPGA design. The new approach uses four DC/DC regulators in parallel (Figure 1) to increase output current while sharing the current equally among each device. This solution relies on the accurate current sharing of these regulators to prevent hot-spots by dissipating the heat evenly over a compact surface area.

The move to shrink the size of FPGA-based systems while increasing functionality, memory storage and computational power, have prompted designers to refine the techniques used to cool the components. One simple method is to provide an efficient air flow over the components. Tall components obscure the flow over the thinner packages such FPGAs or a memory ICs. In the case of pre-fabricated DC/DC point-of-load regulators, the blockage is severe as these devices reach a height that is between 6 to 10 times the height of the FPGA and other ICs.

The thin ball grid array (BGA) packaging of the FPGAs is extremely helpful in efficient dissipation of internally generated heat from the top of the package. This benefit is diminished when a taller device such as a pre-fabricated DC/DC regulator inhibits air flow and casts a "shadow" on the device next to it.

Figure 7 is a thermal image of the board shown in Figure 1 with readings of the temperatures at specific locations. Cursors 1 to 4 show an estimation of the surface temperature on each module. Cursors 5 to 7 indicate the surface temperature of the PCB. Note the difference in temperature between the inner two regulators, cursors 1 and 2, and the outside ones, cursors 3 and 4. The LTM4601 µModule regulators placed on the outside have large planes to the left and right promoting heat sinking to cool the part down a few degrees. The inner two only have small top and bottom planes to draw heat away, thus becoming slightly warmer than the outside two.

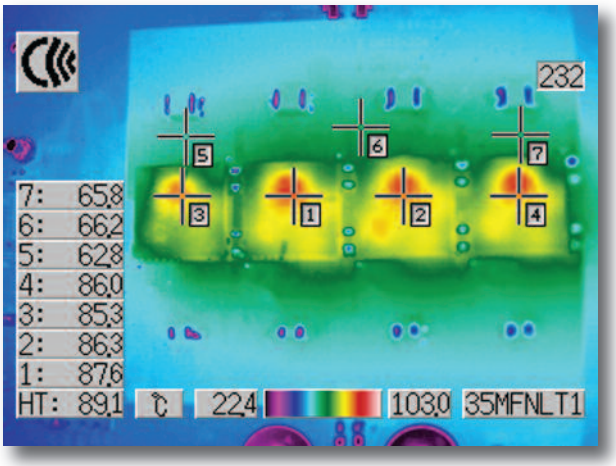

Figure 7: Thermograph of 48A, 1.5V circuit of Figure 1 shows balanced power sharing among each DC/DC µModule regulator and low temperature rise even without airflow (V_{IN}=20V to 1.5V_{OUT} at 40A)

Airflow also has a substantial effect on the thermal balance of the system. Note the difference in temperature between Figures 2 and 3. In Figure 7, a 200LFM airflow travels evenly from the bottom to the top of the demo board, causing a 20°C drop across the board compared to the no air flow case in Figure 7.

The direction of airflow is also important. In Figure 4 the airflow travels from right to left, pushing the heat from one regulator to the next, creating a stacking effect. The device on the right, the closest to the airflow source, is the coolest. The leftmost regulator has a slightly higher temperature because of spillover heat from the other regulators. Heat transfer to the PCB also changes with airflow.

Simple copy and paste layout

Further heat dissipation is possible by adding vias underneath the part. Vias provide a path to the power planes and into the PCB, which helps draw heat away. Vias should not be placed directly under the pads. Figure 6 shows the layout of the vias on the DC1043A demonstration circuit. The cross marks indicate the vias in between the LGA pads.

Layout of the parallel regulators is relatively simple, in that there are few electrical design considerations. Nevertheless, if the intent of a design is to minimize the required PCB area, thermal considerations become paramount, so the important parameters are spacing, vias, airflow and planes.

The LTM4601 regulator has a unique LGA package footprint, which allows solid attachment to the PCB while enhancing thermal heat sinking. The footprint itself simplifies layout of the power and ground planes, as shown in Figure 7. Laying out four parallel regulators is just as easy. If laid out properly, the LGA packaging and the power planes alone can provide enough heat sinking to keep the LTM4601 cool.

Conclusions

Delivering 60W of power in a compact space without efficient means to remove the heat from the power supply exacerbates the already challenging task of system heat management and cooling. The DC/DC µModule family is designed with careful attention to the layout of its internal components, package type, and electrical operation, which ease thermal management of a very dense power supply circuit. The LGA package and simple layout allow 100% surface mountable and low profile design for maximum efficiency in air flow. This new approach in power supply design takes advantage of paralleling multiple DC/DC µModule regulators and following a copy & paste approach in layout design, to provide a 60W power supply with minimum components while operating efficiently in a compact, low profile space.