Fast Switching IGBTs Create New Challenges

Fast switching power semiconductors are needed to reduce dynamic power losses. A typical system consists of dozens of power semiconductors connected in parallel that switch several thousands of Amperes at DC link voltages in the Kilovolt range. The resultant power losses are particularly challenging for application engineers, who strive to keep switching times as short as possible. But this is easier said than done. **Stefan Schuler, Development Engineer, Semikron, Nuremberg, Germany**

Application engineers call for higher switching speeds and lower dynamic losses at the same time. This is owing to the fact that for good enough approximation, a minimum PWM frequency is needed to obtain a sinusoidal output signal. Higher clock speeds reduce the harmonics which cause losses and mechanical stress in drive systems. The latest generation of fast switching IGBTs opens up all sorts of possibilities. The downside, however, is that they also bring about problems that have a particularly strong impact on the height of turn-off voltage peaks.

Efficient turn-off control

The requirement is clear: fast turn-off of power semiconductors. This, however, is not without its problems: beside greater EMC interference, dangerous voltage peaks are produced at the power semiconductor that is being turned off. If the maximum permissible blocking voltage is exceeded, the power semiconductor may be destroyed, usually resulting in a short circuit.

Figure 1 shows a half-bridge with a short circuit inductance L_B between the DC link voltage and the center AC tap. In this example, turning on transistor T_2 will cause the current i_{ZK} (u_{CE} is negligible) to rise continuously (equation 1):

$$i_{ZK} = \frac{U_{ZK}}{R_{ZK}} * \left(1 - e^{-t/\tau}\right) \quad (1)$$

$$\text{with} \quad \tau = \frac{L_{ZK} + L_B + L_{Module}}{R_{ZK}}$$

During turn-off (equation 2), i_{ZK} must drop to zero within the IGBTs turn-off time. The magnetic field stored in L_{ZK} tries to maintain the current i_{ZK} , but this is only possible if this current is taken up by the snubber capacitor C_{ZK}. As this combination is a resonant circuit type [3], a decaying sine wave superimposition, corresponding to the resonance frequency of L_{ZK}, C_{ZK} and R_{ZK} is generated:

$$f_{Res,ZK} = \frac{1}{2\pi} * \frac{1}{\sqrt{L_{ZK} C_{ZK}}} * \sqrt{1 - \frac{C_{ZK} R_{ZK}^2}{4 L_{ZK}}} \quad (2)$$

The magnetic energy stored in the inductor L_{ZK} charges the snubber to the voltage U_{ZK}+Â by t=π/2. At the same time, the former current through the short-circuit inductor L_B is commutated to diode D1. In addition, due to this current impression and the diode forward recovery (Figure 3), an additive voltage component is generated. What must also be observed are the parts of the current branch that represent an open mesh after the switching operation. Owing to the di/dt, the parasitic inductances, aggregated in L_{Module}, ensure that the voltage peak is high and also superimposed.

The voltage curve u_{CE} at transistor T_2 during turn-off (Figure 2) comprises three parts:

$$u_{CE} = U_{ZK} + u_{Module} + u_{ZK} \quad (3)$$

1) The constant DC link voltage U_{ZK}.

2) Voltage curve u_{Module} during turn-off owing to the high di/dt at L_{Module}, and a high di/dt at the freewheeling diode D_1.

3) Oscillation between the snubber and the DC link inductor, caused by their resonance and the energy stored in L_{ZK} (the parasitic inductance of the snubber and its leads L_{Sn} causes a slightly higher sine wave amplitude by t=π/2, since this is still uncharged at the time of turn-off).

The different shares should be defined on the basis of a real u_{CE} curve. Here, at the moment the turn-off process begins the u_{ZK} share is zero to begin with, since the snubber is still charged to the DC link voltage level and energy transfer of the parasitic L_{ZK} is just beginning at this moment.

The voltage caused by the parasitic module inductance, as well as the diode forward recovery time is a function of di/dt and coupled to the turn-off behavior of T_2. The only di/dt parameter that can be influenced is the switching time, since the

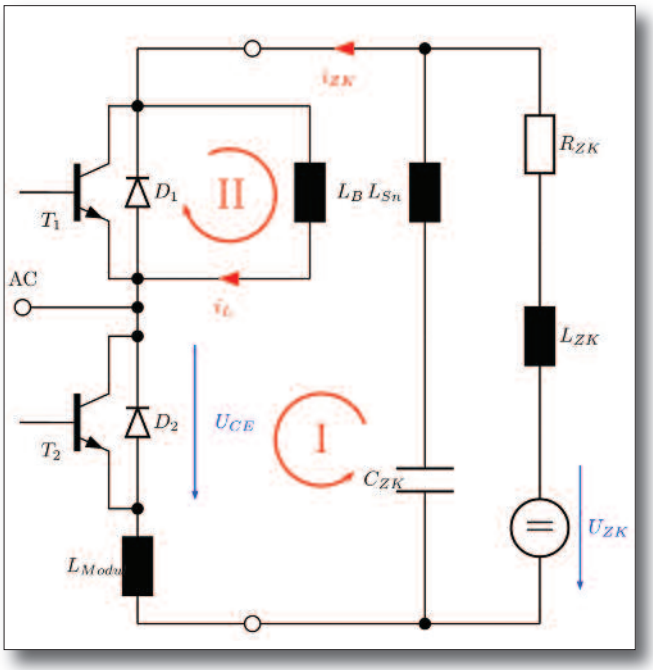

Figure 1: DC link circuit and half-bridge with short-circuit inductance L_B (simplified)

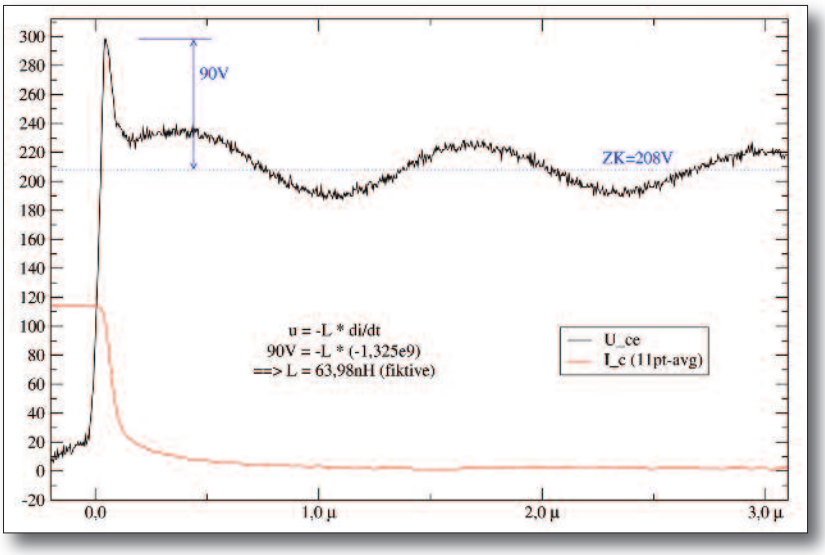

Figure 2 : Voltage u_{CE} and current iC at T_2

amount of current is defined as a load-dependent value. As soon as the turn-off process is complete, this voltage share will disappear again. Only the swing-out transient of the DC link circuit can still be seen.

Influence of the DC link circuit

In order to try to minimize the voltage peak caused by the parasitic DC link inductance, a snubber capacitor is a mounted directly at the module [4]. The voltage curve u_{ZK} during turn-off can be modeled using a sine wave with exponential decay:

$$u_{ZK} = U_{ZK} + \hat{A} * \sin(\omega_{Res} t + \varphi) * e^{-t/\tau_S} \quad (4)$$

The amplitude of the envelope Â is a function of the current provided by the DC link circuit shortly before turn-off of T_2, as well as the constant share of the DC link voltage. The magnetic energy that is stored in the parasitic DC link inductor L_{ZK} at the beginning swings periodically to the snubber C_{ZK} and back (the effective capacitance of the DC link capacitors is large enough in comparison to C_{ZK} and is therefore negligible) with decaying intensity (due to losses in R_{ZK}). At $t=\pi/2$, when the entire energy W_L is present in C_{ZK}, the amplitude of Â can be determined as follows:

$$W_C = \frac{1}{2} C * (U_{max}^2 - U_{ZK}^2)$$

$$\rightarrow U_{max} = \sqrt{\frac{2 * W_C}{C_{ZK}} + U_{ZK}^2}$$

$$\text{where } W_C = W_L = \frac{1}{2} L_{ZK} * I_{ZK}^2 \quad (5)$$

$$\rightarrow U_{max} = \sqrt{\frac{L_{ZK} * I_{max}^2}{C_{ZK}} + U_{ZK}^2}$$

$$\text{where } \hat{A} = U_{max} - U_{ZK}$$

Figure 4 shows a slightly higher amplitude of the sinus wave at $t=\pi/2$. This is owing to the (in this case neglected) influence of L_{Sn}.

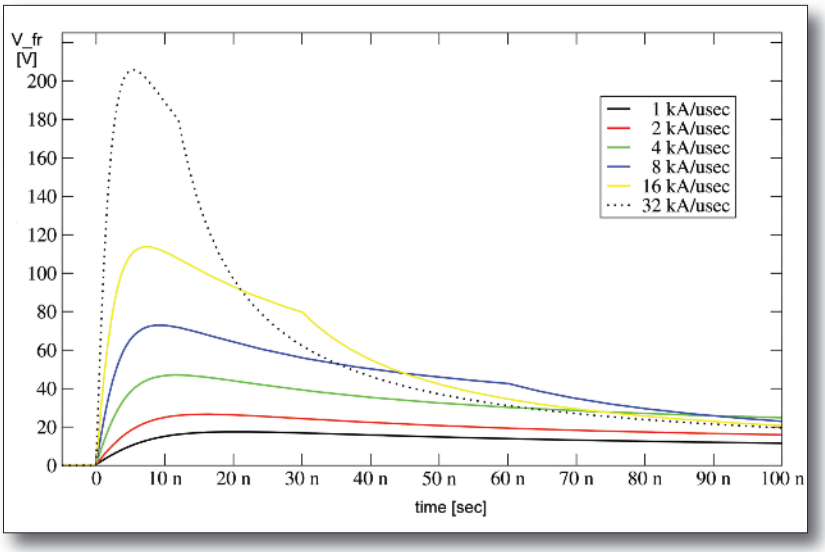

Figure 3: Forward recovery time of a power diode for various di/dt

Influence of the module

In the power module itself the conditions are different. Here, for reasons of space and operational safety (high temperatures) no snubber can be mounted. The parasitic inductances inherent in the module, e.g. busbars, DBC layout and bond wires, therefore have to be minimized by way of suitable design measure. In addition, the turn-off voltage peak can only be influenced by way of suitable switching time modulation, since this value depends on the di/dt:

$$u_{Module} = -L_{Module} * \frac{\partial i}{\partial t} + u_{D1}$$

$$\text{with } u_{D1} = f(t, i_{D1}) \quad (6)$$

The formula above contains the diode voltage uD1 as an additional component. This voltage, which is also denoted the forward recovery time voltage [1], occurs if a high current with a high di/dt is injected into the diode operating in forward direction, as is the case with freewheeling current of an inductive load. Figure 3 shows the voltage curve of a power diode (for different injected current values) which reaches its maximum after around 10..20ns and then drops to the normal forward voltage. The maximum voltage can reach as much as several hundred volts.

The curve in Figure 2 is intended to show how to define the key characteristic values. The sample curve refers to a small experimental set-up with a 200V DC link circuit, a 0.68µF snubber and a short-circuit inductance of 350µH.

DC link share analysis

To define the time constants _ for the selected DC link voltage, two meaningful measuring points are taken from the curve:

$$\tau = \frac{t_2 - t_1}{\ln(U_1 - U_{ZK}) - \ln(U_2 - U_{ZK})} \quad (7)$$

$$\tau = 3{,}872\ \mu s$$

The parasitic DC link inductance can be calculated from the defined frequency (f_R=763.5kHz) using resonance condition for a series resonant circuit (R_{ZK}, L_{ZK} and snubber C_{ZK} are in equation 8):

$$L_{ZK} = \frac{1}{\omega_{Res}^2 C_{ZK} + \frac{1}{4 R_{ZK}^2 C_{ZK}}} = 62{,}3nH \quad (8)$$

The magnetic loss resistance is calculated as follows:

$$R_{ZK} = \frac{2 L_{ZK}}{\tau} = 0{,}0326\ \Omega \quad (9)$$

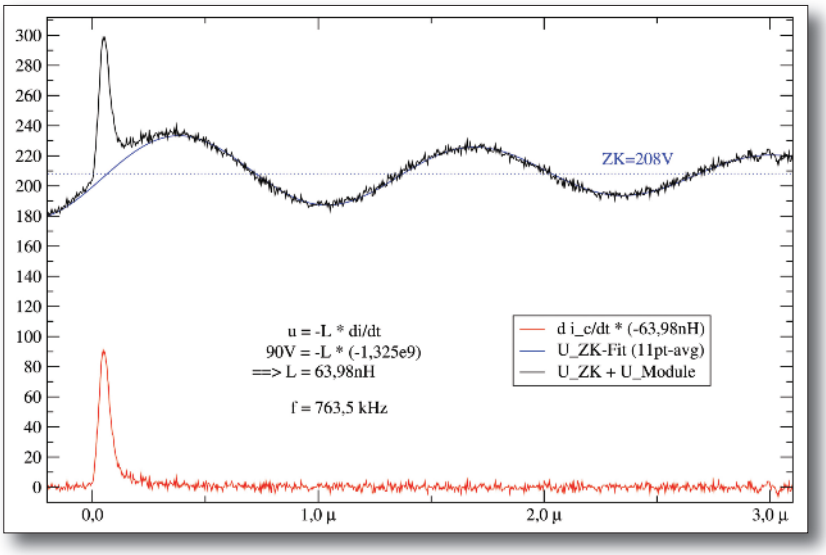

Figure 4: Calculated curves for uZK and uModul based on uCE und iC

The quality of the series resonant circuit is thus:

$$Q = \frac{\omega_0}{\Delta\omega} = \omega_0 * \frac{L_{ZK}}{R_{ZK}} = 9{,}29 \quad (10)$$

A more elegant and precise way of defining ω, τ, U_{ZK} and the amplitude Â is to use the numerical data processing and visualization tool xmgrace [2]. Here, the following formula is fit to an area between the voltage peak and after several oscillations:

y = a0 + a1 * sin(a2*g0.s1.x-a3) * exp(-(g0.s1.x-a3)/a4) (11)

The parameter results after 20 iterations for this non-linear fit are shown in Table 1. The resultant curve can be seen in Figure 4.

Analysing the module share

The module share of the over-voltage can be dealt with in two steps: first through a differentiation of the collector current curve i_C, (with e.g. xmgrace). Scaling is then performed to insert the new curve into the first u_{ce} voltage peak accordingly. Here, the (negative) scaling factor found does not correspond to the parasitic module inductance, since the influence of the diode still has to be taken into account. This is why the term fictitious module inductance $L_{Module,fict.}$ is introduced according to equation 12:

$$u_{Module} = -L_{Module} * \frac{\partial i}{\partial t} + u_D(i,t) \quad (12)$$

$$L_{Module,fikt.} = 64\,nH \quad \text{(fiktive value!)}$$

In actual fact, the voltage curve u_{Module} depends not only on the switching behaviour of the semiconductor and the parasitic module inductance, but also on the diode forward recovery time. For this reason, $L_{Module,fict}$ has to be corrected on the basis of the diode forward recovery time. The maximum share of the forward recovery time in the total voltage increase should be estimated using the maximum di/dt (Figure 3) as a basis: below 10kA/µs the forward recovery voltage $U_{fr,max}$ of a standard power diode can be approximated rather accurately using the following equation 13:

$$U_{fr,\max} = 6{,}93^{-6} * \left(\frac{\partial i}{\partial t}\right)^{0{,}71}_{\max} \quad (13)$$

For di/dt=1.3kA/µs in this example, this amounts to around 20.5V. Thus, the over-voltage drops to around 70V as a result of the inductive share, and the inductance of the test module itself drops to 49.8nH (computed value).

The superimposition of both curves (Figure 4) results in the curve calculated originally u_{ce}, which is applicable as of t=0. Now the characteristic for an alternative snubber, for example, can be easily determined.

Table 1: Fitting results

a0	voltage U_{ZK}	208,3 V
a1	amplitude Â	44,4 V
a2	resonance ω_R	4,797e6 Hz
a3	time offset	362,4e-6 s
a4	time constant τ	3,64e-6 s

Critical behavior

Together with the snubber, the DC link circuit behaves like a resonant circuit with resonance frequency $f_{Res,ZK}$. For this reason, critical states may occur. This would happen, for example, if the switching frequency were an even factor of f_0. In this case, if the quality of the resonance circuit is good enough, the energy injected into the snubber during the next switching operation is in phase. This can lead to a critical over-voltage after just a few clock pulses. Owing to the comparatively poor quality of the test module shown, this effect can be expected for switching frequencies of 30kHz and above.

Furthermore, poor interconnection of various DC link circuits and/or modules can also lead to undesired excitation, which should be checked in the individual cases.

Conclusions

The analysis of u_{ce} and i_C measurement during switch-off illustrates the interplay between parasitic DC link inductance and module inductance. This makes it easy to analyse the weak points of a given application and exploit optimization potential in simulations.

What can be seen is that pure modification of the turn-off speed merely reduces the over-voltage peaks generated by the module. The over-voltages in the DC link circuit are primarily a function of the current level and can only be reduced very slightly by decreasing the di/dt.

The formal description of the turn-off process reveals both possibilities and restrictions that apply when choosing the right switching speed, snubber and module design. A balanced combination of measures is a good way to optimize costs and improve reliability - directly on the PC, without the need for complex testing.

Literature

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[4] Application Note AN7006: IGBT Peak Voltage Measurement and Snubber Capacitors Specification