New SiC JFET Boost Performance of Solar Inverters

The article proposes a new normally-on Silicon Carbide (SiC) JFET device concept with monolithically integrated body diode. The new device combines ultra fast switching with ohmic forward characteristic and a zero reverse recovery characteristic of its body diode. It allows a significant boost of the performance of solar inverters especially in the light of new requirements such as reactive power capability and fault ride through. Best device performance is achieved with a direct driven approach, compatible with safety aspects in voltage driven topologies which is implemented in combination with a low voltage MOSFET.

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SiC devices are characterized by a number of promising properties like low switching losses, high rated voltages, high operating temperature, high radiation hardness, which were discussed earlier in [1,2]. In the laboratory the potential of SiC MOSFET and SiC JFETs [2-4] in solar inverters have been demonstrated concerning improvements of efficiency and size reduction. This article focuses on investigation of the new SiC JFET in an already existing photovoltaic (PV) inverter platform. Challenges here are the assessment of the safety risk due to normally-on characteristic combined with the proof of an increased efficiency under the restriction of EMI demands.

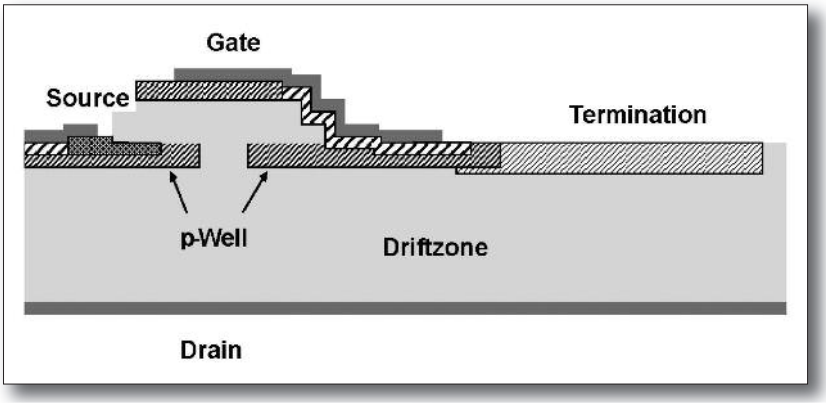

Figure 1: Cross section of the proposed SiC JFET device concept

SiC device concept with integrated body diode

We believe that a JFET structure without a channel being formed below a gate oxide as shown in Figure 1 has strategic advantages over a SiC MOSFET. First, the reliability aspect is easy to meet in a JFET structure but difficult in a MOS structure due to the still high density of extrinsic defects in the oxide. Second, the still unsatisfying subthreshold behavior of MOSFETs at high temperature does not exist in a JFET. This issue is important for the leakage current and may hurt the efficiency of the entire converter. And last but not least the structural elements of a SiC JFET are very close to the structural elements of SiC Schottky barrier diodes, which are selling in millions of pieces with proven quality in the field.

The proposed SiC JFET concept has a bipolar diode integrated between the p-well contacted by source and the backside drain contact. This diode can handle the full current rating of the SiC JFET. Beyond the obvious advantages of driving the JFET in a synchronous rectification manner the body diode is still needed for the dead time between the switching intervals of opposite devices, in an e.g. DC/AC output

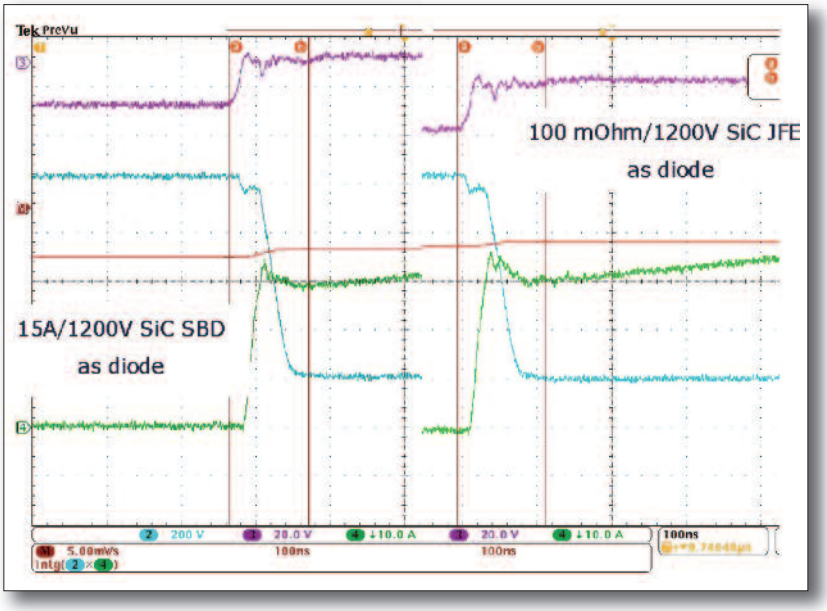

Figure 2: Comparison of hard commutation of the body diode of a 100mΩ/1200V SiC JFET (right) vs the recovery perfomance of a 1200V/15A SiC Schottky barrier diode (left) at load current I_D=30A, V_{DS}=800V, Rg=3Ω; (Channel 2: Drain voltage, Channel 3: Gate voltage, Channel 4: Current; time base 100ns/div)

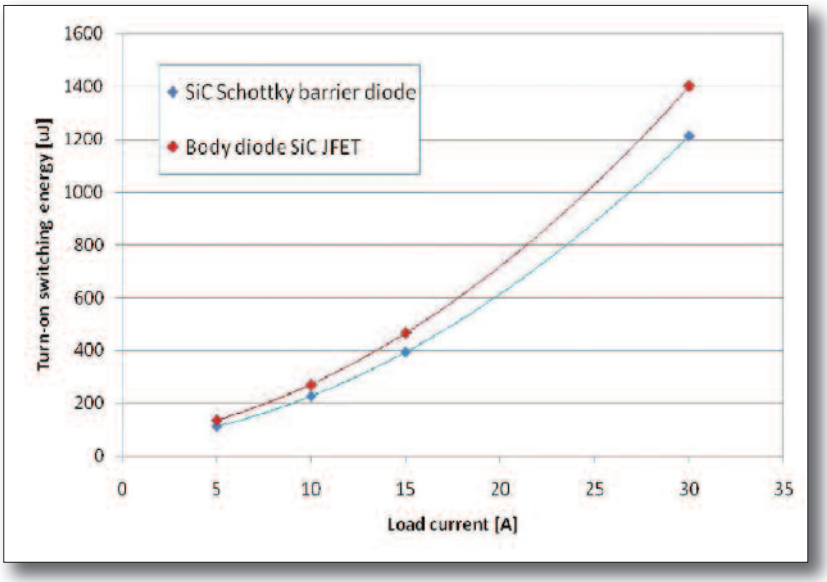

Figure 3: **Comparison of turn-on losses of the new 1200V/100mΩ SiC JFET with a 1200V/15A SiC Schottky barrier diode versus the body diode of the SiC JFET as freewheeling diode at V_{DS}=800V, T_j =75°C, R_g=3Ω**

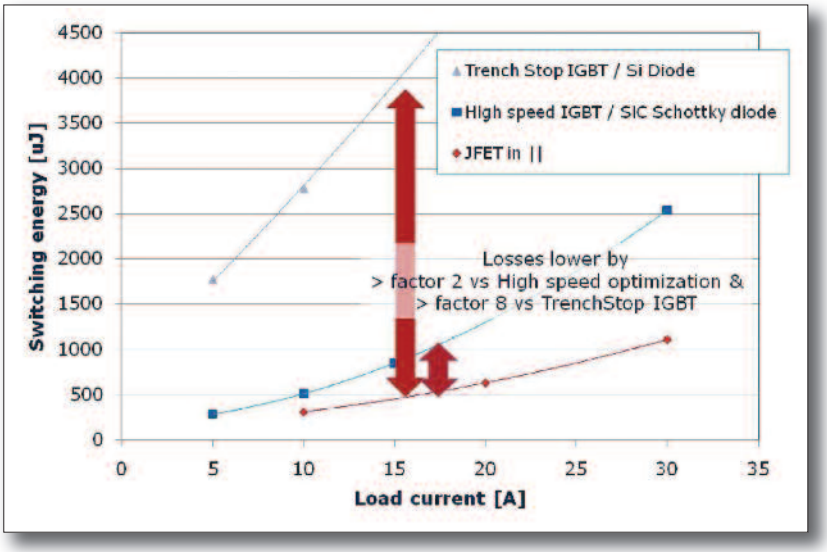

Figure 4: **Comparison of switching losses (turn-on plus turn-off) of a 1200V-50mΩ SiC JFET vs a combination of a high-speed optimized IGBT with a SiC Schottky barrier diode and a conventional 1200V IGBT combined with a fast Si pin-diode at V_{DS}=800V, T_j =75°C, R_g =3Ω**

bridge. If this diode is not present in the device structure a full current rated SiC Schottky barrier diode has to be implemented additionally for paralleling with the SiC JFET. During hard commutation the body diode of the proposed SiC JFET shows practically zero reverse recovery charge. This behavior is otherwise known only from SiC Schottky barrier diodes.

Experimental JFET results

Figure 2 compares the hard commutation of a 15A SiC Schottky barrier diode with a 100mΩ SiC JFET. Both waveforms show a very similar characteristic with the reverse recovery current flowing nearly only during the voltage rise. This is a strong indicator for a pure capacitive displacement current in both devices.

Figure 3 shows the comparison of turn-on losses in a JFET half bridge configuration versus a combination of JFET as switch and a SiC Schottky diode as freewheeling element. The switching behavior of the SiC JFET shows both very fast turn on and turn off behavior. In comparison to commercially available 1200V trench-IGBTs based on field-stop technology a reduction of both turn-on and turn-off energy of one order of magnitude has been observed. In comparison to IGBT technologies with a specific high speed optimization the switching losses are lower by a factor of 2. These ultra low switching losses are the natural key to move towards higher switching frequencies needed for the cost reduction of the magnetic components. Figure 4 shows the respective comparison.

Solar inverters and their requirements to power semiconductors

From all types of PV inverters string inverters [6] are manufactured in the highest number of pieces. Due to this market relevance a string inverter was chosen as a platform for the following investigations. String inverters are characterized by an output power range from 1kW up to about 20kW, comprising single phase or three phase topologies and showing very high efficiencies up to 98%. Typically power semiconductors with rated voltages between 600V and 1200V are being used at RMS currents between 10A and 50A. The switching frequency is in the range of 16kHz to 48kHz. Today Silicon (Si) based IGBTs and MOSFETs are commonly used in this application. However, Si diodes are already replaced step by step with SiC Shottky diodes.

For increased efficiencies suitable topologies in combination with low-loss power semiconductors are required. Over the years a number of PV specific topologies have been developed. They can be analyzed for instance by the number of phases (one, two or three phases), galvanic isolation (transformer less or with transformer), the kind of transformer (LF or HF) or which DC potential can be grounded to earth [7]. Due to the

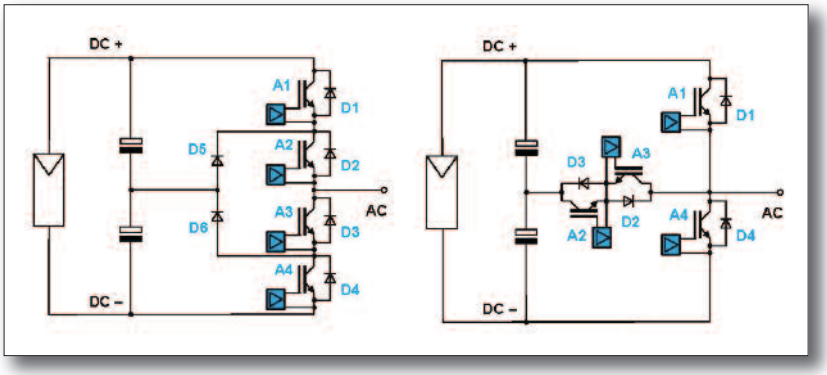

Figure 5: **Topologies for PV inverters: NPC (left) and BSNPC (right)**

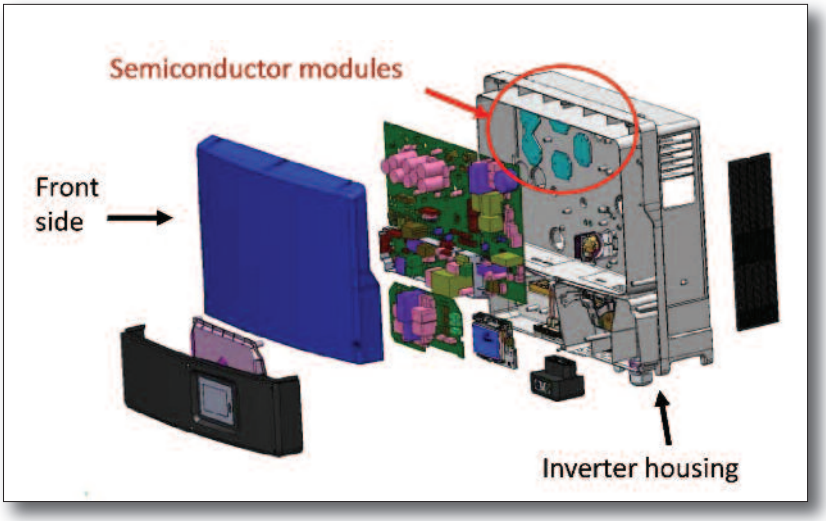

Figure 6: **Exploded view to a three phase PV inverter - Sunny TRIPOWER [6]**

improved flexibility for the PV module configuration on roof tops, for which a significant wider input voltage range is advantageously, often an inverter topology is combined with a boost or buck stage between PV generator and the inverter. Typical inverter topologies are the well known H-bridge, the PV specific H5 or HERIC bridges or multilevel arrangements like the Neutral Point Clamped (NPC) or Bipolar Switch Neutral Point Clamped (BSNPC) topology [8]. Figure 5 shows for each one leg: a NPC (left) and a BSNPC (right) connected to a PV generator followed by a divided DC link capacitor.

Both topologies use four switches A1 to A4. The high and low side switches A1 and A4 are switched at high frequency (e.g. 16kHz), the switches A2 and A3 operate at grid frequency. In the NPC one of the diodes D5 or D6 in combination with one of the switches A2 or A3 clamps the voltage to the half of the PV voltage if one of the corresponding switches A1, A4 is turned off. Which pair of diode and switch is active, depends on the polarity of the grid voltage. In every case the load current flows through two switches connected in series: A1, A2 or A3, A4.

In the BSNPC a bipolar switch arranged by A2, A3, D2 and D3 clamps the voltage to the half of the PV voltage if one of the previous two switches is turned off. In this case, most of the load current flows only through one switch A1 or A4. By using Si semiconductors for all switches an efficiency of 98.2% in maximum for the whole inverter system can be obtained. The use of SiC JFETs for A1 and A4 enhances the inverter efficiency in particular.

Construction and topology of PV inverter with new SiC JFET

For this research presentation existing three-phase PV string inverter SUNNY TRIPOWER with a maximum output power of 17kW by SMA acts as a platform.

Figure 6 shows an exploded drawing of the inverter assembly. The heart of the device is an integrated housing made of aluminum die cast. This housing has an inner separating wall which separates the inverter in a front and a back compartment. On the front side a compartment for sensitive electronic components like semiconductors is situated. All modules are thermally coupled to the separation wall of the housing. Mounting places are marked. On its backside cooling fins are located so that the housing acts as the cooling system. Generally on the backside heat generating components such as embedded inductive component are assembled for cooling.

The inverter uses a two-stage topology consisting of two boosters for the connection of two strings of PV modules and a three-phase BSNPC topology. All semiconductors are integrated in five Easy1b modules from Infineon Technologies: two booster modules and three inverter modules. The two booster modules include semiconductors for the booster stages. Each of the inverter modules is configured as one leg of the BSNPC topology. The configuration of semiconductors and the semiconductor module is represented in Figure 7.

High and low side transistors A1, A4 (see Figure 5) are replaced by normally-on SiC JFETs. To prevent a short circuit during start up of the system a Cascode formed by a direct driven JFET and a serial low voltage MODFET was introduced [9]. Here a low voltage MOSFET is arranged in series to one JFET. Both switches are driven

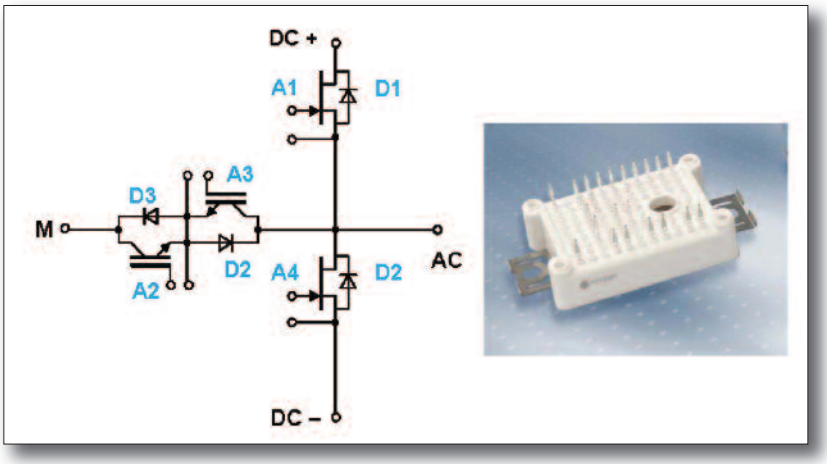

Figure 7: **Semiconductor inverter module Easy1b and its PV specific equipment**

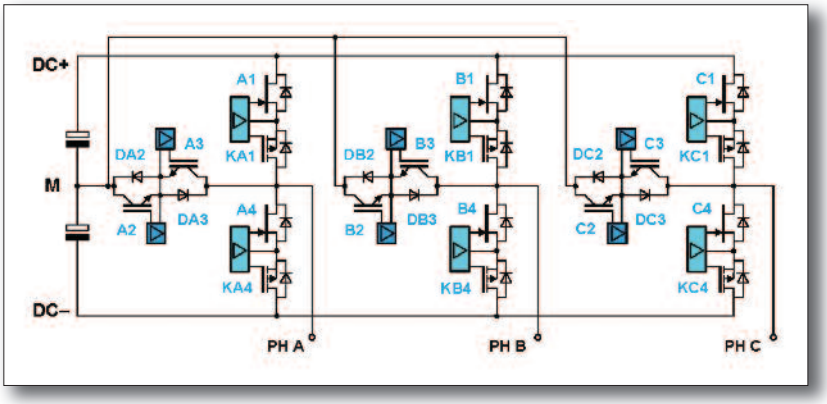

Figure 8: **Three-phase BSNPC with direct driven SiC JFETs at high and low side positions in a Cascode configuration**

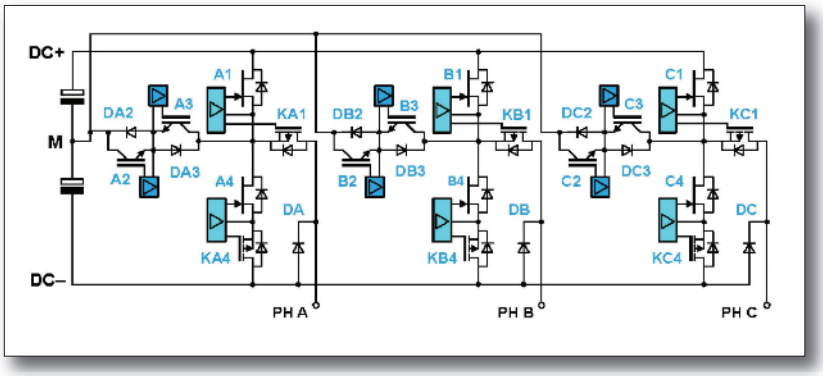

Figure 9: Three-phase BSNPC with direct driven SiC JFETs at high and low side positions in a modified Cascode configuration

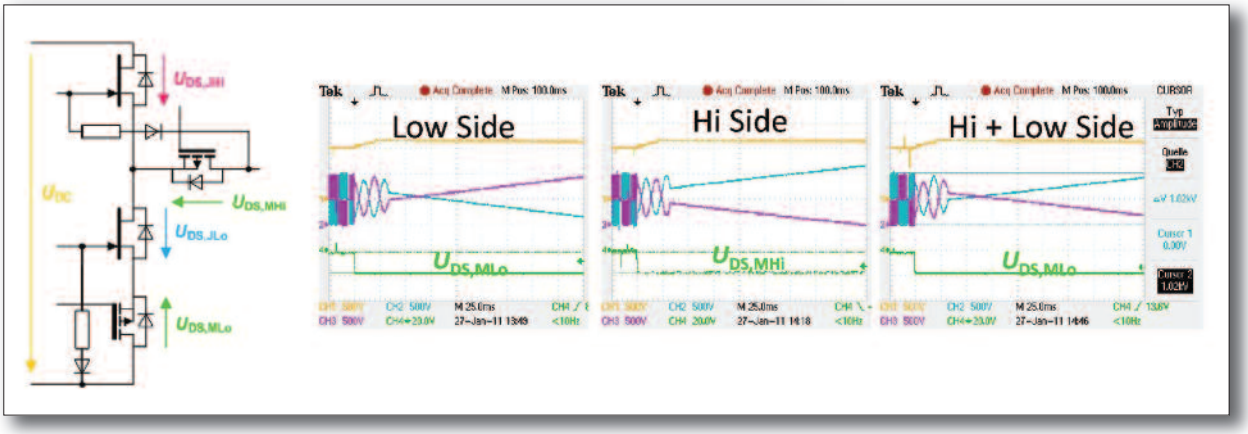

Figure 10: Results of shutdown tests induced by interruption of auxiliary driver supply per one phase at DC link voltage U_{DC}=950V and Output power P_{out}=17kW (Channel1: DC link voltage U_{DC}, Channel 2: $U_{DS,JHi}$ of high side JFET, Channel 3: $U_{DS,JLo}$ of low side JFET, Channel 4: MOSFET voltage $U_{DS,MLo}$ or $U_{DS,MHi}$; time base 25ms/div)

directly and independently. P-channel MOSFETs are advantageously because then the two driver channels for JFET and MOSFET use the same reference potential and can be operated with only one auxiliary supply voltage.

The complete three-phase BSNPC topology using direct driven SiC JFETs on high and low side in a Cascode configuration is depicted in Figure 8. By using semiconductor modules as shown in Figure 7 the low voltage MOSFETs are located outside of the module. This requires a modification of the arrangement shown above into the configuration depicted in Figure 9. Additionally diodes DA, DB and DC are necessary. They act as freewheeling elements in case of shutdown of the Cascode MOSFET. This topology has the advantage, that the Cascode MOSFETs KA1, KB1, KC1 are not a part of the commutation circuits. This results in lower losses of the systems. For the additional diodes DA, DB and DC simple and cheap rectification diodes can be used, what mitigates the disadvantage of their existence. Combining all MOSFET of the low sides to only one device is an interesting option to reduce the number of semiconductor devices.

Results of shutdown tests are depicted in Figure10. During shutdown DC voltage and voltages across all switches have been measured. This is illustrated on the left side of Figure10, where one leg of the investigated topology is represented. The resistor and the diode pull the gate of the JFET to the lowest potential. The waveforms show the results of several shutdown tests. The supply voltage of the driver of the low side JFET (A4), of the high side JFET (A1) and of both JFET (A1 and A4) has been interrupted in these cases. Shutdowns at several combinations of DC link voltage and output power have been investigated, results are represented at a DC link voltage of 950V and 17kW output power.

As long as the JFETs are actively switching the Cascode MOSFET is in an always-on conductive mode. With the interruption of the supply the voltage across the low voltage MOSFET changes.

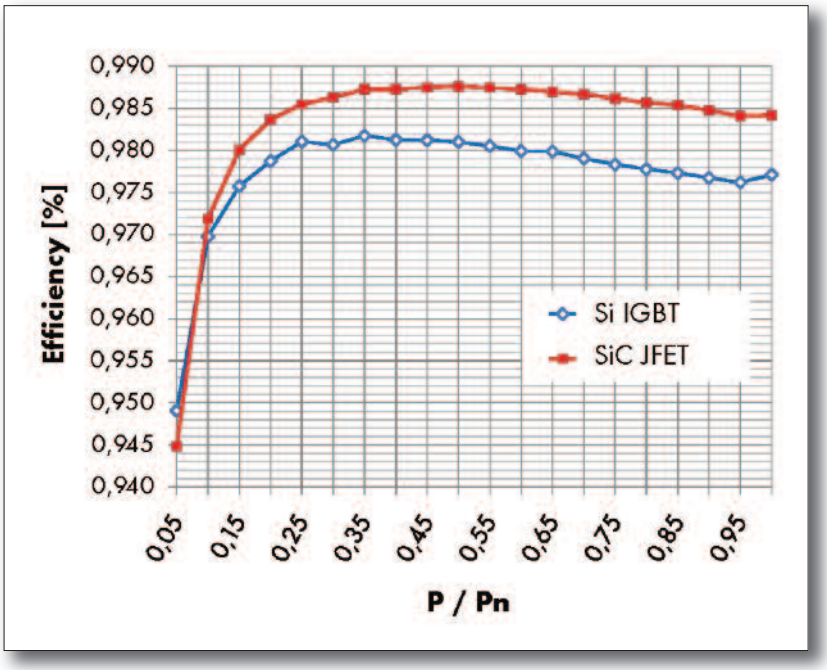

Figure 11: Measured system efficiencies at optimum operation point

The MOSFET turns-off immediately, which puts the entire Cascode formed by the JFET and the low voltage MOSFET into the off-state. Later on after one and a half period of the AC voltage the relay between inverter and grid opens and realizes the disconnection from the grid. After opening the relay the voltage over the JFETs rises slowly up to their stationary value. With these pictures the safe operation of the direct driven Cascode in the application is demonstrated.

Experimental inverter results

Figure 11 shows efficiencies of the inverter system at optimum operation point over several output power levels. A significant difference between both solutions can be seen. The standard inverter based on Si switches achieves a maximum efficiency of 98.2%. For the inverter equipped with the new SiC JFETs 98.8% system efficiencies can be obtained.

EMI and efficiency tests have been done for several current rise rates. In principle a shorter switching time and hence a further increase of efficiency is possible. But this is in contradiction with EMI demands. An improvement of the EMI behavior is expected with an optimization of the PCB and semiconductor module layout, which will allow further increase the efficiency.

Conclusions

This article presents a new normally-on SiC JFET with monolithically integrated body diode. The device concept achieves ohmic characteristics in forward and reverse direction (when driven in a "synchronous rectification" mode) and extremely low switching losses. It shows a nearly zero reverse recovery performance of its monolithically body diode.

Safety requirements can be fulfilled by combining the direct driven normally-on SiC JFET with a low-voltage MOSFET in a Cascode arrangement. This pair of switches operates like one normally-off switch in critical situations. Topology and functionality tests have been presented in this paper. The influence of the Cascode MOSFETs on the system efficiency is extremely low.

SiC JFETs reduce static and dynamic losses significantly in comparison to Si-based switches resulting in a clear improvement of the PV inverter efficiency. Experimental results demonstrating this have been presented and discussed showing that efficiencies as high as of 98.8% could be reached. All required EMI tests have been passed. Further improvements are expected by an optimization of PCB and module layout. The new SiC JFETs are suitable for an improvement of efficiency or output power of PV inverters. Even an increasing of switching frequency can be expected at the same level of losses compared to the existing solution, based on Si transistors. This leads to a reduced size of inductive components. Smaller inductive components can make a significant contribution to cost reduction of PV systems.

The new SiC JFET allows full usage of the integrated body diode. It saves anti-parallel diodes in the topology, which are otherwise required in the case of reactive power. Due to the relatively high on-state voltage of the body diodes the turn-on of the channel in parallel to the diode in a synchronous rectification mode is strongly recommended. The new SiC JFET is hence an ideal choice in both forward and reverse operation, as outlined at PCIM 2011 [10].

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