Digital Control Brings More Efficiency to DC/DC Converters

As energy prices rise and "green" initiatives gain success, private companies and government regulators are ratcheting up the demands on power-supply manufacturers. The demands on server power supplies by the European Commission, which is the executive body of the European Union (EU), and the United States Environmental Protection Agency (EPA), have grown to cover efficiency across varying load levels, as well as standby power draw. Server-farm operators have implemented similar demands on their power-supply manufacturers. The Phase-Shifted Full-Bridge (PSFB) topology is one type of DC/DC converter that has the potential to meet the efficiency demands on future power supplies. A DSC's flexibility makes the temperamental PSFB topology easier to manage, and also enables advanced techniques that further improve the efficiency of the PSFB topology. **Charlie Ice, Product Marketing Manager, and Ramesh Kankanala, Principal Applications Engineer, Microchip Technology, Chandler, USA**

With these stringent regulations, and more on the horizon, power-supply manufacturers are turning to digital control. In a fully-digital solution, a fully-programmable Digital Signal Controller (DSC) directly generates the PWM signals that control the power stage. At the same time, the controller handles system-management tasks, such as data logging, communication and fault reporting. This enables the power-supply designer to program advanced control methods into the DSC, which would be difficult if not impossible in an analog design. This feature also gives the designer the flexibility to implement any data logging and communication standards needed by the end customer.

Necessity for the phase-shifted full-bridge topology

Let us discuss the simple full-bridge topology, necessary for high-frequency operations, and then move to efficiency-improvement strategies.

As shown in Figure 1, a Full-Bridge Converter is configured using four switches - Q1, Q2, Q3 and Q4. The diagonal switches Q1, Q4 and Q2, Q3 are switched ON simultaneously, which provides a full input voltage (VIN) across the primary winding of the transformer. During each half cycle of the converter, the diagonal switches Q1, Q4 and Q2, Q3 are turned ON, and the polarity of the transformer reverses in each half cycle. In the Full-Bridge Converter, at a given power compared to the Half-Bridge Converter, the switch current and primary current will be half. This reduction in current makes the Full-Bridge Converter suitable for high power levels. However, the diagonal switches are hard switched, resulting in high turn ON and OFF switching losses.

In the past, when sophisticated controllers were not available, power-supply engineers were forced to use less efficient hard-switched power-conversion methods. These losses increase with frequency and, thus, limit the frequency of operation, limiting the power supply's ability to efficiently deliver power.

Soft-switched full-bridge topology

Using today's DSCs, designers now consider higher operating frequencies to reduce the volume of magnetics and filter capacitors in power supplies. These higher frequencies, in turn, result in higher switching losses in hard-switched power converters, such as the traditional Full-Bridge Converter. A better alternative is to choose relatively complicated soft-switching methods to reduce switching losses and deliver higher power density.

A Soft-switched full-bridge (PSFB) converter is a soft-switched topology

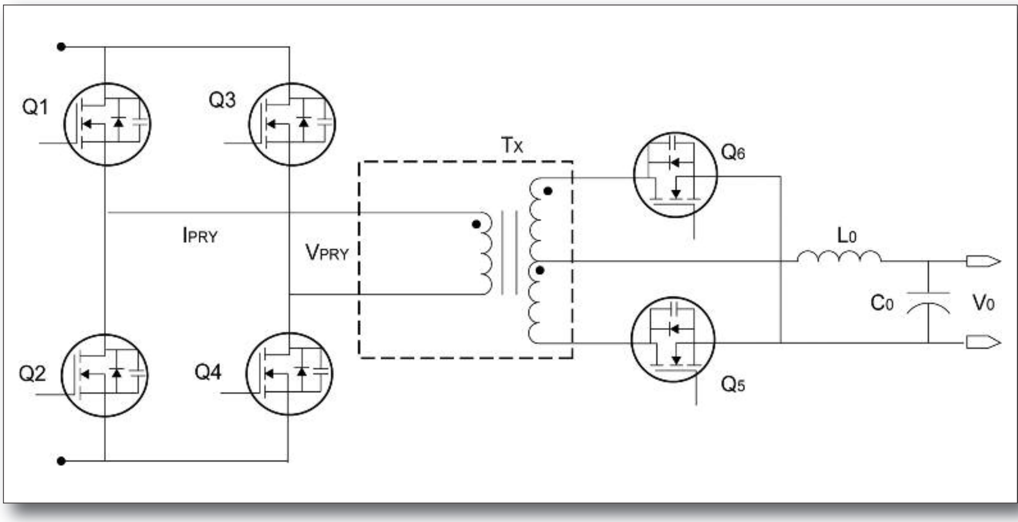

Figure 1: Full-Bridge Converter

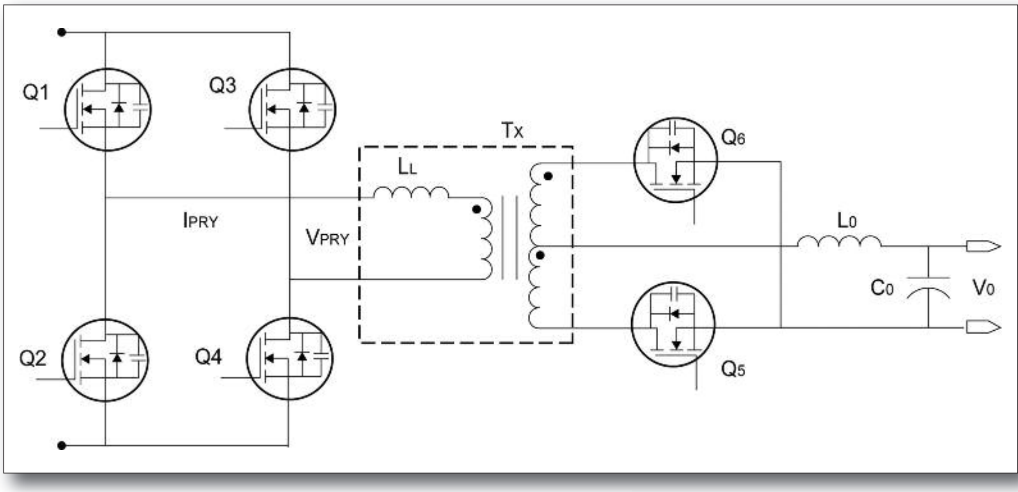

Figure 2: Phase-Shifted Full-Bridge Converter

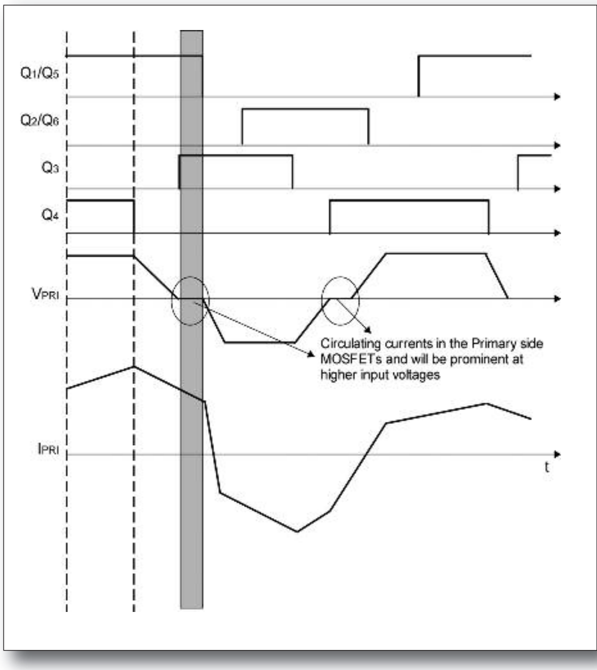

Figure 3: Traditional Configuration of Synchronous MOSFET Gate Drives

that uses parasitics such as output capacitance of switching devices (MOSFET, IGBT) and leakage inductance of transformers to obtain the resonant transition (Figure 2). This resonance will place zero voltage across the switching devices while they turn ON, and therefore eliminate their turn ON switching losses.

PSFB converters have been used in telecom and server applications where density and efficiency of the converter is paramount. The normal operation of PSFB converters is explained in many papers and we will start from that point to showcase how a DSC can further improve the performance.

Phase-shifted full-bridge converter with conventional synchronous MOSFET gate drives

Most DC/DC converters are designed with isolation transformers for user safety, and to comply with rules imposed by regulatory bodies. Higher-rated power supplies are designed with the PSFB topology in the primary and full-wave synchronous rectifier in the secondary to achieve high efficiency.

In PSFB converters, with a traditionally controlled synchronous MOSFET configuration, the MOSFETs Q1, Q3 or Q2, Q4 should be ON (Figure 3). At that time, there is no power transfer from the primary to the secondary and the MOSFET Q5 is still ON.

Due to the presence of an inductor (L_o) in the secondary side of the converter, the energy in the output inductor is circulating through the MOSFET Q5 and the transformer (T_x) secondary coil. The current continues to flow through the transformer secondary coils, either through the MOSFET's channel, or through the MOSFET's body diodes. Due to reflection of current from the secondary to the primary, circulating current exists during zero states (non-energy transfer states from the primary to the secondary) in the primary, which causes losses in the converter. These circulating current losses are predominant at higher voltages than the rated nominal input voltages. And also to avoid cross conduction, there is an intentional dead band between Q5 and Q6 MOSFET gate drives. During this period, neither of the synchronous MOSFETs conducts. Therefore, the current takes the path of the MOSFET body diode. These MOSFET body diodes have a high forward drop compared to the $R_{ds(ON)}$ of the MOSFET, which translates to (V_F * I) >> (I^2_{rms}* $R_{ds(on)}$).

The higher losses encountered in conventional synchronous gate drives can be prevented by using the overlapping gate-drive signals, as described in the next section.

Overlapping of synchronous MOSFET gate-drive signals

Losses that occur during the zero state of the transformer's primary side can be avoided by overlapping the synchronous MOSFETs' PWM gate drive. This increases the power supplies efficiency in three ways: First, in a center-tapped full-wave rectifier, overlapping the synchronous MOSFETs' results in cancellation of flux in the transformer secondary center tapped coils, effectively no flux linking from secondary to the primary. Second, instead of one synchronous MOSFET and one coil of the center-tapped transformer, two synchronous MOSFETs and two transformer center tapped coils conduct simultaneously. Therefore, the secondary current will have only half the effective resistance, and losses are reduced by half compared to when only one synchronous MOSFET is ON (Figure 4).

Finally, in the conventional switching methodology, intentional dead time may be around 10% of the switching and during this dead time, high secondary current flows through the high forward-drop body diode of the MOSFET. By configuring the overlap of the

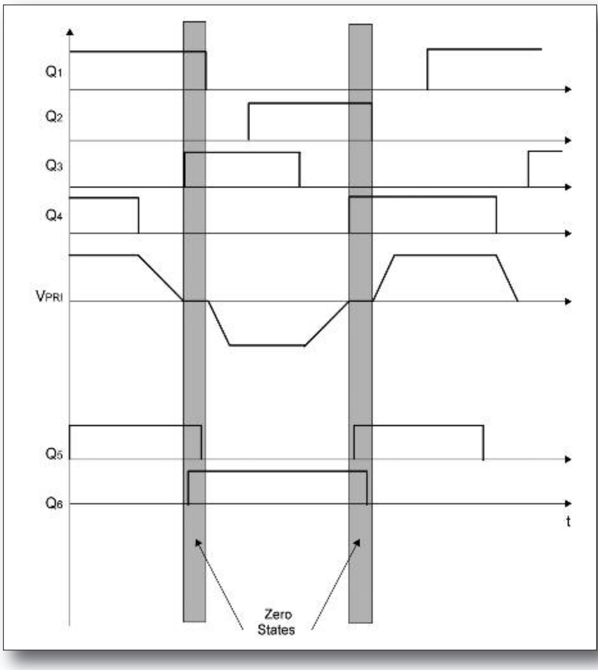

Figure 4: Overlapping Synchronous MOSFET Gate Drivers for Improved Efficiency

synchronous MOSFET's PWM gate drive, high secondary currents flow through MOSFET channel. In this instance, there will be only $R_{ds(ON)}$ losses, which are much less than the losses incurred by the MOSFET body diodes in the dead time. For a system with a telecom input (36 to 76 VDC), the DC/DC converter's efficiency improves anywhere from 3-4% by overlapping the synchronous MOSFET gate drive.

Implementing these techniques require a flexible power supply controller with completely independent PWM outputs. DSCs such as the dsPIC® DSC, offer the flexibility and PWM peripherals to easily implement this and other efficiency improving techniques.

Conclusion

The PSFB topology has the potential to achieve the efficiencies needed for modern power supplies. Digital control gives designers the ability to both control the PSFB topology very precisely and implement advanced control techniques, such as overlapping the synchronous MOSFETs. New topologies, new techniques, and new ideas are catapulting power supplies into the 21st century. Digital controllers such as the dsPIC DSC from Microchip are ready to take power supplies into the future.

Literature

Microchip Application Note AN1335, "Phase-Shifted Full-Bridge (PSFB) Quarter Brick DC/DC Converter Reference Design Using a dsPIC® DSC."