Silicon Carbide BJT's in Boost Applications

Efficiency is becoming more and more important as well as size and cost. In boost DC/DC converters, typically used in PV inverters and PFC circuits, increased switching frequency makes a big impact on both size and cost. Silicon Carbide (SiC) bipolar junction transistors (BJT's) offer low-loss high speed switching combined with low conduction losses enabling higher switching frequency and maintaining high efficiency. SiC BJT's combine the best properties from Silicon unipolar and Bipolar technologies in a normally-off device. The design and performance of a 1kW boost circuit based on the SiC BJT is presented in this article.

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SiC BJTs using a vertical NPN structure were fabricated and assembled in an industrial standard TO-247 package. This type of transistor combines very low conduction losses with fast and low loss switching behavior [1]. The high critical field strength of SiC gives the possibility to have low saturation voltages without driving the transistor into hard saturation. Since there is no channel region in a BJT the $V_{CE(SAT)}$ is determined mainly by the collector series resistance.

It is not necessary to drive the SiC BJT into hard saturation which gives them excellent switching properties. There is no current tailing and a minimal storage delay (5 ns) at turn-off. The SiC BJT is also a very robust device with a wide RBSOA, good short circuit capability [2] and can operate at high temperatures [3]. SiC BJT's have suffered from bipolar degradation, making the gain decrease significantly over time [4]. The BJT's discussed do not have this problem (Figure 1).

Base drive circuit and the challenges

A SiC bipolar transistor is a current driven device. The driver must deliver enough current to turn the device on and off, plus load and unload the Miller charges quickly enough. Nevertheless the losses in the drive circuit should be limited. One target for this development was to decrease the driver losses as much as possible, without impacting the switching speed.

To have enough safety margin the base current should be oversized by a factor of 1.5 compared with the calculated base current (I_b = beta • I_c). To simplify the base drive circuit using a constant base current is recommended.

We developed a driver board with an adjustable dual supply, V_{cc} and V_{ee}, a high speed opto-isolator and an additional capacitor C10 in parallel to the base resistor R2 to boost the base current for a short moment, just during turn-on and turn-off of the BJT.

When the BJT is turned on, V_{be} is equal to 2.9 V with a slightly negative temperature coefficient. The positive supply voltage of the driver is divided into a small voltage drop in the driver, the V_{be} and the voltage drop across the base resistance R2. The capacitor C10 in parallel to R2 will be charged in this moment to the voltage across R2. When the device is turned off, this capacitance provides a short increase in the drive current to increase the switching speed of the BJT.

Two big obstacles for fast switching are the parasitic inductances of the package and the PCB. To reduce the influence of these parasitics the supply voltage for the driver could be increased, but this would lead to significant higher drive losses during turn-on. The alternative would be two separate drivers, one for fast switching, the other for supplying the base current. As this would make the circuit expensive and complicated, we decided to use the additional boost capacitor C10 in parallel to the base resistance R2. In any case, the negative supply for the driver cannot be avoided for fast switching.

Double pulse test setup

The base drive circuit has been optimized with the double pulse test setup. Turn-on and turn-off waveforms can be analyzed separately without the need for a full thermal design.

The test set up is optimized, the inductor is a 1 mH coreless choke and the capacitors have been placed in shortest

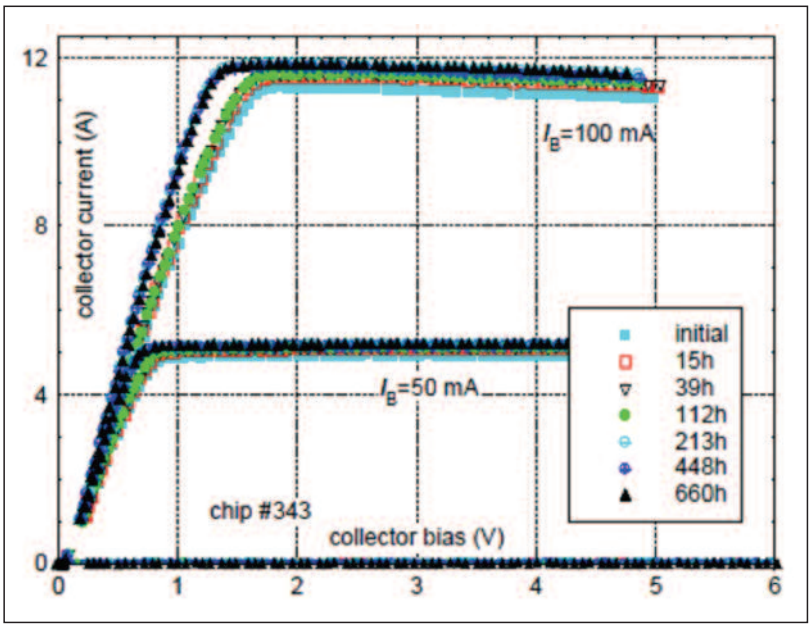


Figure 1: Gain (hFE) and $V_{CE(SAT)}$ before and after 660 hour DC stress test (open collector, I_{BE}=0.25 A)

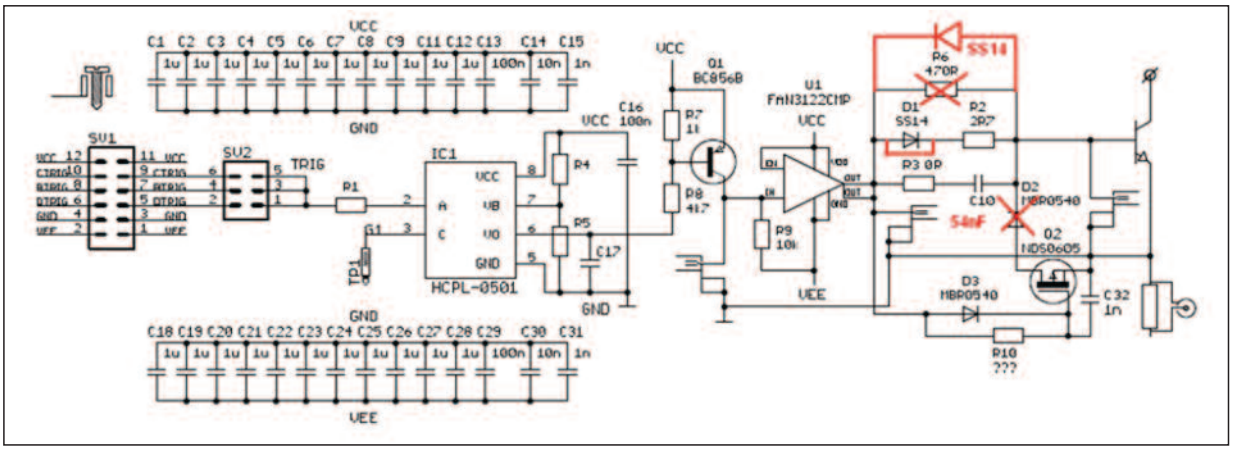


Figure 2: Base drive circuit for SiC BJT

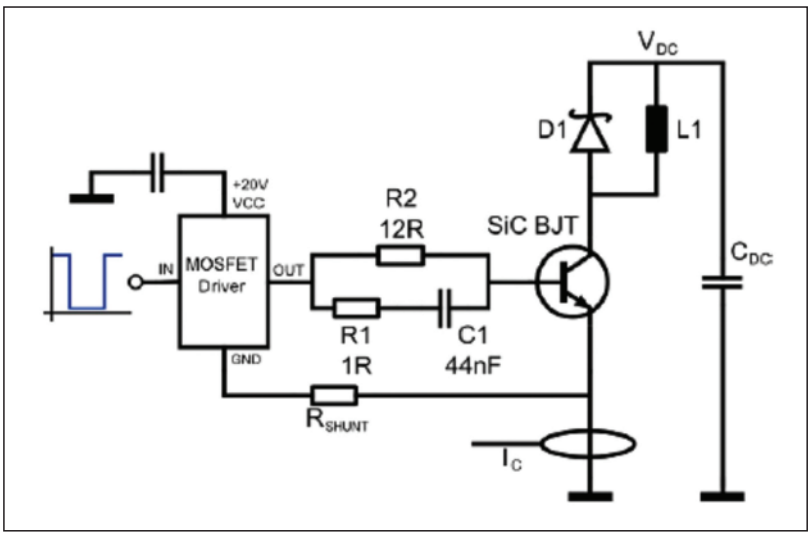


Figure 3: Double pulse test setup

distance to the semiconductors in order to reduce the current loop inductance.

By changing the position of the diode, the same test setup can be used for the boost function. In this case the diode will charge an additional bank of capacitors connected to the load. That means that at least the primary side circuit and the drive circuit are identical and the test results can be compared easily.

Some differences from SiC BJTs to conventional switches are characterized by the turn-on and turn-off waveforms shown in Figure 4 and 5. The drive circuit is supplied by V_{cc} = 7V and V_{ee} = -3V. The red curve M1 shows V_{be}, which is measured by the differential signal between base and emitter lead. When turning the BJT on, the signal starts to rise from -3V to +3V by charging C_{be}. At the threshold of 3 V the current starts to commutate from the diode to the BJT at a di/dt of around 1000 A/µs.

The relatively big C_{be} capacitance gives the BJT stability, as well at slightly noisy gate signal. The first drop of V_{ce} is caused by the induced voltage across the loop inductor ($V_{ind} = -L_{loop} \cdot di/dt$).

As soon as the diode current drops to zero, the V_{ce} of the BJT starts to drop. A strong base driver is now needed to discharge the Miller capacitance of the BJT.

During turn-off, both the current and voltage waveform start to change at the same time. In the first nanoseconds the base current must charge the Miller capacitance. As soon as V_{ce} reaches the bus voltage, the change in the di/dt of the current drop is visible. Due to the ideal features of the SiC material the influence of the removal of the stored carrier charge is negligible, this causes just a delay of about 5 ns in the begin of the turn-off procedure.

It is often said that TO247 packages cannot handle the high switching speeds of the SiC devices. In order to double check we performed some tests. As the driver board is opto-isolated, the connection to the BJT is rather flexible. The GND-trace of the driver is connected to two different points of the emitter lead of the BJT.

The most significant difference is visible at highest currents and at maximum di/dt. During turn-on at a di/dt of 1000 A/µs,

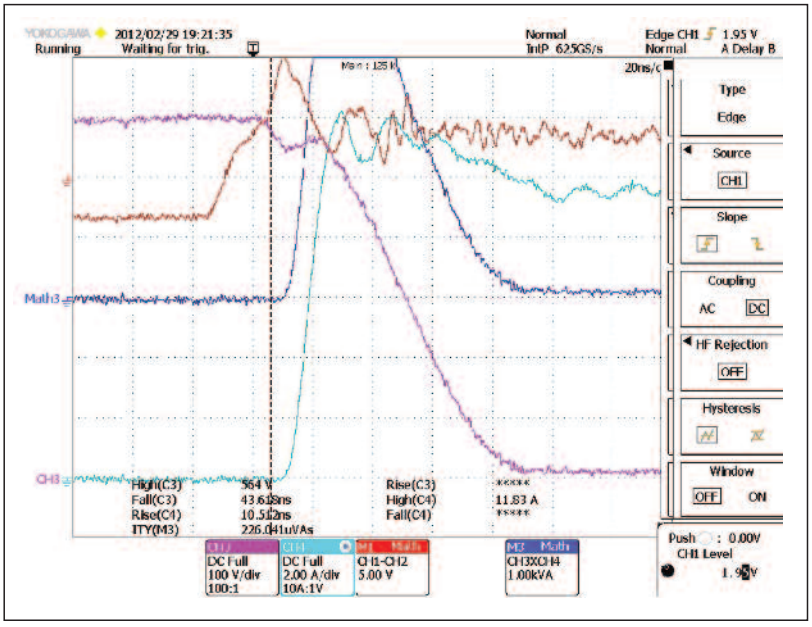
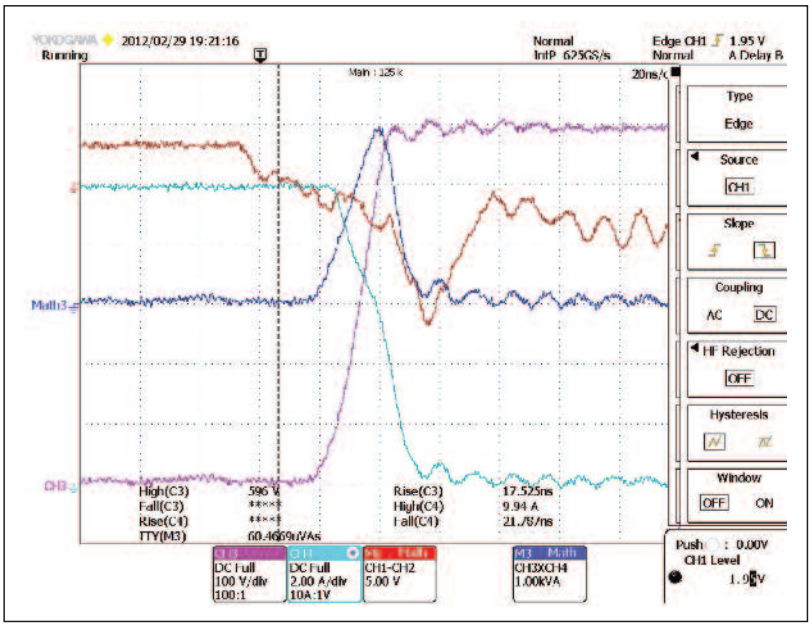
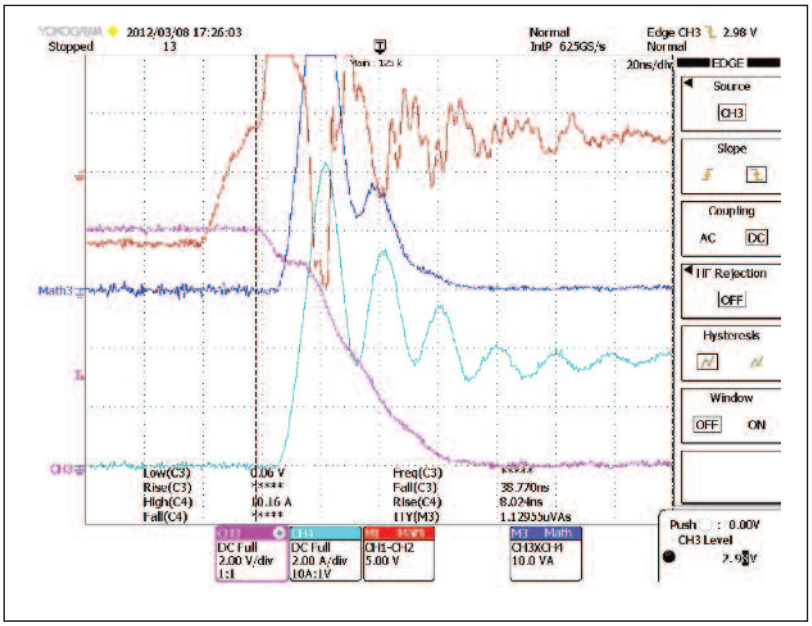
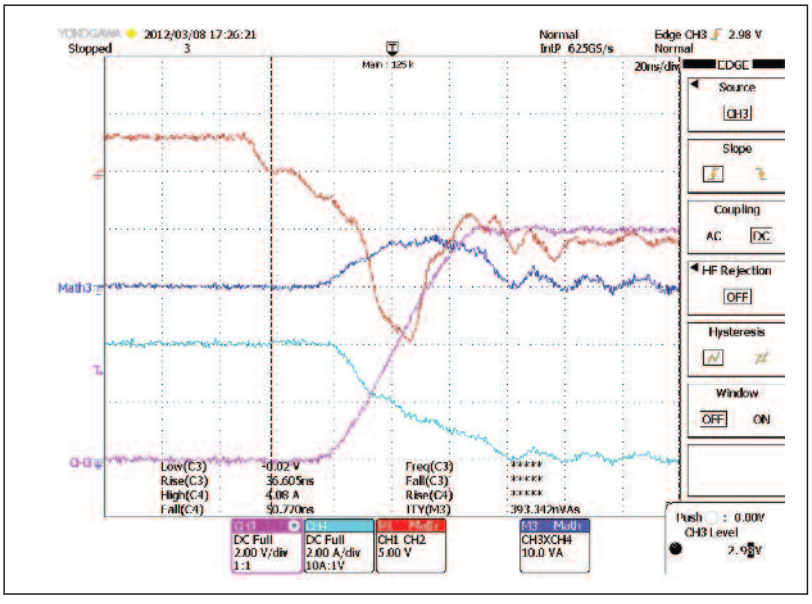


Figure 4: Turn-on of the SiC BJT (E_{on} = 226 µJ, Ch3 magenta...V_{ce} = 600V, Ch4, blue...I_c = 10 A)





ABOVE Figure 6: E_{on} measurement in CCM (E_{on} = 113 µJ, Ch3 magenta...V_{ce}, Ch4 blue...I_c)



LEFT Figure 5: **Turn-off of the SiC BJT (E_{off} = 60 µJ, M1, red...V_{be} = V_b - V_e, M3, dark blue...E_{on}, E_{off})**

we measured an increase of E_{on} losses from 117 µJ to 172 µJ and the peak voltage drop across this lead has been measured at 7 V. A similar effect can presumably be seen when considering the voltage drop across the emitter bond wire under the similar conditions. The good thing is the relatively large base-emitter capacitance which prevents the device from a parasitic turn-off. The usage of packages with separated power-emitter pins and drive-emitter pin will solve this problem and will make the device easier to control.

The boost converter

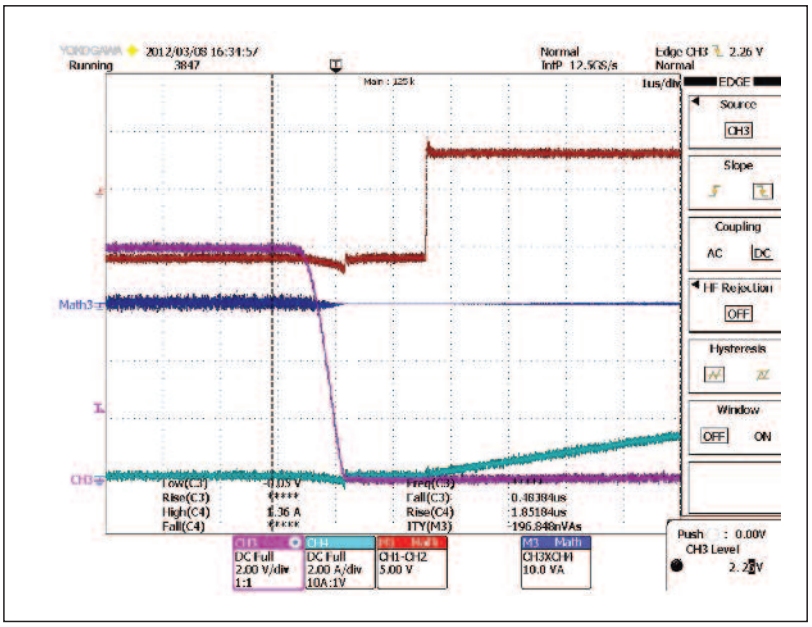
Three different boost configurations were reviewed. The first circuit was a continuous conduction mode (CCM) boost circuit using the 12 A/1200 V SiC BJT and 20 A/1200 V SiC diode. This was tested at the two switching frequencies 20 kHz and 40 kHz. The second circuit was a boundary conduction mode (BCM) boost circuit using the same devices. The ZVS approach of the BCM boost looks very promising in comparison to the hard switched CCM mode. Finally we operated our high speed IGBT FGL40N120AND in combination with the SiC diode at 20 kHz in CCM mode as a reference.

For the CCM operation we used a 10 mH coreless inductor. In order to reduce the drive losses the positive operation voltage the driver V_{cc} was reduced to 6 V. The negative driver supply V_{ee} has been increased to -6V without any impact on the drive losses. The waveforms at max power at V_{out} = 812 V are shown in Figures 6 and 7.

The big obstacle for BCM operation is high ripple currents and varying frequencies. A typical power range of a practical 2-phase interleaved PFC application is about 1 kW down to 90 VAC input voltage. Increasing the input voltage to 400 VAC, it is easily possible to increase the power range to 4 kW without changing the current level. By going from PFC to boost or from 2-phase to 4-phase interleaved operation a power level of 8 kW with this topology will be no problem. Figures 8 and 9 show the test results.

The very smooth decrease of the V_{ce} and the turn-on without any losses is clearly visible. The parasitic capacitance of the inductor and the junction capacitance of the SiC diode limit the dV/dt in Figure 9

LEFT Figure 7: **E_{off} measurement in CCM (E_{off} = 51 µJ, M1 red...V_{be}, M3 dark blue...E_{on}/E_{off})**



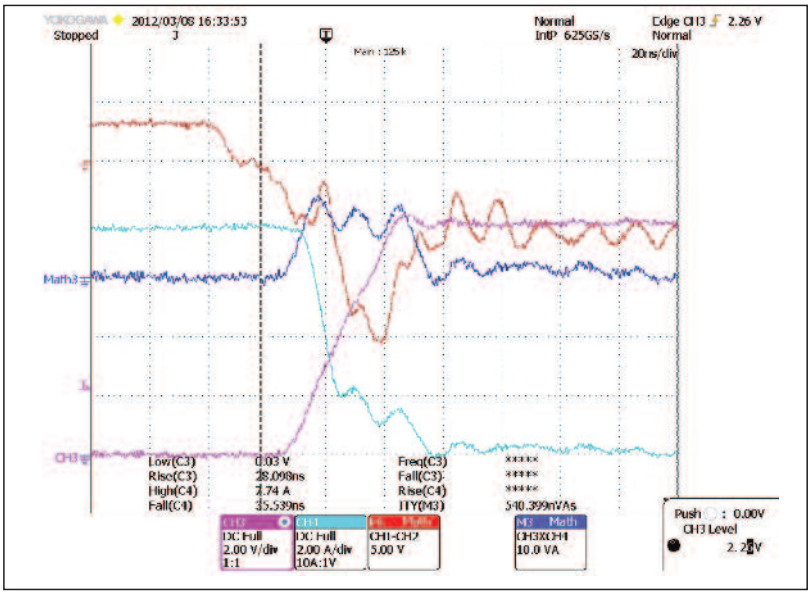


Figure 9: Turn-off waveform in BCM at V_{out} = 800 V (E_{off} = 54 µJ, M1 red...V_{be}, M3 dark blue...E_{on}/E_{off})

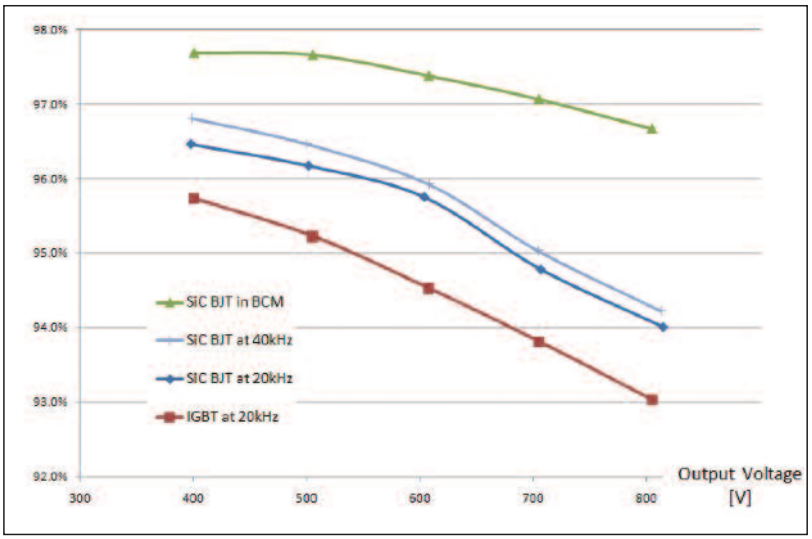


Figure 10: Measured efficiency of the variations of the boost converters

LEFT Figure 8: Smooth turn-on of the SiC BJT in ZVS (E_{on} = 0 µJ, V_{out} = 800 V, Ch3 magenta...V_{ce}, Ch4 blue...I_c)

to 5 kV/µs. All transitions look very smooth and promising, especially regarding EMI performance. For the inductor we chose a Kaschke E-core with L= 0.68 µH and multistrand wire, which is optimized for high di/dt.

Finally we compared the very well known behavior of a fast switching 1200V IGBT to the SiC BJT in CCM mode. The identical power circuit operates at 20 kHz, the driver is as well the FAN3122, but for IGBTs it operates between V_{cc} = 15V and GND. The gate resistor is equal to 4.7 Ω. The IGBT at a T_B=100ns shows about 10x higher E_{off} losses. The E_{on} losses of the SiC BJT and IGBT are in the same range.

The boost measurements have been performed with a constant V_{in} = 210 VDC. The output voltage was adjusted by changing the duty cycle or/and the frequency in 100 V steps from V_{out} = 400 V to 800 V. The load is a parallel and series operation of incandescent bulbs of 880 W in total.

The BCM boost shows best results, the CCM boost at 20 kHz and 40 kHz medium and the Si IGBT comes third in this competition. The higher efficiency for the 40 kHz CCM circuit versus the 20 kHz CCM is attributed to the lower ripple current seen in the inductor and capacitor at 40 kHz compared with the 20 kHz solution. Figure 10 shows the measured efficiency of the variations of the boost converters.

Actually we would have expected in general a better total efficiency for all measurements. Similar to tests seen on very low $R_{DS(ON)}$ MOSFETs in DC/DC applications, the package and layout effects start to dominate as the losses of the semiconductors become less significant. Based on the accompanying

Losses [W]	CCM 20 kHz	CCM 40 kHz	BCM 27 kHz – 51 kHz	IGBT CCM 20 kHz
Conduction losses	1.0	1.0	1.24	2.77
E_{on} losses	2.3	4.5	-	2.14
E_{off} losses	0.8	1.6	1.5	8.62
Total losses	4.1	7.1	2.7	13.5

Table 1: Loss calculation of the switches in the application at V_{in}=210 V, V_{out}=800 V, P_{out}=735 W (assumption for conduction losses: SIC BJT R_{on}=100 mΩ; IGBT $V_{CE(SAT)}$=1 V)

scope measurements for E_{on} and E_{off}, a loss calculation for the switches has been performed (see table 1). The weak point of the test setup is a symmetric EMI filter, which should prevent noise getting in the power analyser. A big portion of the total losses are dissipated in this device. More than 80 % of the losses are dissipated in the passive components.

Conclusion

The SiC BJT offers significant efficiency advantages in boost applications compared with silicon IGBT technology. Similar to when using other high performance technologies, the passive and layout parasitic elements start to dominate the losses. This article is derived from a paper given at PEE's Special PCIM 2012 Session [5].

Literature

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[2] Y. Gao et. al., "Comparison of static and switching characteristics of 1200 V 4H-SiC BJT and 1200 V Si-IGBT", IEEE Transactions on Industry Applications, Volume 44, No. 3, p. 887, 2008

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