3D-GaN Technology for GaN-on-Silicon

Today, the technical and electrical advantages of the AlGaN/GaN devices are understood and deployed successfully in RF applications. To make these devices commercially successful for high voltage applications, new aspects need to be considered. These aspects of technical, topological and product strategic nature are discussed and solutions are presented in this article. **Dr. Ertugrul Sönmez, Dr. Ulrich Heinle, Dr. Ingo Daumiller, and Dr. Mike Kunze, MicroGaN, Ulm, Germany**

The combination of low static and dynamic losses are provided by the AlGaN/GaN material system, which exhibits high conductivity through its highly mobile 2D-electron gas and makes small devices possible due to its high critical electrical field strength. The resulting lateral normally-on device (HEMT) features for a given R_{DSon} a so low input and output capacitance compared to its Silicon counter parts that the loss mechanisms in the application is dominated by the chosen RDSon. The absence of tail and stored minority charges leads to a switching energy dominated by dielectric charging-discharging losses, which are in the first order neither operation current nor temperature dependent and therefore for today's common switching frequencies negligible. These conditions simply lead to the well known fact that the AlGaN/GaN transistor gives technically a huge freedom in increasing the switching speed and frequency for passive component size and system volume reduction purposes.

Commercialization aspects of GaN-on-Silicon

The recent electrical efficiency trend pushes the power electronics market for higher performance at no additional cost. Therefore, to address this market the AlGaN/GaN-devices need to be provided at competitive cost, which leads to the decision to use standard large diameter Si wafers as a substrate.

This decision comes with the constrain that the required GaN epitaxy is mechanically more strained compared to competing substantially more expensive substrates like Sapphire or Silicon Carbide. On the one hand the utilization of large diameter substrates is a prerequisite to keep the process cost low. On the other hand the mechanical strain of large diameter GaN-on-Silicon is the main challenge for the commercialization process. Generally speaking, the lattice mismatch between GaN and Si cause crystallographic defects, which are partly electrically active. On Si wafers the isolating GaN layer thickness is defining the maximum application voltage of the devices processed on such wafers. Figure 1 shows a GaN-on-Silicon HEMT structure and the typical potential distribution schematically. Here, the source electrode potential is provided to the backside of the device substrate.

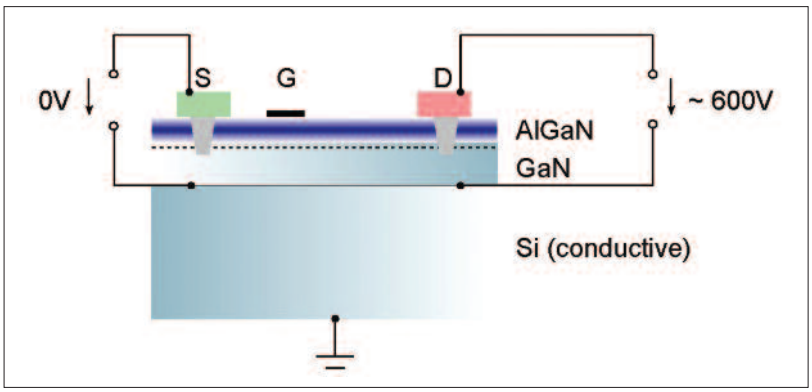

Figure 1: Typical epitaxial structure of GaN-on-Silicon substrates and potential nodes

Compared to the conductivity of the nominally isolating GaN buffer layer, the silicon substrate and its interface to the GaN buffer layer can be assumed to be conductive providing an equipotential plain. Applying the maximum application voltage at the drain electrode leads to the condition that the GaN layer alone will accommodate this voltage vertically. Thus, an increase in the demanded application voltage requires an increase of the buffer layer thickness which in turn contributes to the mechanical stress in the GaN epi-layer deteriorating material quality, homogeneity and device yield. Consequently, it is a demanding engineering task to cope with this mechanical strain for large area wafers.

From MicroGaN's perspective, today 4-inch GaN-on-Silicon wafers with the appropriate epi layer thickness are available, which make 600 V devices feasible. The material quality improvement in 6-inch GaN-on-Silicon is closely monitored and it is a matter of homogeneity progress in the epi quality and thereby a matter of yield improvement to switch to 6-inch utilization. In order to enable commercialization with a smaller wafer diameter, MicroGaN developed a new technological approach, which cuts die size for given performance into half, at least.

3D-GaN technology

The goal was to develop an area efficient device technology with an interconnect technology for surface based lateral devices for high current and high voltage application, minimize parasitics and provide flexibility in device design. The contact electrode areas have been relocated above the active region, keeping the typical low complex technology of GaN-based lateral devices and providing the following advantages at the same time:

- Standard packaging equipment compatible interface,
- minimal die area for given R_{DSon},
- therefore, minimized dynamic parasitics for given R_{DSon},
- improved yield by reduced die size and
- lowest parasitic interconnect for full function block per die by integration.

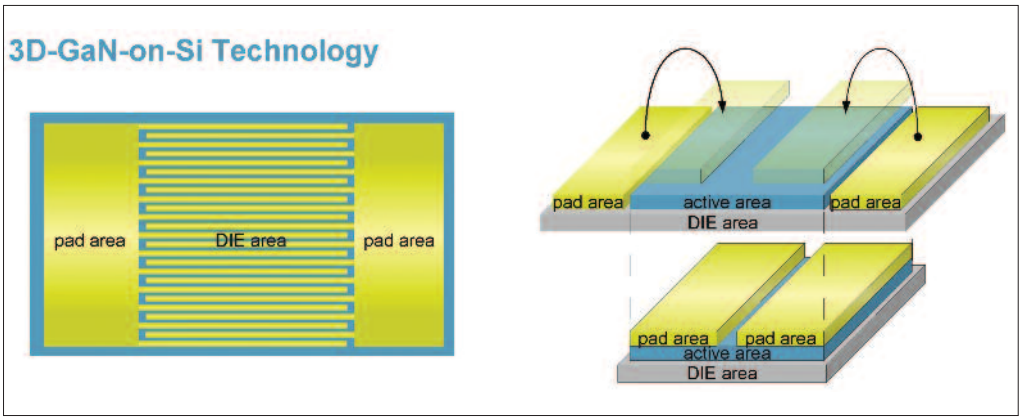

Figure 2: **3D-GaN technology topology**

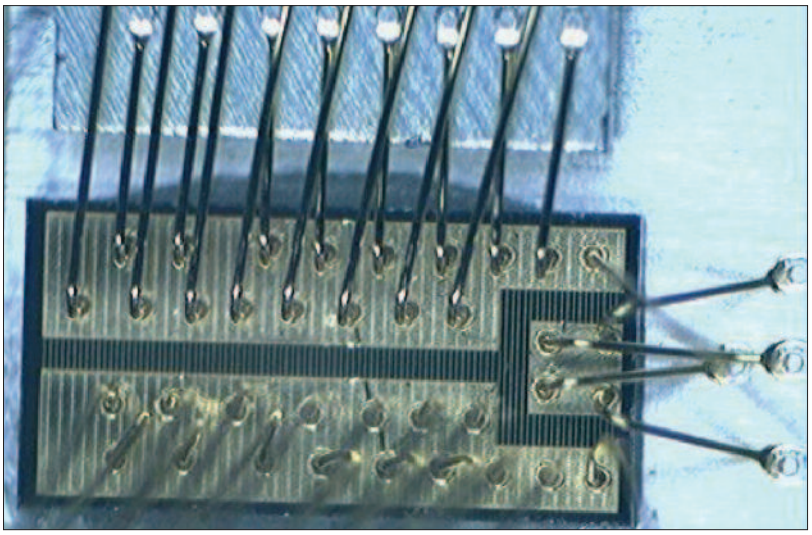

Figure 3: **Standard packaging technology compatible pad areas**

The schematic topology of a single device applying the 3D-GaN technology is shown in Figure 2 and the wire bonding technique compatible switch, on which multiple wire bonds have been applied for low inductive interconnect purposes, is shown in Figure 3, respectively.

To keep this technology flexible, it has been developed and realized modularly. To carry this flexibility to the application and thereby to the customer level, a proprietary simulation tool has been derived to predict and adjust the technology parameters for a required electrical performance. Also from the opposite direction, device topological parameters dictated from processing point of view can be tracked back to the device's electrical performance using the same tool.

Family of function blocks

The static and dynamic operational GaN normally-on switches combined with low voltage Si devices provide all required function blocks to set up an efficient high voltage solution. As a result of such a mini module, i.e cascode or cascade, normally-off switch and high voltage diode operation are available.

The normally-on operation of the devices made on AlGaN/GaN system is the natural one providing the best possible area efficiency and basically promising the fastest improvement in maturity level. All deviations from the normally-on operation at device level requires additional technology development action, which has not been prioritized at MicroGaN at the first step. The fully operable normally-on switch is depicted in Figure 4.

The 170 mΩ normally-on switch with C_{iss} = 38pF, C_{rss} = 8pF and C_{oss} = 90pF is combined with low voltage Si-MOSFET to a normally-off switch in terms of cascode configuration. This new normally-off switch has now again a very low C_{oss} of 42pF (@100V) with a resulting R_{DSon} of 250 mΩ. Using a low voltage Si diode in reverse polarization instead of the Si-MOSFET in same circuit configuration is ending up in diode operation with a voltage barrier defined by the Si diode and a differential resistance dominated by the high voltage GaN switch. The resulting diode capacitance is again defined by the GaN switch resulting in 43pF (@100V).

Attention should be payed that the low voltage Si devices are only operated at the GaN switch gate control voltage level and therefore transferring a very low amount of charge, representing the lost energy per cycle. The GaN normally-on switch is providing the high voltage isolation capability and is properly connected to its controlling Si low voltage device.

This article is derived from a paper given at PEE's Special PCIM 2012 Session [1].

Literature

[1] "Efficient Power Electronics for the price of Silicon - 3D-GaN Technology for GaN-on-Silicon", PEE Special Session "High Frequency Switching Devices and Technologies for Green Applications", PCIM 2012, Nuremberg.

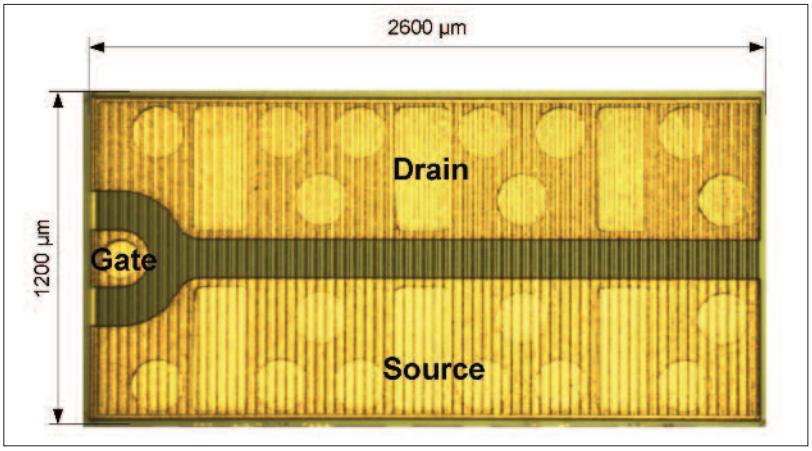

Figure 4: **600 V / 170 mΩ normally-on switch (full device area ~570 mΩmm²)**