Current Handling Capability of 600 V GaN High Electron Mobility Transistors

The development of thick, crack-free Gallium Nitride (GaN) epitaxy on standard thickness Silicon (Si) substrates, together with device fabrication in high volume silicon CMOS factories, has opened the potential for highly cost competitive, high voltage GaN devices. The simultaneous combination of advantages in efficiency, power density and cost over silicon based devices presents a compelling competitive advantage, which should help to drive rapid and widespread adoption of GaN devices throughout the power electronics industry including automotive and industrial applications. **Michael A Briere, Tim McDonald, International Rectifier; Han S. Lee, Delphi Automotive Systems; and Laura Marlino, Oak Ridge National Laboratory, USA**

The revolutionary performance capabilities of Gallium-Nitride (GaN) based power devices compared to the incumbent Silicon based alternatives has been frequently demonstrated in a variety of power electronic applications where such GaN based High Electron Mobility Transistors (HEMTs) provide remarkably improved performance for essentially any power conversion circuit in terms of power density and efficiency.

There have, however, been several members of the power electronics community who have suggested that, due to the lateral near surface nature of the GaN based power HEMTs (Figure 1), there is an inherent current handling limitation to less than 10 A for these devices. Whereas it has been previously shown that low voltage GaN-on-Si based HEMTs can process more than 150 A, even with a drain-source potential drop of 40 V [1], such current handling capability has not yet been shown for more recently developed 600 V rated devices. In this article, we present the measured current handling capability of such 600 V rated GaN-on-Si based HEMTs. Further, these results are for normally-off switches using the well established and robust cascode configuration [2], with a low voltage Si device in series with the GaN based HEMT, and with the Si device source tied to the GaN device gate. These output characteristics represent the expected initial configuration that will be used in several power electronic applications in the near future.

Research on high current capability

One impetus for higher current and voltage (power) handling power semiconductor devices is the requirements for electrification of transportation vehicles, which involves the main traction drive motor inverter, as well as auxiliary power conversion for steering, air conditioning and other passenger comfort functions.

As in other industrial motor drive applications, the main traction inverter for hybrid and electric vehicles requires significant power density, while processing as much as 200 kW of power, or even greater. For the present power bus voltage of about 450 V, this can require up to 500 A of current. Inverters for this task currently utilize IGBTs, which have a rated current density of 150 A/cm^2 with maximum current handling capabilities of some 300 A/cm^2. It is expected that any alternative power semiconductor technology, suggested for use in these applications, should provide at least the same current handling capability as the incumbent silicon based devices.

In an effort to investigate the potential for GaN based devices for such higher-powered motor drive applications, a program was sponsored by the U.S. Department of Energy under the Advanced Research Projects Agency for Energy (ARPA-E) with Delphi Automotive Systems,

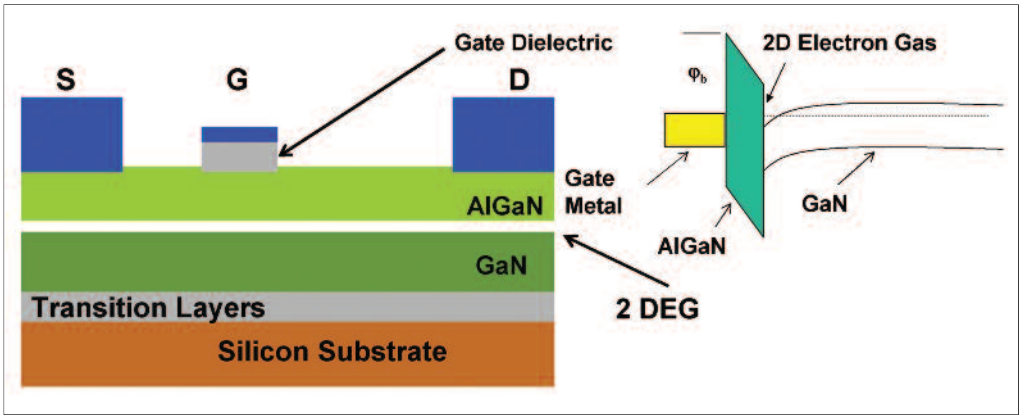

Figure 1: Schematic of a depletion mode (normally on) GaN-on-Silicon FET. 2D Electron gas spontaneously forms between AlGaN and GaN

International Rectifier (IR) and Oak Ridge National Laboratory participating. In addition to the use of IR's GaNpowIR® 600 V rated devices, the program investigated the use of a scalable two-sided cooled, sintered (wire-bondless), surface mount dual-side cooled power device package from Delphi [3]. In as much as both the package and the device layout are scalable, the early results of this study are also expected to scale to device sizes at least 5 to 10 times larger.

Figure 2 shows the 600 V GaN-on-Si based HEMT cascoded with a low-voltage

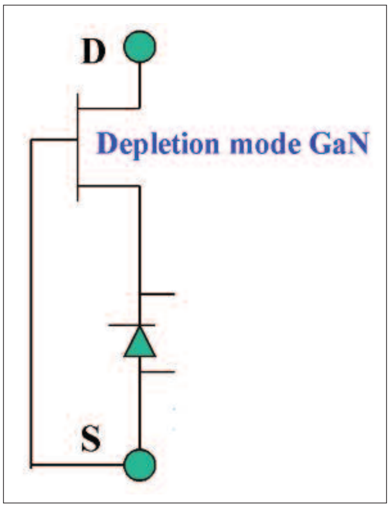

Figure 2: HV GaN switch cascoded with a Silicon FET

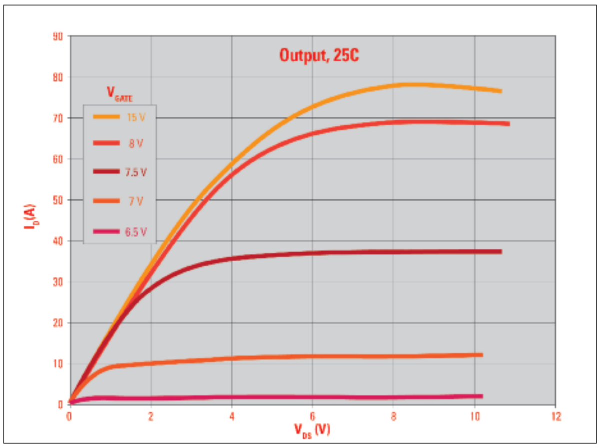

Figure 3: Measured output characteristics of a cascoded 600 V rated GaN-on-Si based HEMT with an active area of 8 mm² and a gate width of 300 mm in a dual sided cooled package at room temperature

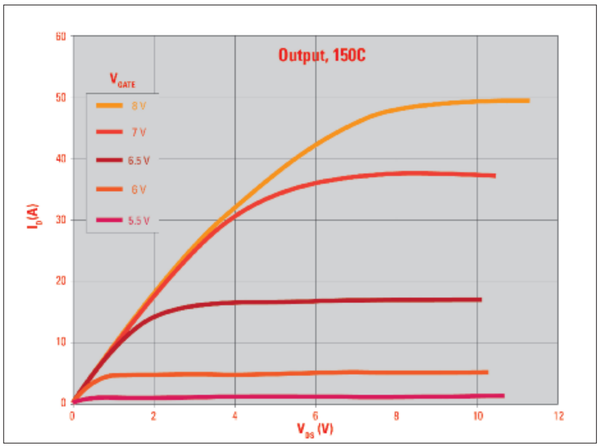

Figure 4: Measured output characteristics of the 600 V rated GaN-on-Si based HEMT in a dual sided cooled package at 150°C

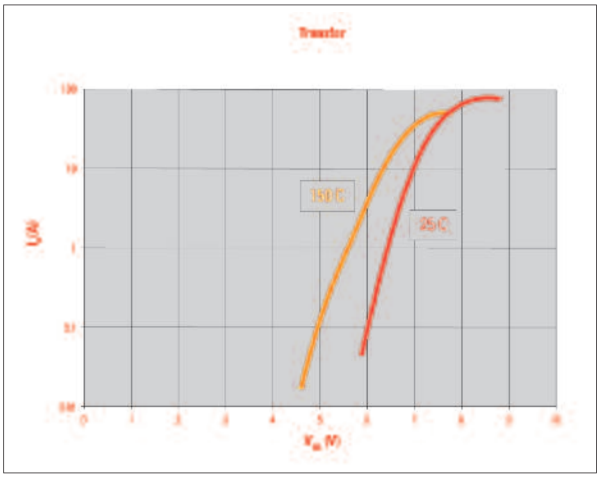

Figure 5: Measured transfer characteristics of the 600 V rated GaN-on-Si based HEMT in a dual sided cooled package at room temperature and 150°C

Silicon FET and Figure 3 the measured output characteristics of this device in a Delphi dual-side cooled power device package at room temperature. As can be seen, this device, with an active area of 8 mm_ and a gate width of 300 mm, shows well behaved current handling capability to nearly 80 A. The resulting current handling density of nearly 1000 A/cm² is well in excess of that achieved by state-of-the-art 600 V rated trench IGBTs. It can also be seen in the figure that a gate drive of at least +15 V is supported by the cascode switch design, demonstrating the advantage of the cascode switch design over an enhancement-mode GaN gate structure.

However, as can be seen in Figure 4, the current handling capability is severely degraded at 150°C, as expected for a FET and unlike the behavior for IGBTs where the saturated current capability are not adversely effected by increasing device temperature. The resulting current density per active area of the GaN based HEMT at 150°C is still a respectable 625 A/cm². The unipolar device also has the advantage that it does not exhibit the large forward knee voltage associated with the bipolar IGBT, which is very deleterious in applications at light load conditions. As such, the improved working current density of approximately 200 A/cm_ can be achieved for the GaNpowIR HEMTs with enhanced application performance, allowing the simultaneous achievement of greater power density and efficiency.

Figure 5 shows well behaved normally-off transfer characteristics at both room temperature and 150°C, with near full channel enhancement at a gate voltage of +9 V. The stable threshold voltage of more than +4 V at 150°C provides for a high level of noise immunity, further demonstrating the advantage of the cascode switch design over a discrete enhancement mode GaN gate structure.

The consistency of the measured on-state resistance as a function of drain-to-source current is shown in Figure 6, for both room temperature and 150°C operation. As expected, there is approximately a factor of 2 in the measured on-resistance over this temperature range, due primarily to the decrease in the mobility of the electrons in the two-dimensional electron gas of the GaN based HEMT.

Cooling down

It is important to note that the ability to practically extract the current carrying capability of lateral GaN based HEMTs depends on the proper application of modern packaging technology. While a

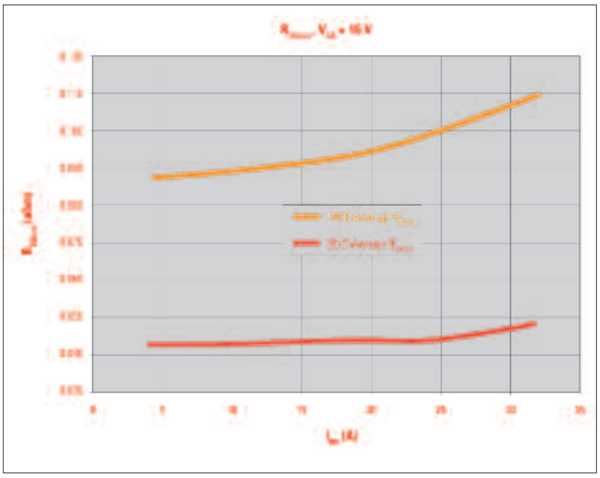

Figure 6: Measured on-state resistance as a function of drain to source current for the 600 V rated GaN-on-Si based HEMT in a dual sided cooled package at room temperature and 150°C

flipped GaN device, as described previously [4], using solderable front metal to attach the device to the external circuit elements without wirebonds, allows for the scaling of the semiconductor, it must be properly paired with a packaging technology that can effectively transfer this current to the application circuit, if chip scale packaging is undesirable. Another advantage of the flipped, direct-mount device construction is that much of the heat generated in the conduction region of the GaN device is removed very effectively through the top surface of the device, negating the often touted deficiency of Silicon substrates for poor heat conduction compared to, for instance, Silicon Carbide (SiC).

In this way, highly efficient higher power devices can be constructed using the combination of GaN-on-Si semiconductors with flip chip, direct surface mount packaging technologies. It is expected that considerable efforts will be expended over the coming several years to further demonstrate and leverage the inherently high current handling capability of efficient, unipolar GaN-on-Si based power HEMTs in many power electronic applications where higher power density and higher efficiency are needed at a commercially viable cost.

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Literature

[1] Electronics in Motion and Conversion, November 2010 pp. 20-24

[2] Power Electronics Technology, July 2012 pp. 19-21

[3] See within arpa-e.gov

[4] Power Electronics Europe, April 2010 pp. 35-37