Sugar-Coated Power Cycling Lifetime

Power cycling is an important method to characterize the lifetime of power semiconductor modules. Application engineers use lifetime curves published by manufacturers to verify that their system design meets the required reliability. An important condition for the lifetime of a module under repeated temperature swings is the control strategy applied during the test. Power cycling tests with identical start condition but different control strategies have been performed, which have been conducted on specially assembled test equipment with ultimate control of all test parameters. The results show, that different control strategies deliver lifetime results that vary by a factor of 3. **Stefan Schuler, Development Engineer and Dr. Uwe Scheuermann, Department Manager Product Reliability, SEMIKRON, Nuremberg, Germany**

In the early days of power cycling testing the temperature swing was considered as the only parameter relevant for the test result. The very comprehensive investigation conducted during the LESIT project [1] in the middle of the 1990s revealed that also the medium temperature of the temperature swing has a significant impact on the number of cycles to failure.

A recent publication [2] confirmed this result and extends the list of parameters with an impact on the test result by four additional factors: the on-state time of the load impulse, the bond wire diameter, the current density in a bond contact and even the chip blocking rating, which reflects the variation in chip thickness with the blocking voltage in state-of-the-art IGBT designs.

The discussion so far only addressed the set of start parameters, which are relevant for a power cycling test; the numbers of cycles to failure are conventionally related to this set of initial parameters. In an experimental power cycling test, however, these initial parameters are not constant throughout the test. Degradation effects can cause a change of these parameters and an important feature of the power cycling test is the control strategy, i.e. the strategy how to react on parameter changes during the test.

Control strategy in PC tests

Since a power cycling test simulates the stress incorporated in a power module under highly accelerated test conditions, wear-out and degradation effects must be expected.

Solder fatigue phenomena increase the thermal resistance of the device and thus increase the junction temperature under constant test conditions. The positive temperature coefficient of modern IGBT devices will consequently lead to increased losses, which again will increase the device temperature. This positive feedback loop can significantly accelerate the failure process.

The mechanical and thermal stress implied on wire bond interconnections can result in an increasing resistance of the contact and can alter the current distribution in the devices (Figure 1). This degradation process, which can lead to a total breakdown of individual wire bonds, can be detected in the monitored forward voltage drop by instantaneous stepwise increase. Therefore, the control strategy is a very important feature of the power cycling test. Four different control strategies will be compared in the experimental investigation:

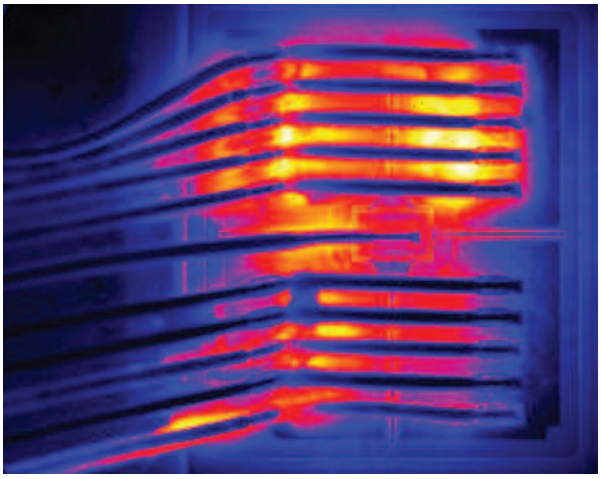

Figure 1: Infrared image of an aged IGBT with inhomogeneous surface temperature

1) t_{on} and t_{off}=const.

The strategy of constant timing switches the load current on and off in fixed time intervals. A degradation of the module will have an immediate impact on the resulting temperature swing with no compensation by a control strategy. This is the most severe test strategy.

2) ΔT_c=const.

This control method uses a reference thermocouple to turn on and off the load current according to fixed case temperatures. The on-time and off-time is not fixed, but is determined by the time constants for heating and cooling the device. This is the preferred test method, since a change of the cooling liquid temperature would be compensated by adjusting the heating and cooling times. However, also a potential degradation of the thermal interface between the case of the module and the heat sink surface would be compensated by this control strategy. It is therefore less severe than the constant timing strategy.

3) P_V=const.

The third control method is based on constant t_{on} and t_{off} times with the additional requirement, that the power losses are kept constant. This requirement is achieved by

controlling the gate voltage. At test start, the gate voltage is reduced, so that an increase of the forward voltage drop due to degradation can be compensated by enhancing the gate voltage. This control strategy is much less severe for a power module, because it significantly reduces the acceleration effects by positive feedback loop described above.

4) ΔT_j=const.

As a pendant to the most severe test with no compensation at all, the junction temperature swing control totally compensates for any degradation. This can be accounted for by adjusting the load current, by controlling the timing or by regulating the gate voltage.

Experimental PC test equipment

Experimental test equipment has been constructed for power cycling a single chip in an open housing without silicone gel. The chip temperature can be directly monitored by a pyrometer (2.5 mm spot size).

The module is mounted on a 18°C liquid cooled copper heat sink with an attached thermocouple to measure the base plate temperature. The test equipment is controlled by a Linux PC. It records the gate voltage V_G, the collector emitter voltage V_{CE}, the collector current I_C, the pyrometer temperature T_j and the case temperature T_c with a sample rate of 66.7 ms.

The gate voltage can be adjusted via a digital analog controller 15 times a second by software and thus allows a control of the gate voltage during the power cycles. The desired value is calculated as a feed forward control with a low pass filter to eliminate gate voltage overshoot.

An adjustable fast switching constant current source (250 A/12 V) is used to supply the load current. It is controlled by the software as well, so that the equipment is not limited to square shaped current pulses, but can run freely defined current waveforms and even customer specific temperature profiles.

All test parameters must be carefully adjusted to ensure identical start conditions. Since the individual test sample each have a slightly different thermal resistance $R_{th(j-c)}$ and V_{CE} values, the gate voltage V_{GE} control was applied to adjust them as close as possible (Figure 2).

After a stabilization sequence, an automated procedure starts with the measurement of the thermal resistance $R_{th(j-c)}$. Then all other parameters were evaluated on a statistical basis during the next 100 power cycles. Based on these results, the initial parameters were adjusted to generate a temperature swing ΔT_j=125°C at a medium temperature T_m=87.5°C. The constant DC current was fixed at I_C=85 A for all tests with the 9.1 x 7.7 mm² generation 4 IGBT from Infineon.

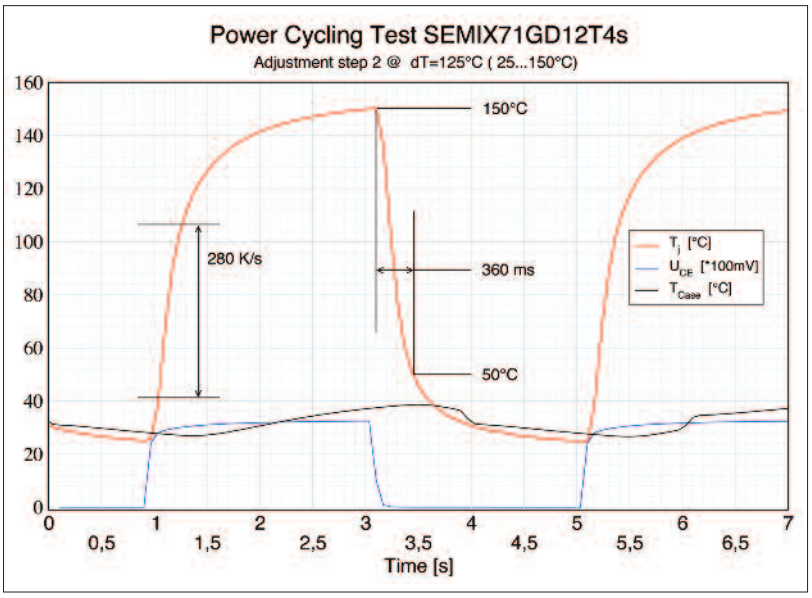

Figure 2: **Initial adjustment of parameters for the PC test**

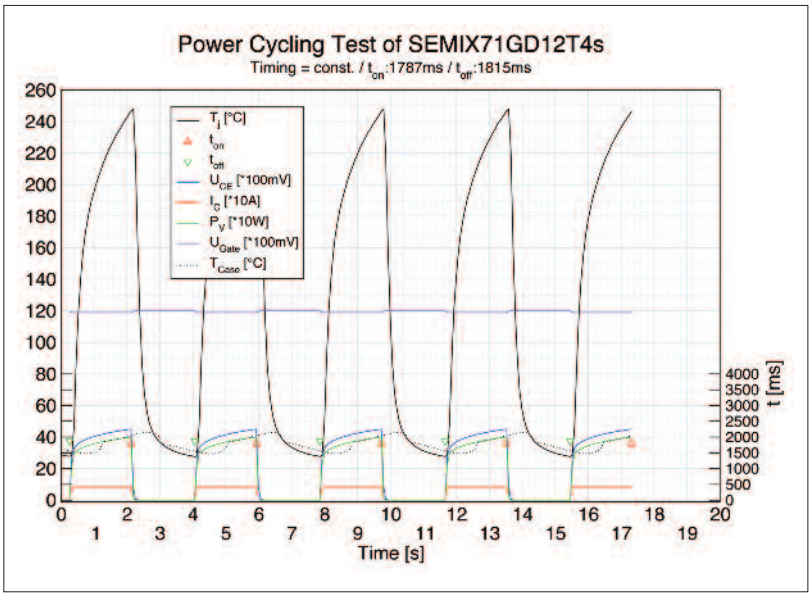

Figure 3: **PC parameters for t_{on}/t_{off}=const.**

Experimental results

After the initial adjustment procedure, the four previously described control strategies were applied to four different test samples. The differences in evolution of parameters are presented here for the situation after 31,000 power cycles, when degradation effects have already caused a change of the initial conditions.

1) t_{on}=const. and t_{off}=const.

The control strategy of constant timing leads to an increase of the temperature swing during the test. After 31,000 cycles, the end-of-life is almost reached and the maximum junction temperature has well exceeded 240°C. The dissipated power has increased by 23 % from the initial value (Figure 3).

2) ΔT_c=const.

This control strategy maintains constant maximum and minimum case temperature limits and adjusts the ton and toff times accordingly. These limits were selected to 27.10°C and 33.77°C in the initial adjustment procedure. The power dissipation has increased by 8.9 % due to degradation. The total cycle time (t_{on}+t_{off}) has decreased by 6.9 % and the maximum junction temperature has just exceeded 175°C after 31,000 cycles (Figure 4).

3) P_V=const.

The third control method of constant timing with the additional requirement of

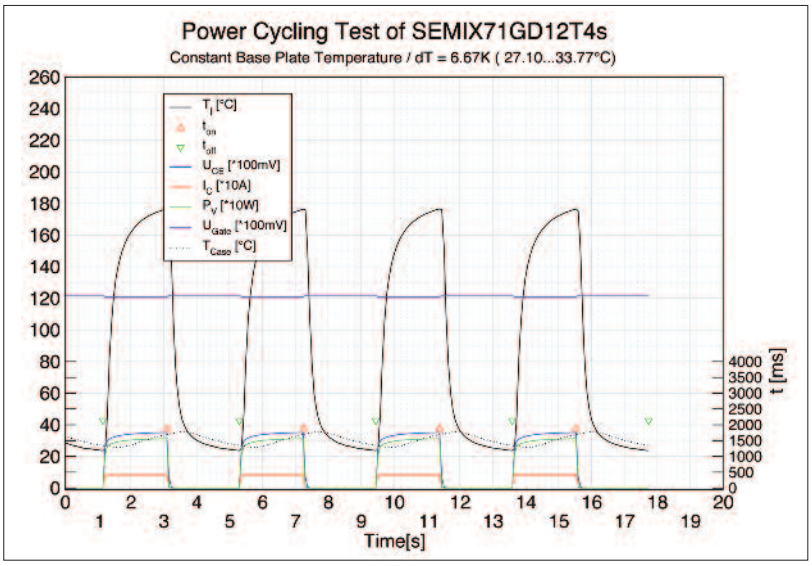

Figure 4: **PC parameters for Δt_c=const.**

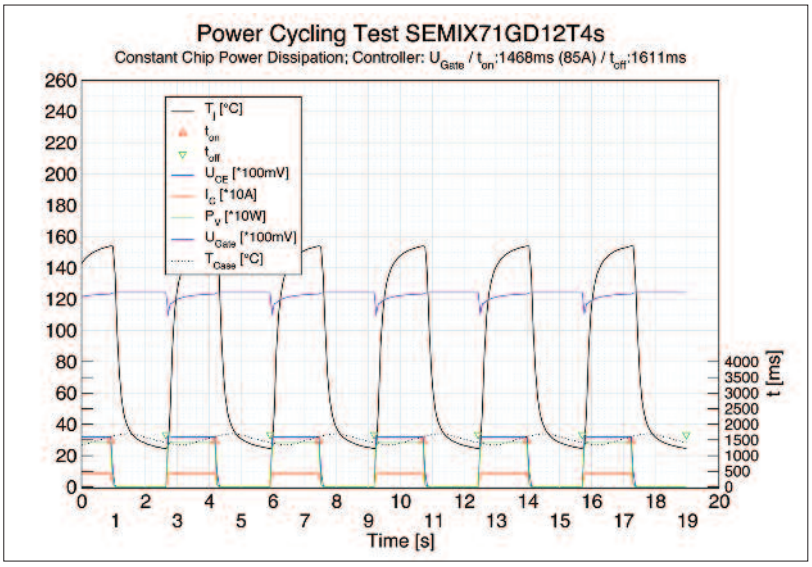

Figure 5: **PC parameters for P_v=const.**

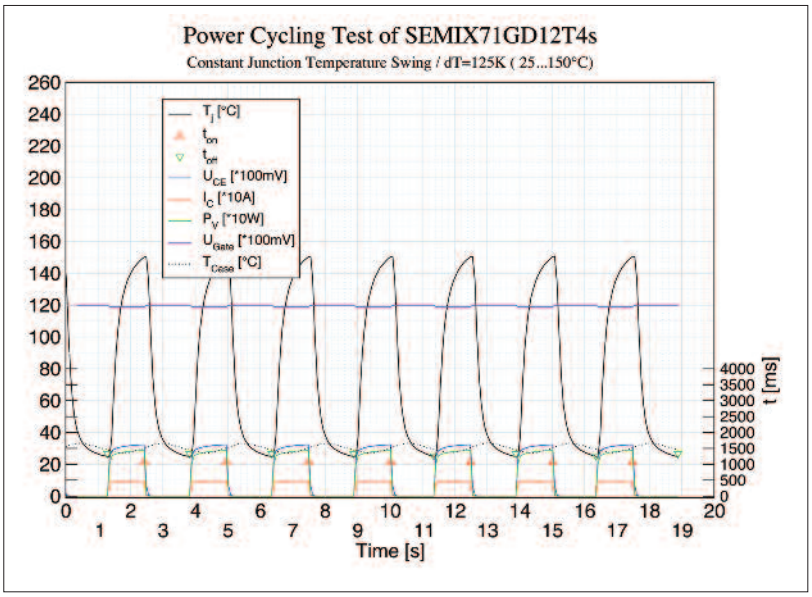

Figure 6: **PC parameters for ΔT_j=const.**

constant power losses shows only little deviation from the initial starting conditions. The maximum junction temperature reaches only 155°C after 31,000 cycles, which is equivalent of a 3 % increase in temperature swing. The control of the gate voltage can be seen clearly in Figure 5, starting with a low value right after turn on and is then increased as the temperature rises in each cycle. The control of the gate voltage leads to almost square shaped power loss profiles during the cycles. The maximum gate voltage at the end of each cycle was adjusted to 12.06 V in the initial phase and has increased to 12.5 V after 31,000 cycles. The increase continued and reached 14.53 V at the end-of-life.

4) ΔT_j=const.

Finally, the control strategy that maintains a constant junction temperature swing, indicates no change in temperature swing after 31,000 cycles (Figure 6). The reduction of on-time, however, is significant to a value of 42 % of the initial adjustment value, showing that severe degeneration effects are to be compensated. Due to this ongoing compensation, the lifetime can be dramatically increased. In the final phase of this test, ton will be reduced to even 11.8 % of the initial value.

End-of-life results

Figure 7 shows the evolution of the maximum junction temperature versus the number of cycles during the power cycling test in comparison for all four control strategies. The curves also show the numbers of cycles to failure.

For the constant timing, the end-of-life was reached after 32,073 cycles, when the junction temperature approached 360°C and the emitter metallization melted and failed.

In case of constant base temperature swing, the final failure was observed after 47,485 cycles, when the maximum junction temperature exceeded 340°C. Again, the metallization of the emitter failed.

With the third one, the constant power losses, a lifetime of 69,423 cycles was determined. In this case, the maximum junction temperature never exceeded 178°C and the failure was caused by the lift-off of all wire bonds, while the emitter metallization remained intact.

Last, the constant junction temperature swing recorded a lifetime of 97,171 cycles. Obviously, the control loop limits the maximum junction temperature effectively to values below 160°C until the end-of-life is almost reached. Then, the temperature control procedure fails to function when

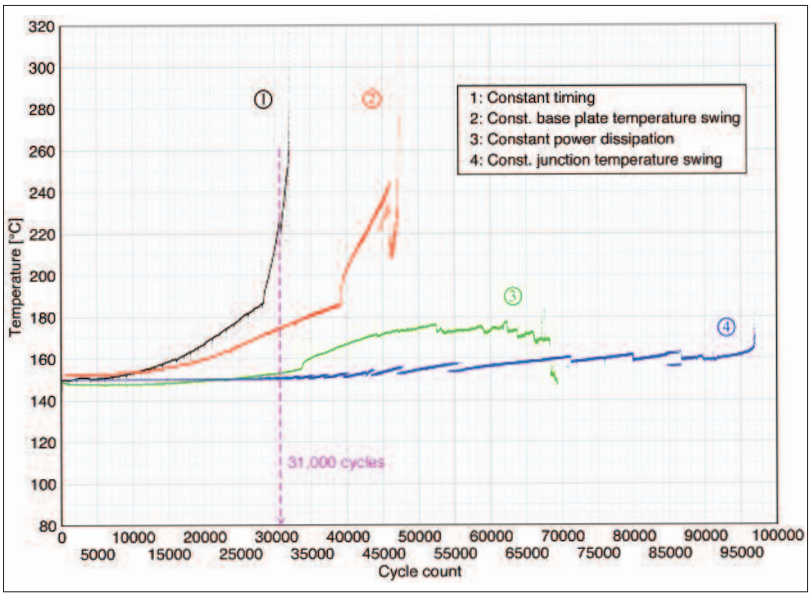

Figure 7: Comparison of maximum junction temperature evolution for all four different control strategies

the on-time is approaching the control interval. The minimum value for the on-time just before the final failure was t_{on}=0.42 s.

Reliability estimation

As seen, lifetime is determined strongly by the chosen control strategy [3]. Therefore, the answer for the right strategy also needs to consider the practical usage. From this application point of view, only the first two control strategies are relevant to estimate the reliability in real applications. Here, the constant base plate temperature swing control (ΔT_C=const.) is the preferred method. It is immune to changes in the cooling condition and also eliminates degradation effects in the thermal grease interface to the heat sink. The last two strategies are not suited for field life estimation, because they reduce the stress during the lifetime to compensate for ageing effects.

Application engineers, who are using power cycling curves to estimate the lifetime of a module in their application, should consult the manufacturer. Why? For information on the applied control strategy, to generate non-sugar-coated lifetime curves.

Literature

[1] M.Held, P.Jacob, G.Nicoletti, P.Scacco, M.H.Poech, Fast Power Cycling Test for IGBT Modules in Traction Application, Proc. Power Electronics and Drive Systems 1997, 425-430.

[2] R.Bayerer, T.Herrmann, T.Licht, J.Lutz, M.Feller: Model for Power Cycling Lifetime of IGBT Modules - various factors influencing lifetime, Proc. CIPS 2008, pp. 37-42.

[3] S.Schuler, U.Scheuermann: Impact of Test Control Strategy on Power Cycling Lifetime, Proc. PCIM 2010