Industrial Grade 25 A Versatile Voltage Regulator

At APEC International Rectifier introduced the IR3847 high current Point-of-Load (POL) integrated voltage regulator that extends the current rating of IR's third generation SupIRBuck® family up to 25 A in a compact 5x6 mm package. **Ramesh Balasubramaniam, Cecilia Contenti, Enterprise Power Business Unit, International Rectifier, El Segundo, USA**

As a result of a new thermally enhanced package using copper clip and several proprietary innovations in the controller, the IR3847 can operate without heatsink, and reduces PCB size by 20 % compared to alternative integrated solutions and 70 % compared to discrete solutions using a controller and power MOSFETs. A complete 25 A power supply solution can be implemented in as little as 168 mm^2. Peak efficiency is greater than 96 % and temperature rise at 25 A is as low as 50 K (see Figure 1).

Theory of operation

The IR3847 uses a PWM voltage mode control scheme with external compensation to provide good noise immunity and maximum flexibility in selecting inductor values and capacitor types. The switching frequency is programmable from 300 kHz to 1.5 MHz by connecting an external resistor from Rt pin to LGnd. The output voltage is precisely regulated and can be programmed via two external resistors from 0.6V to 0.86 * PVin.

The IR3847 operates with an internal bias supply (LDO) which is connected to the VCC pin. This allows operation with single supply. The bias voltage is variable according to load condition. If the output load current is less than half of the peak-to-peak inductor current, a lower bias voltage, 4.4 V, is used as the internal gate drive voltage; otherwise, a higher voltage, 6.8 V, is used. This feature helps the converter to reduce power losses. The device can also be operated with an external supply from 4.5 to 7.5 V, allowing an extended operating input voltage (PVin) range from 1.0 to 21 V. For using the internal LDO supply, the Vin pin should be connected to PVin pin. If an external supply is used, it should be connected to VCC pin and the Vin pin should be shorted to VCC pin.

Under-voltage lockout and POR

The under-voltage lockout circuit monitors the voltage of VCC pin and the Enable input. It assures that the MOSFET driver outputs remain in the off state whenever either of these two signals drops below the set thresholds. Normal operation resumes once VCC and Enable rise above their thresholds.

The POR (Power On Ready) signal is generated when all these signals reach the valid logic level (see system block diagram in Figure 2). When the POR is asserted the soft start sequence starts.

Enable

The Enable features another level of flexibility for startup. The Enable has precise threshold which is internally monitored by the Under-Voltage Lockout (UVLO) circuit. Therefore, the IR3847 will turn on only when the voltage at the Enable pin exceeds this threshold, typically 1.2 V.

If the input to the Enable pin is derived from the bus voltage by a suitably programmed resistive divider, it can be ensured that the IR3847 does not turn on until the bus voltage reaches the desired level (see Figure 3). Only after the bus voltage reaches or exceeds this level and voltage at the Enable pin exceeds its threshold, IR3847 will be enabled. Therefore, in addition to being a logic input pin to enable the IR3847, the Enable feature, with its precise threshold, also allows the user to implement an Under-Voltage Lockout for the bus voltage (PVin). This is desirable particularly for high output voltage applications, where we might want the IR3847 to be disabled at least until PVIN exceeds the desired output voltage level. A resistor divider is used at EN pin from PVin to turn on the device at 10.2 V.

Pre-bias startup

The device is able to start up into a pre-charged output which prevents oscillation and disturbances of the output voltage.

The output starts in asynchronous

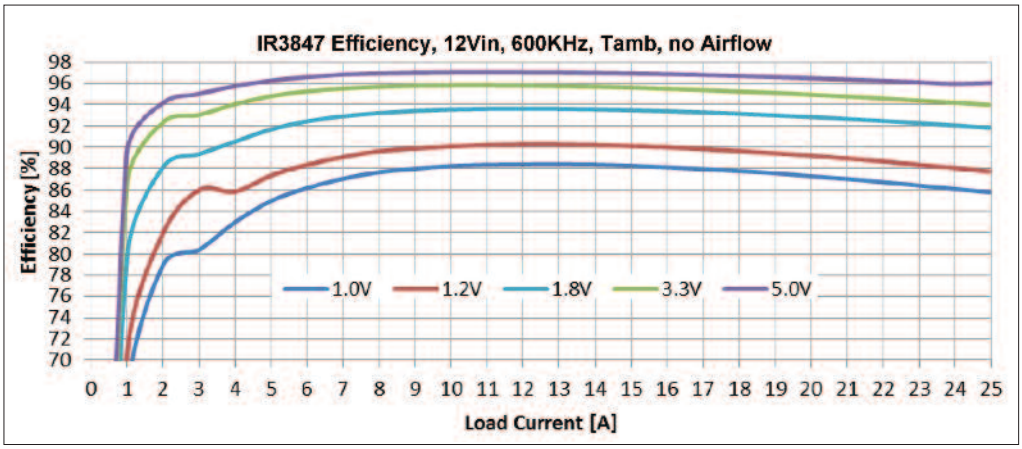
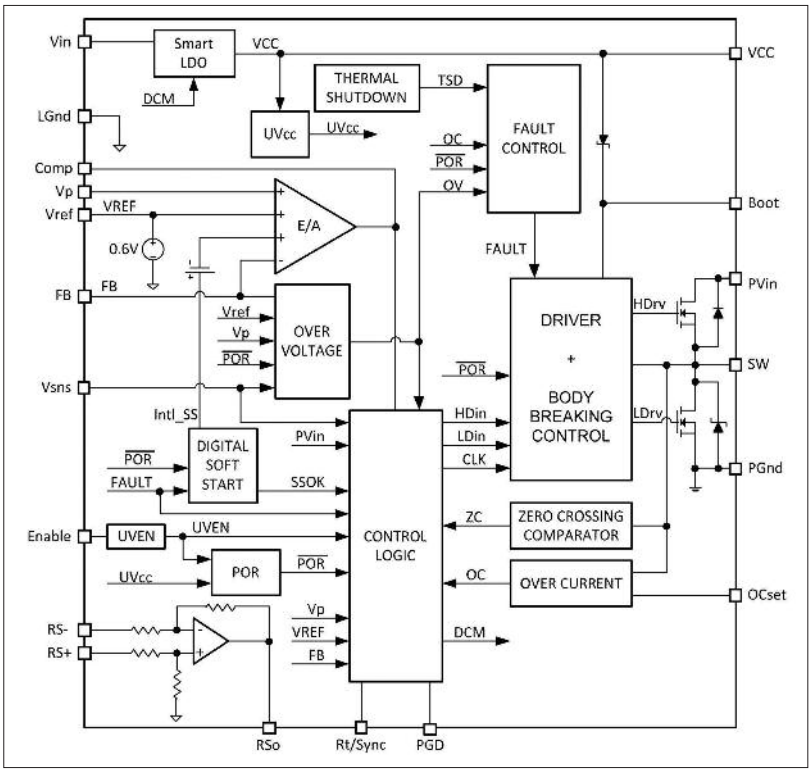
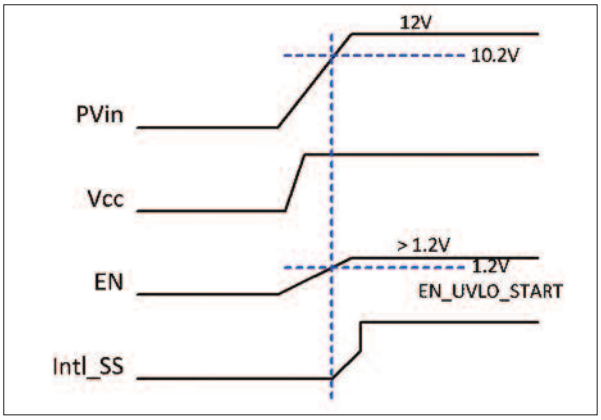


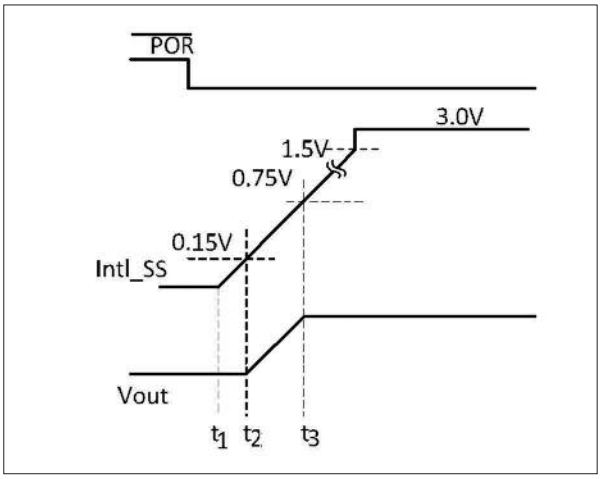
Figure 1: New POL integrated voltage regulator featuring peak efficiency greater than 96 %



ABOVE Figure 2: IR3847 functional block diagram



LEFT Figure 3: Normal Start up, device turns on when the bus voltage reaches 10.2 V



LEFT Figure 4: Theoretical operation waveforms during soft-start (non tracking / non sequencing)

fashion and keeps the synchronous MOSFET (Sync FET) off until the first gate signal for control MOSFET (Ctrl FET) is generated. The sync FET always starts with a narrow pulse width (12.5 % of a switching period) and gradually increases its duty cycle with a step of 12.5 % until it reaches the steady state value. The number of these startup pulses for each step is 16 and it is internally programmed.

Soft-start

IR3847 has an internal digital soft-start to control the output voltage rise and to limit the current surge at start-up. To ensure correct start-up, the soft-start sequence initiates when the Enable and V_{cc} rise above their UVLO thresholds and generate the POR signal. The internal soft-start (Intl_SS) signal linearly rises with the rate of 0.4mV/µs from 0 to 1.5 V. Figure 4 shows the waveforms during soft start. During the soft start the over-current protection (OCP) and over-voltage protection (OVP) is enabled to protect the device for any short circuit or over voltage condition.

Over current protection

The Over Current (OC) protection is performed by sensing the inductor current through the on-resistance of the synchronous MOSFET. This method enhances the converter's efficiency, reduces cost by eliminating a current sense resistor and any layout related noise issues. The Over Current (OC) limit can be set to one of three possible settings by floating the OCset pin, by pulling up the OCset pin to V_{cc}, or pulling down the OCset pin to PGnd. The current limit scheme in the

IR3847 uses an internal temperature compensated current source to achieve an almost constant OC limit over temperature.

Over Current Protection circuit senses the inductor current flowing through the synchronous MOSFET. To help minimize false tripping due to noise and transients, inductor current is sampled for about 30 ns on the downward inductor current slope approximately 12.5 % of the switching period before the inductor current valley. However, if the synchronous MOSFET is on for less than 12.5 % of the switching period, the current is sampled approximately 40 ns after the start of the downward slope of the inductor current. When the sampled current is higher than the OC limit, an OC event is detected.

When an Over Current event is detected, the converter enters hiccup mode. Hiccup mode is performed by latching the OC signal and pulling the Intl_SS signal to ground for 20.48 ms (typ.). OC signal clears after the completion of hiccup mode and the converter attempts to return to the nominal output voltage using a soft start sequence. The converter will repeat hiccup mode and attempt to recover until the overload or short circuit condition is removed.

Over-voltage protection

Over-voltage protection (OVP) is achieved by comparing sense pin voltage Vsns to a preset threshold. In non-tracking mode, OVP threshold can be set at 1.2*Vref; in

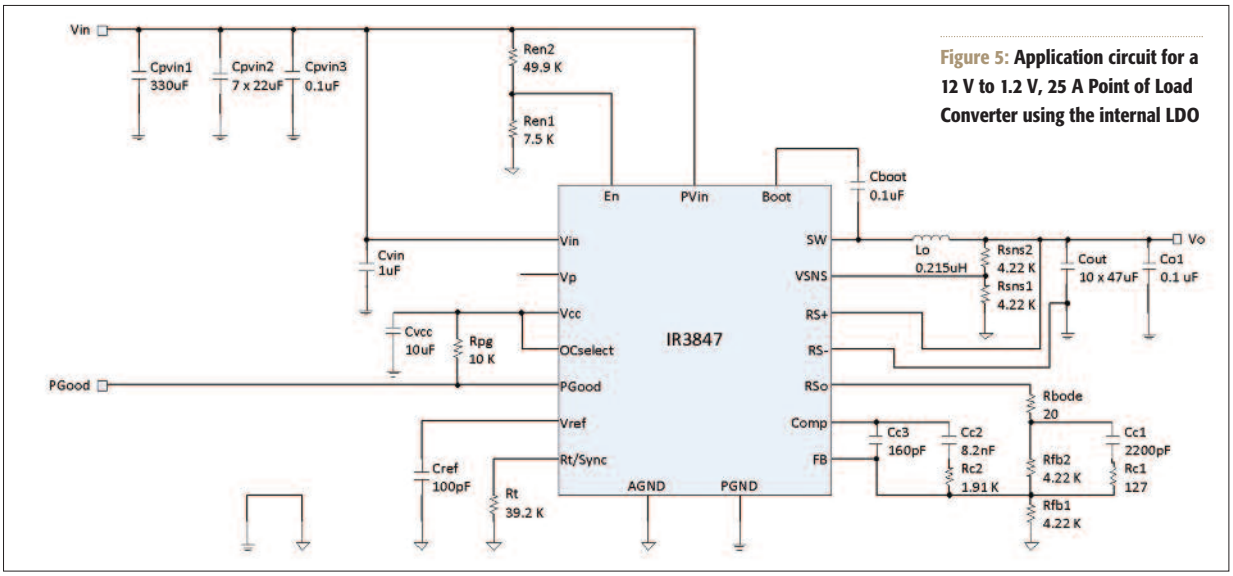


Figure 5: Application circuit for a 12 V to 1.2 V, 25 A Point of Load Converter using the internal LDO

tracking mode, it can be at 1.2*Vp. When Vsns exceeds the over voltage threshold, an over-voltage trip signal asserts after 2.5 µs (typ.) delay. The high side drive signal HDrv is latched off immediately and PGood flags are set low. The low side drive signal is kept on until the Vsns voltage drops below the threshold. HDrv remains latched off until a reset is performed by cycling either VCC. OVP is active when enable is high or low. Vsns voltage is set by the voltage divider connected to the output and it can be programmed externally.

Design example

The design example is a typical application for the IR3847 (see Figure 5) with 12 V input voltage, switching frequency 600 kHz, 1.2 V output voltage, 25 A output current, and ± 1% ripple voltage.

A free user friendly, interactive, web-based design tool is available at http://mypower.irf.com/SupIRBuck to simplify design and calculate Bill of Materials, schematics, Bode diagram, simulation waveforms and thermal analysis for selected design inputs. The IRDC3847 reference design is also available.

Literature

Preliminary IR3847 datasheet, International Rectifier, March 2013