Power Semiconductors on 300-Millimeter Wafers

In February 2013 Infineon Technologies released the first products of the CoolMOS™ family being produced on its new 300-millimeter line at the Villach site in Austria. The production process based on the new technology has completed qualification and is now ready for delivery. This follows more than three years of intensive research and development activities within Infineon and with partners all over Europe in the fields of process technologies, production technologies as well as handling and automation for advanced power technologies. **Dr. Gerald Deboy, Dr. Kurt Aigner Infineon Technologies, Villach, Austria**

Due to their larger diameter compared to standard 200-millimeter wafers, two-and-a-half times as many chips can be made from each wafer. With this massive invest of capital and engineering efforts Infineon Technologies will be able to sustainably support the market with significantly enhanced capacity for leading edge power semiconductor devices.

The need for efficient power electronics

Power electronics play a major role in harvesting the huge potentials towards a more efficient usage of energy around the globe as outlined in the OECD scenarios in Figure 1. Being more efficient along the generation and conversion chain will be the key enabler to reduce the emission of greenhouse gases.

With an ever increasing contribution of electricity to the global energy mix the importance of power electronics will further grow. Most importantly, power electronics are mandatory to dramatically reduce the huge energy losses that occur between the primary energy source and the energy end use(r). Today, even losses of up to 90 % are seen in the market, with 50 % loss being the norm rather than the exception. Figure 2 depicts the losses from the first conversion into electricity, along the distribution to the final delivery of power to the load in the end user equipment. Modern power semiconductor devices play a vital role to drive power electronics to better performance and lower system costs, thus supporting further proliferation of power electronics into more and more aspects of power conversion and control.

If we take a closer look into the saving potential of various power applications the biggest impact can be reached in motor control applications, where up to 40 % of the electricity is being consumed. The key topic here is to move from on/off control to variable speed drives, which besides the enormous energy saving foster less noise generation and more comfort in e.g. air conditioning applications. A further important focus area are lighting applications with a roughly 15 % contribution to the energy consumption. In lighting mainly the transition from incandescent bulbs and magnetic ballasts, now being widely banned from EU countries to LED lighting and more sophisticated electric ballasts drives the saving of energy. Power electronics support these transitions with fitting high voltage MOSFETs, drivers and controllers.

Last but not least power supplies fuelling datacenters and RF telecommunication base stations are indispensable for modern life style with ubiquitous internet access and exchange of data at high speed. Industry has undertaken major steps under the Computing Climate Initiative to set out more and more challenging efficiency targets now culminating in the titanium standard, which will be rolled out with ever increasing share in new IT equipment in the coming years. Key technologies here are mainly high voltage and low voltage MOSFETs ranging from 600 V devices in the AC front end to 25 V in the point-of-load converter.

Strongly growing applications such as photovoltaics (forecasted to 60 GW fresh installations in 2016) and electro mobility will further drive global demand for power semiconductor devices.

Power technologies on 300 mm

Infineon Technologies hence undertook as

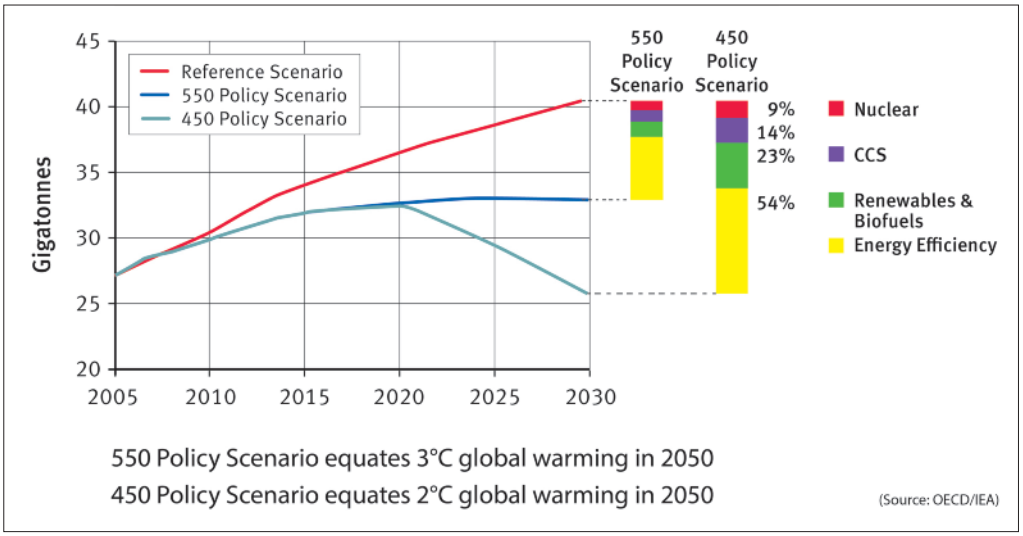

Figure 1: CO_2 reduction in different scenarios. The highest CO_2 savings can be gained from increasing energy efficiency

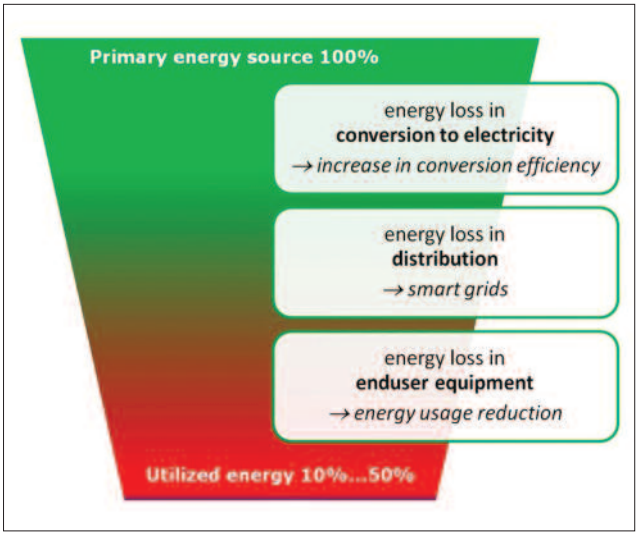

Figure 2: Energy losses from the source to the sink are dramatic

the first power semiconductor company the challenging task to manufacture leading edge power devices on 300 mm wafers. This massive investment of capital and engineering efforts will put Infineon Technologies into a prime position for sustainably delivering production capacity into a power sustainably growing market. Bundling the results of more than three years intensive research with the manufacturing expertise in factories such as Villach and Dresden, Infineon achieved the first customer releases for proprietary CoolMOS™ technology fabricated on 300mm by February 2013.

Infineon Technologies is partner in the EPT300 project [1] – "Enabling Power Technologies on 300 mm wafers" – an ENIAC Joint Undertaking. With the help of EPT300, a consortium of 23 Partners from the European semiconductor manufacturing and the European equipment & materials industries are the first worldwide with a 300 mm power semiconductor processing line dedicated to power device production, realizing leading edge manufacturing capabilities in Europe.

It is important to clearly distinguish power electronics fabrication from conventional CMOS manufacturing technology. Having very different product characteristics, power electronics require different materials and processes, which had not been realized on 300 mm wafers before. The current state-of-the-art in manufacturing power semiconductors (MOSFETs, IGBTs and power IC technologies) today relies worldwide on 150 mm and 200 mm wafer technology. Consequently, today's manufacturing equipment for such applications is specifically designed to these wafer diameters. Technologies dedicated to manufacturing power semiconductors on 300mm wafers require capabilities that in the recent past posed unresolved manufacturing challenges.

To overcome this limitation, the EPT300 project aimed to provide solutions to the following targets:

- Provide first MOSFET-products fabricated on 300 mm wafers in lead-fab environment in a 1:1 transfer approach to fully prove compliance with application requirements on new substrate material.
- Provide enhanced equipment and new process technologies.
- Prove manufacturability of these products in a high volume production environment with stable and acceptable yield figures.
- Set the technology base for future enhancements in power semiconductor technologies.

The production of power semiconductors is highly complex, involving many production steps requiring in-depth material knowledge and know-how. The first precondition is the availability of proper raw materials and production equipment. Given these, the first manufacturing steps deal with a series of steps in which the active area of the device is built up. Consequent steps are dedicated to semiconductor back-end production, which includes thin-layer metallization and a set of wafer backside process steps that are essential in manufacturing power semiconductors. One key process out of these is wafer thinning, since the thickness of a power device has significant influence on its performance. Infineon Technologies has been pioneering the field of thin wafer manufacturing mainly for its portfolio of IGBTs enabling e.g. the performance of its TRENCHSTOP IGBTs. However, wafer thinning will also be a performance boost for Low voltage MOSFETs and is being used in our CoolMOS technology.

Specific challenges on the way to 300mm manufacturing

In the first step to enable power technologies on 300mm wafers, existing 200mm technologies have to be "transferred". Nevertheless it is much more than a transfer, because no power base materials were available for 300 mm at project start. Also some equipment for power technologies was not available for 300 mm. In reality it was and still is a challenging R&D project and not a "transfer".

Therefore it is necessary to prove the 1:1 capabilities of transferred products which are already available on 200 mm. Identical or improved performance of the devices has to be proved.

Out of this, three major challenges are pointed out as a key for the development and production of power on 300mm wafer diameter:

1. Availability of power substrate on 300 mm at a cost efficient level (e.g. Infineon modification of p-type standard substrate, development of 300 mm power substrate by substrate suppliers)
2. Adaptation of 300mm CMOS equipment for power processes (e.g. front side- and back side processing and processing, thick layer processing, high temperature processing and of course thin wafer processing, processing on bridge tools)
3. Thin wafer technology for 300 mm power technologies (adaptations of Infineon's 200 mm thin wafer technology for 300 mm down to 40 µm, enabling 20 µm silicon thickness).

300 mm power substrate material challenges

Today, CMOS devices are routinely manufactured on 300 mm substrates, enabling better chip performance at lower costs. While the performance is driven by smaller feature size (<45 nm), the cost per device depends on chip size and wafer

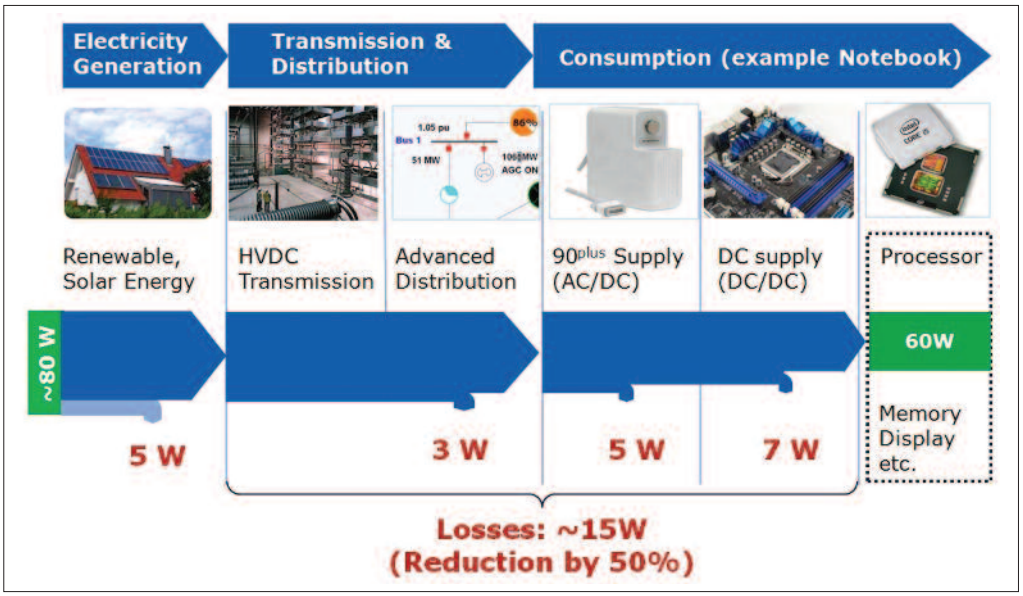

Figure 3: Power Semiconductors significantly reduce energy losses

diameter as well. Still, given the demand volume, the available substrate materials are optimized to the requirements of these CMOS technologies, and do not necessarily allow for the specific requirements of power technologies on the substrate material.

For CMOS-technologies, p-type substrates (mostly Boron) are in use, while power technologies require n-type (typically Phosphor-doping) substrates. Furthermore, the needed doping levels and device thicknesses depend strongly on the desired break down voltage, which created another technological gap that could be solved within the project.

In CMOS technologies, the only active electrical area is located on the surface, whereas in most power technologies the entire silicon volume is used as electric currents flow from top to bottom of the device. Contaminations and impurities in the substrate thus affect the properties of the devices in a much stronger way than CMOS structures.

Even now, dedicated raw materials for 200mm power technologies are far more expensive than standard materials for advanced CMOS processes. It is essential to find a cost efficient solution for the substrate to maintain the expected cost benefits out of the 300mm wafer diameter.

Equipment challenges

The bigger part of the semiconductor market is 300 mm CMOS technology down to 28 nm feature size for mass products like DRAMs, Flash memories or CPUs for PCs, notebooks and smart phones. At the same time, the rapidly growing potential of power technologies generates a demand that calls for the adoption of 300mm technology also for these devices. However, even though all mainstream equipment for the semiconductor production is now commercially available for 300 mm wafers, there are big differences between mainstream CMOS tools and the special equipment required in power technologies manufacturing.

Compared to CMOS processing the processing of energy efficient power semiconductor requires "3 dimensional processing" (front side processing, back side processing and processing vertically (trenches) in the silicon), thick layer processing, high temperature processing and of course thin wafer technology.

Infineon`s high voltage MOSFETs are based on the so-called Superjunction principle, a technology which allows to

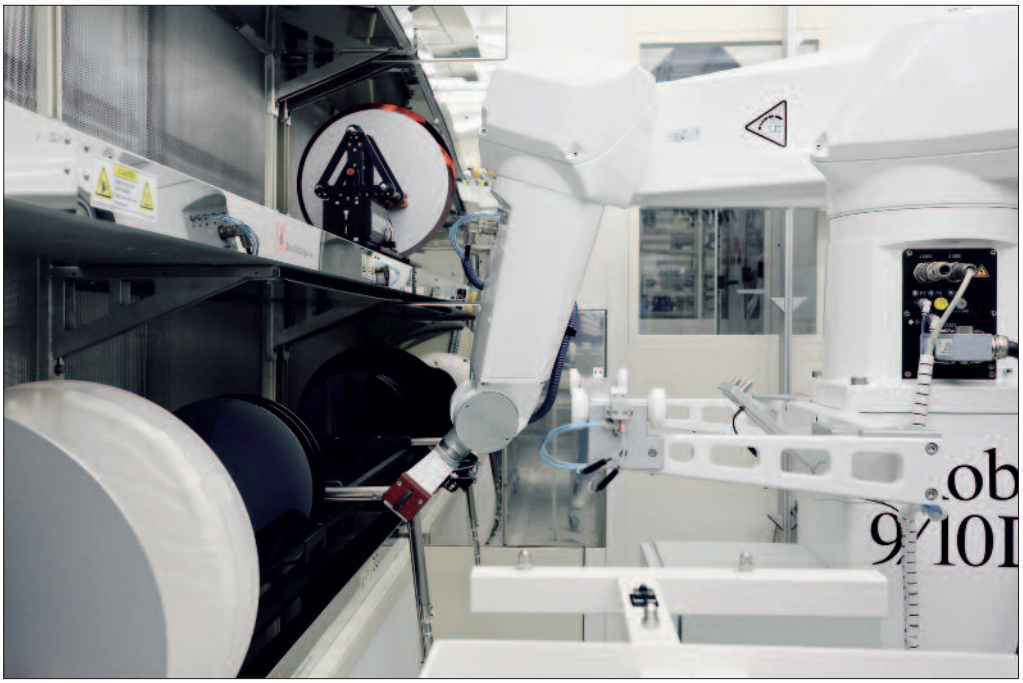

Figure 4: Flexible use of equipment processing 200 mm and 300 mm is crucial

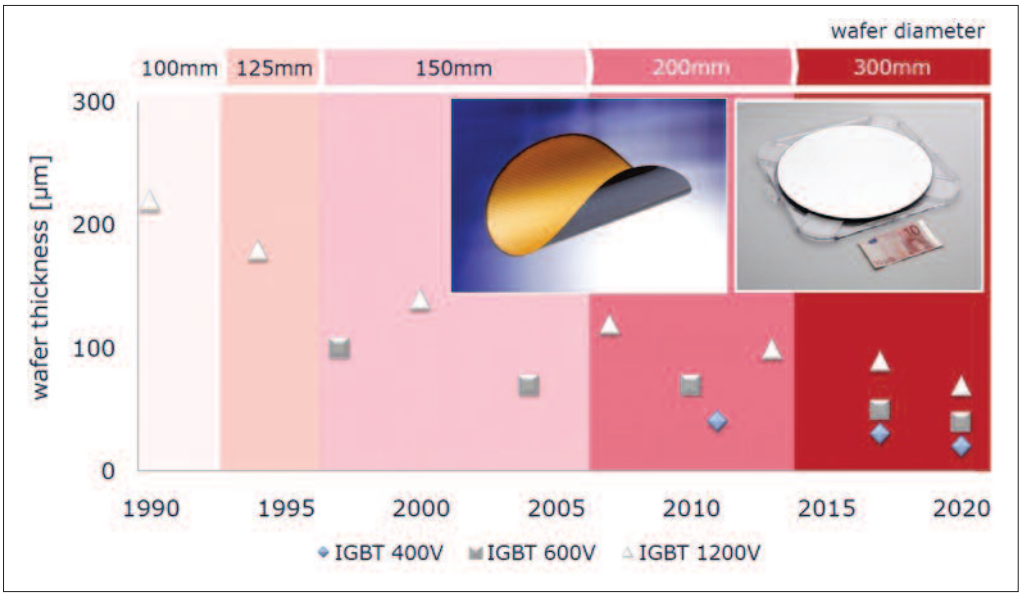

Figure 5: Target wafer thicknesses for IGBTs

drastically reduce the on-state resistance per chip area and to overcome the famous limit line of Silicon. While the on-state performance benefits from an ever higher doping level of the drift region the blocking voltage demands a perfect compensation of three-dimensionally structured p- and n-doped regions across each device, across the entire wafer, from wafer to wafer and from lot to lot. Significant effort is spent on in-line control methods and sophisticated equipment operation and maintenance respectively to successfully transfer the CoolMOS technologies to 300 mm.

Other challenges for power technologies are the high-temperature furnace processes. Standard equipment for 300 mm technologies is capable of processing at a maximum temperature of ~1000°C. Power technologies require temperatures up to ~1200°C. This leads to major research on the hardware of furnaces in order to comply with these challenging requirements. This includes the heating system and sophisticated temperature controllers as well as special, adapted quartz ware technologies.

The flexible use of equipment being capable to process 200 mm and 300 mm wafers (bridge tool) is a key to enable highly flexible and cost competitive manufacturing on European manufacturing sites. Another important aspect of these bridge tools is the possibility to have an identical 200 mm reference on the same equipment.

Thin wafer manufacturing challenges

As outlined above, power devices show vertical current flow, the load current flows from the front to the backside of the device. To optimize the performance the final thickness of a power device is essential. Infineon`s IGBT technology relies on extremely shallow p-doped backside implants to control accurately its emitter efficiency. In combination with a less shallow n-doped field-stop layer and the top side trench structure both the distribution of the electric field (and hence the blocking capability) as well as the carrier profile are precisely engineered. Any excess in device thickness would result both in an increase of the forward saturation voltage as well as the turn-off losses. Hence both key performance indicators of an IGBT would be compromised. Figure 5 shows the target wafer thicknesses for the coming years for the respective IGBT voltage classes.

State of the art wafer thickness for 150mm and 200mm wafers for power technologies is today 70 µm. This already implies a huge challenge in the handling of such thin wafers because of their fragility. Using 300 mm wafers will further increase this challenge, with the trend pointing towards further reductions in the thickness of the wafers. Ultimate wafer thicknesses may be as thin as 20 µm. Other technologies such as Infineon Low Voltage MOSFETs will benefit from the achievements in thin wafer handling to reduce both electrical on-state resistance and thermal resistivity of the remaining substrate thickness.

Conclusion

Infineon has shown the successful implementation of power MOSFET technologies on 300 mm wafer manufacturing. The challenges regarding availability of raw material as well as thin wafer manufacturing have been solved. Specific topics such as those posed for Superjunction devices and low voltage MOSFETs have been successfully demonstrated. These achievements will put Infineon Technologies into a pole position to sustainably deliver capacity into a market with ever increasing demand for power semiconductor devices.

[1] A part of the work has been performed in the project EPT300, co-funded by grants from Austria, Germany, The Netherlands, Italy and the ENIAC Joint Undertaking.