Progress in Silicon-Based 600 V Power GaN

The readiness of 600 V GaN-on-Si based power devices fabricated using the GaNpowIR® technology platform for large scale production is presented in this article. The advantages of such devices over the Silicon incumbent alternatives in several common power conversion application circuits is also shown.

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It has been well documented that the advent of high voltage GaN based power devices provides unprecedented opportunities to reduce both conduction (R_{dson}) and switching losses (Q_{sw}) in a wide variety of power conversion circuits. The combination of hetero-epitaxy using Silicon substrates and device fabrication along side Silicon CMOS products in high volume factories provides the necessary cost structure to compete commercially with Silicon based alternatives.

The capability to grow thick crack free AlxGayN alloys on standard thickness Silicon substrates in manufacturing volumes has often been underestimated either as an essential element to commercialization of GaN based power devices or as a significant technological hurdle when moving from non-commercially viable substrates such as SiC. In the ranking of required capabilities to successfully compete in the commercialization of GaN based power devices, such capability, together with supporting intellectual property should be considered the most important. As such, IR has previously demonstrated the manufacturability of up to 5 µm thick AlxGayN epitaxy on standard thickness 150 mm Si substrates. In addition, Figure 1 shows the manufacturability of low distortion crack-free GaN on Si epitaxy for 2.25 µm thick films on standard thickness (725 µm) 200 mm diameter Silicon substrates.

The use of such substrates is essential to achieve commercial viability of the technology platform. These results are made possible through the use of IR's proprietary compositionally graded transition layer III-N on Si epitaxial technology. Another essential requirement for commercialization is the ability to produce devices alongside the incumbent high volume silicon based power devices. In addition to the use of standard photolithographic and plasma and wet chemical process technologies, this requires the elimination of Gold based ohmic contacts. In this regard, IR was the first to reproducibly demonstrate sufficiently low ohmic contact resistances (< 0.35 ohm-mm) in volume production.

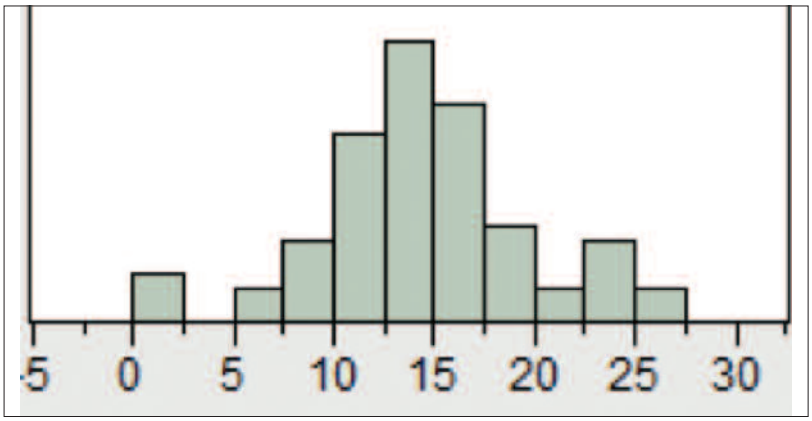

Figure 1: Measured distribution of final wafer bow for over 20 multi-wafer process runs producing more than 60 crack free 2.25 µm thick AlGaN alloys based hetero-epitaxy on 200 mm standard thickness (725 µm) Silicon substrate

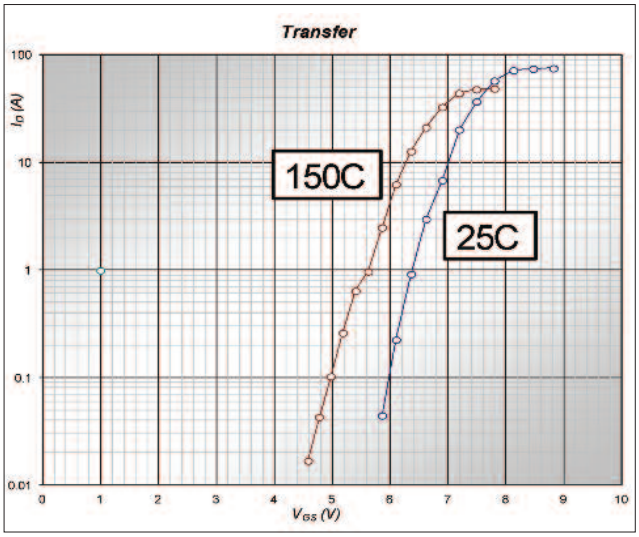

Figure 2: Measured transfer characteristics of a 600 V rated GaN-on-Si based HEMT with an active area of 8 mm? and a gate width of 330 mm, cascoded with a low voltage Silicon FET, in a dual sided cooled package, at room temperature and 150°C

Enhancement mode not required

Further, it is often stated that development of an enhancement mode GaN based high electron mobility transistor (HEMT) is an essential element of commercialization. This is not a valid assertion. Besides the opportunity to use depletion mode, normally-on devices in a majority of power electronic circuits (using DC enable switch based topologies), several topologies such as AC/AC converters used for motor drive actually are superior when implemented with the inherently bi-directional capable depletion mode GaN based HEMT devices, In addition, the inherent instability of the two dimensional electron gas (2DEG) to positive applied fields which collapse the built in barrier potential of the AlGaN barrier layer (in AlGaN-GaN HEMTs) presents a severe crippling restriction of gate drive to

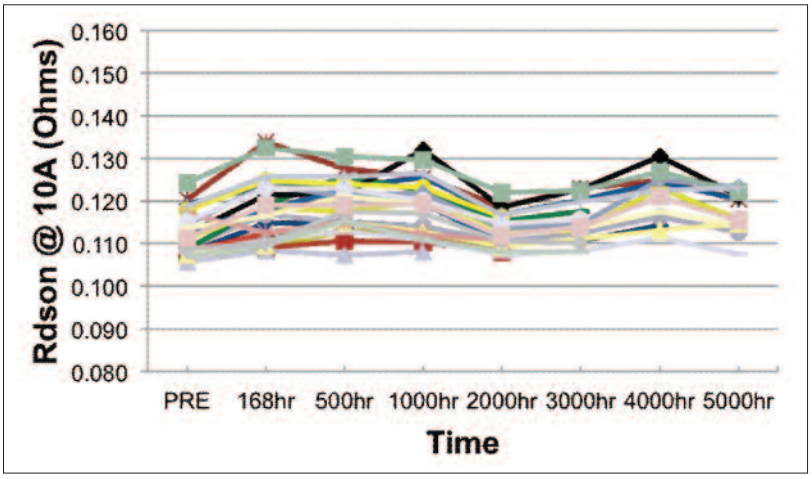

Figure 3: Source-drain resistance of 600 V rated cascode switch for a population of representative cascoded GaN-on-Si based HEMT devices with W_g = 120 mm, under a drain bias of 480 V and 0 V gate bias for 5000 hrs at 150°C

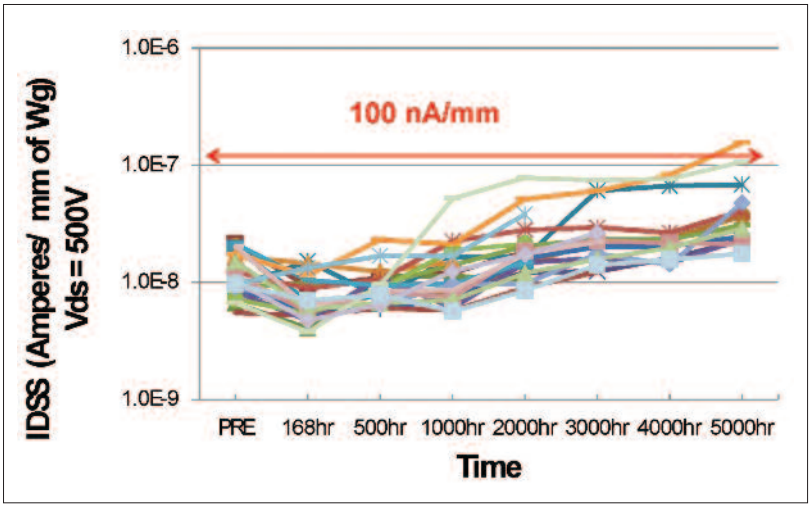

Figure 4: Source to drain leakage current measured with 500 V drain bias and 0 V gate bias of 600 V rated cascode switch for a population of representative cascaded GaN-on-Si based HEMT devices with W_g = 120 mm, under a drain bias of 480 V and 0 V gate bias for 5000 hrs at 150°C

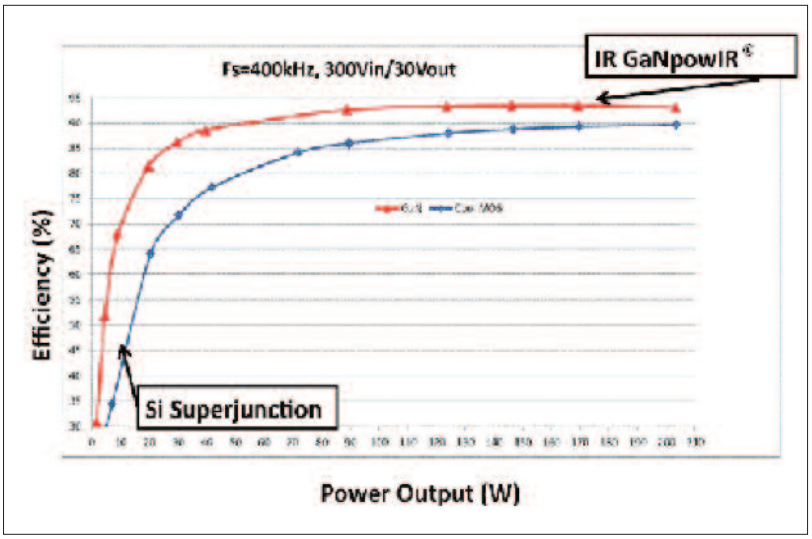

Figure 5: Measured conversion efficiency for a resonant LLC converter with 300 V input and 30 V output voltage operating at 400 kHz, using either IR's GaNpowIR® based devices on both the primary (600 V rated) and secondary side (100 V rated) of the transformer (with synchronous secondary side rectification) or state-of-the-art Silicon alternatives

any enhancement mode barrier based 2DEG device, through the limitation of applied overdrive gate voltage above threshold.

Of course, the addition of voltage clamps, e.g. in intimately coupled gate drive circuitry, can be used at the expense of increased effective gate capacitance, leakage currents and cost. Therefore, in the cases where normally-off behavior is preferred, the cascoded configuration, using a low voltage MOSFET, is recommended. In addition to providing a well established and reliable gate drive interface for external circuits, this approach has many advantages not found in an enhancement mode GaN based power device. When properly configured, one such advantage is the effective HEMT gate drive current capability afforded by the milli-ohm level low voltage cascode device on-resistance, compared to 0.2 to 1 Ω resistance found in commercial driver ICs.

In addition, the effective overdrive capability of the cascoded HEMT is the voltage between V_{pinch} and ground, often about 6-12 V. This is compared to the 2-4 V of overdrive available to a standard clamped enhancement mode GaN based HEMT. This internal gate drive configuration maintains the HEMT gate in the optimal voltage range of $-V_a$ to ground, where V_a is limited by the avalanche clamped breakdown voltage of the low voltage MOSFET. In addition to improved power device performance, the cascode based gate drive configuration reduces hot carrier induced degradation through beneficial barrier potential between the 2DEG and the gate structure, as opposed to the decreased barrier inherent to positive voltage HEMT gate overdrive.

Circuit performance and reliability

In addition to inherent and revolutionary integratability, the lateral GaN based (HEMTs) exhibit advantages of significantly lower terminal capacitances, several times lower specific source-drain resistance and essentially zero reverse recovery charge compared to either Silicon based Superjunction FETs or IGBT alternatives. It is shown that the often feared current handling capability limitation associated with the lateral nature of the HEMTs can be effectively addressed through the use of front side solderable devices and dual sided surface mount packaging techniques. Current handling densities of more than 500 A / cm² at 150°C are demonstrated with 600 V rated devices capable of processing more than 80 A at room temperature. Figure 2 shows the measured normally-off transfer characteristics for such a device, in a cascaded configuration with a low voltage Silicon FET.

The establishment of simultaneous long-

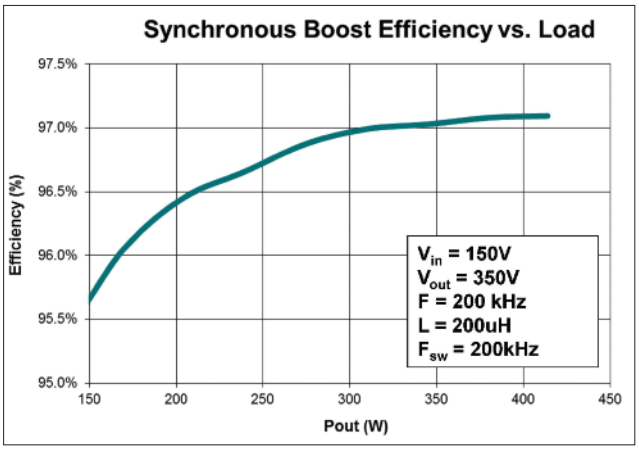

Figure 6: Measured conversion efficiency for synchronous boost power factor correction front end of an AC/DC converter using GaNpowIR® based devices for both switches

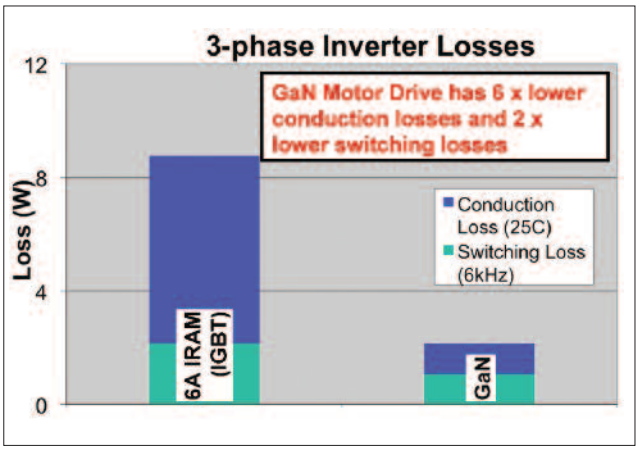

Figure 7: Measured conversion efficiency for nominally 500 W motor drive inverter using either GaNpowIR based devices or IGBTs (I_c = 1.5 A, V_{bus} = 300 V, V_{out} = 160 V, P_{out} = 415 W, T_c = 150°C)

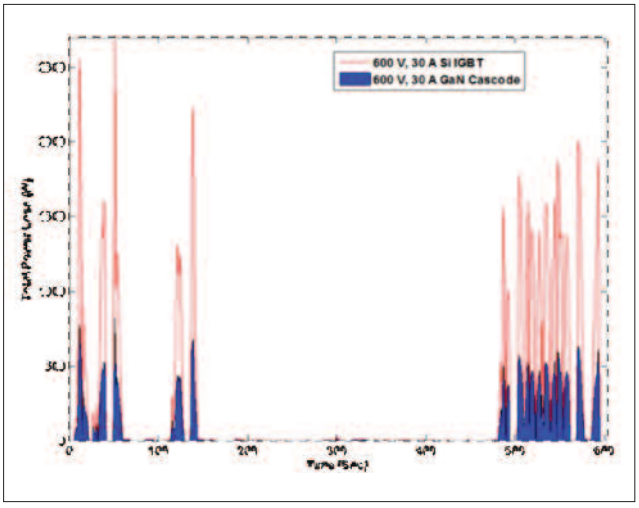

Figure 8: Modeled inverter power loss over the system power processing model for electric propulsion US-06, for a nominally 60 kW motor drive inverter, comparing the expected performance based on device and circuit models for Si IGBTs and diodes and 600 V rated GaNpowIR cascoded switches

term reliability and device robustness RBSOA (including dynamic R_{dson} effects) and FBSOA in application conditions is essential for the adoption of any power device technology. Figures 3 and 4 show some early results demonstrating exemplary stability for such devices under 480 V drain to source reverse bias stress for 5000 hours.

Application performance

These 600 V rated GaN-on-Si based devices have been tested in several widely used power conversion topologies. Figure 5 shows the improved conversion efficiency for a 300 V to 30 V LLC resonant converter operating at 400 kHz, exhibiting remarkably improved efficiency (> 17 %) at light loads and > 3 % improvement at full load conditions. Figure 6 shows the performance of a GaN based synchronous boost converter for application in a power factor correction front end of an AC/DC converter. Though the replacement of the boost diode with a GaN based power device in a synchronous boost converter circuit was first presented in the issued US patent number 7276883, filed in August 2004 assigned to IR, only now are the requisite 600 V devices available to make this circuit commercially available. Note that such a circuit would be impractically expensive if implemented with SiC MOSFETs or JFETs.

One of the most wide-spread applications for 600 V rated devices is in the inverter drive circuitry for motors. It is therefore important to assess the value provided by GaN based power devices in motor drive applications. Two of the largest potential volume applications are appliances and electric or hybrid electric vehicles. Figure 7 shows the drastic improvement in power loss in a nominally 400 W motor drive inverter circuit, using IGBTs and first generation 600 V GaN cascoded switches. As can be seen the conduction losses are reduced by a factor of 6, while at the same time the switching losses are reduced by a factor of 2. This remarkable result is based on the 4-10 x improvement in the V_{ceon} x E_{sw} (or R_{dson} x Q_{sw}) improvement in the performance figure of merit (FOM) of the GaN based devices over the Silicon based IGBTs previously reported. Such improvements in power handling capability allow for the related increase in the inverter power density of a factor of more than 10. In this instance, taking into account that the GaN based inverter does not require the heat sink of the IGBT-based inverter, the power processing volume density is actually increased by more than 100. Such improvements in power processing efficiency and density are examples of the potential of GaN based power devices to transform power electronics.

Another example is shown in Figure 8 for a nominally 60 kW inverter drive for an electric vehicle propulsion system. This work was the result of cooperation between International Rectifier, Delphi Automotive Systems and Oak Ridge National Laboratory, funded through a grant by US Department of Energy through ARPA-e. As can be seen the modeled performance of a state-of-the-art Silicon based inverter is compared to that of a GaNpowIR based inverter using a simulated drive cycle/power schedule known as US-06. The results are based on the extracted device models of measured high current devices, such as those shown in Figure 2 and leveraging the performance of dual sided cooled packaging developed at Delphi known as VIPER. The GaN based inverter exhibits an approximately 50 % reduction in power loss with a coolant temperature of 105°C.

Literature

"The Status of 600 V GaN on Si based Power Device Development at International Rectifier", PEE Special Session Power GaN for Highly Efficient Converters, PCIM Europe 2013, Nuremberg