GaN Switching for Efficient Converters

GaN transistor switching speeds of 50 V per nanosecond and two orders of magnitude improvement in specific on-resistance over Silicon devices improve volumetric and conversion efficiency in any power systems and has particular relevance to solar boost converters. GaN Systems novel switch topology maximizes these advantages whilst reducing cost of manufacture. By designing CMOS integrated driver solutions upon which the GaN die is mounted directly in a stacked chip assembly – combining the switch, its driver, sensors and customized interface circuitry – helps to ease design-in these new devices.

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GaN Systems novel switch is formed from a sea of source and drain islands with a common gate region running between them (see Figure 1). This results in up to four times reduction in the die area occupied by a transistor of given on-resistance and simplifies the semiconductor processing required, thereby minimizing manufacturing cost. In addition high breakdown voltages, in excess of 1200 V, can be achieved with this topology. The current in each source island flows directly from the die through a copper post into the interconnect pattern on the surface to which the die is mounted. Initially produced using GaN on SiC processes, these devices are now migrating to GaN on Silicon.

Each drain island is connected by a through-substrate-via to a common connection pad on the back of the die. In this way no large current flows in on-chip metallization allowing high currents to be switched without danger of electro-migration. The construction allows flip chip assembly of the die eliminating the need for bond wires (see Figure 2). Conventional bonds represent significant inductance that contribute to high frequency switching transients and power loss in designs that take maximum benefit from switching speeds of the order of 50 V/ns.

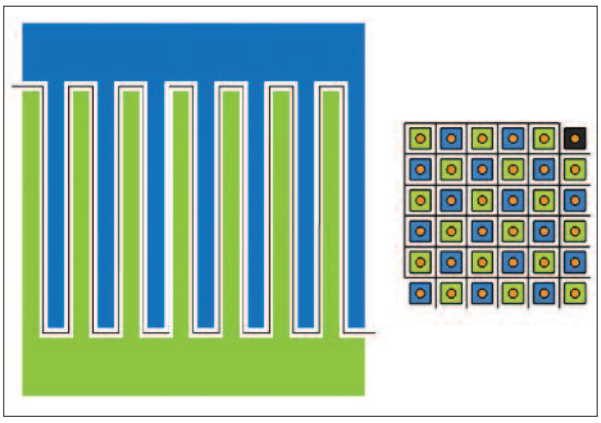


Figure 1: **Compared to the traditional FET finger structure the GaN Systems switch is formed from a sea of source and drain islands with a common gate region running between them**

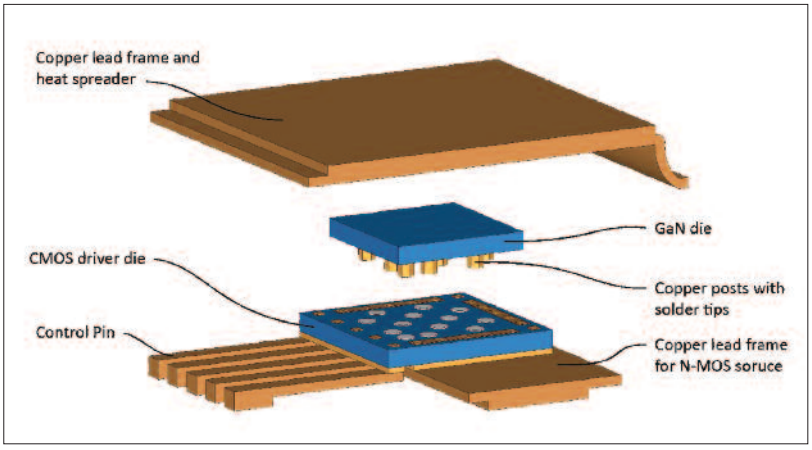


Figure 2: **Flip-chip assembly eliminating the need for bond wires**

Normally-off via cascode

Whilst processes are emerging that allow normally-off switching action using Island designs, the resulting degradation of on-resistance of these devices over equivalent normally-on solutions favors the adoption of the latter in high power applications.

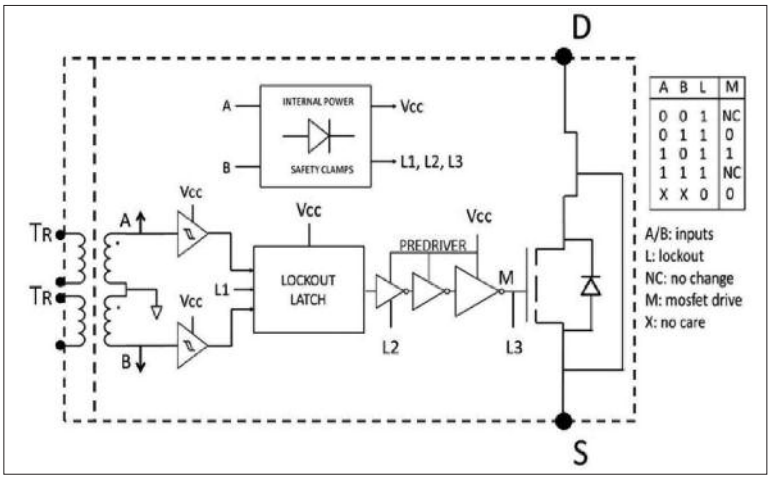
The inclusion of a cascode connected low voltage MOSFET switch in the source connection of the GaN device provides an equivalent normally-off switching action. To facilitate simple application of the switch in practical applications, the GaN switch can be directly mounted onto the drain pad of a low on resistance, low voltage NMOS transistor forming a chip-on-chip CMOS / GaN stack that represents a normally-off structure.

The NMOS transistor is integral to a CMOS driver chip that provides sensing of gate voltage and temperature of the switch and is able to control the slew rate of the GaN switch. First iterations of this switch and driver combination include differential inputs, and a Schmitt trigger. The circuit can be driven by a logic input or even a pulse transformer to facilitate galvanic isolation (Figure 3).

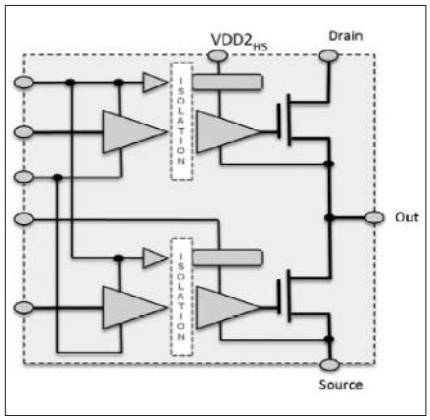
Future developments are planned that will include high voltage isolation within the driver chip using a SOS process. Adding multiple GaN switches then offers the prospect of forming complete half and full bridge isolated switch configurations (Figure 4).

Thermal issues to be solved

Although the GaN die is thinned to 100 microns, thermal resistance remains a concern. Heat removal from the GaN die is



ABOVE Figure 3: **Block diagram of integrated driver / GaN switch**



ABOVE Figure 4: **A future isolated half bridge function using multiple GaN switch die and a SOS driver stack**

achieved separately from the heat that is generated by the MOSFET. This approach is needed to allow the MOSFET to remain within its temperature range. Therefore packaging issues were a prime concern during the design process.

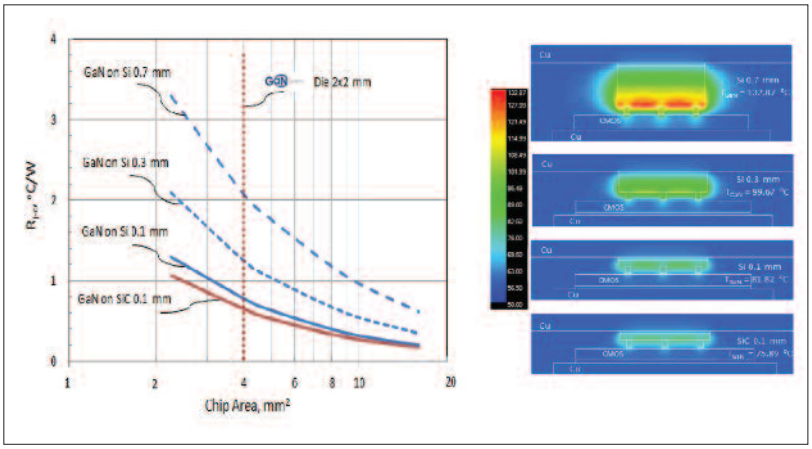
Because the GaN transistor has ten times the on-resistance of the low voltage MOSFET it is vital to achieve effective heat removal from the surface of the GaN device. Although there are 12 plus 1 copper posts mounted on the surface of the GaN transistor, more than 90 % of the heat is actually dissipated via the substructure of the GaN transistor. Currently most GaN transistors produced are built on SiC or Si substrates. GaN on Si devices produced using thick Si substrates are less prone to warp issues but the thermal resistance is problematic. However, if the Si substrates can be thinned to 0.1 mm, the thermal resistance of the SiC and the Si substrates are similar. The graphs shown in Figure 5 were drawn for the example where the GaN device dissipates 40 W and CMOS device dissipates 4 W. The upper and lower heat spreaders are held at 50°C. The combined devices (2 mm x 2 mm GaN and 4 mm x4 mm CMOS) are mounted in an equivalent PQFN structure outlined in the thermal cross section.

Electrical performance

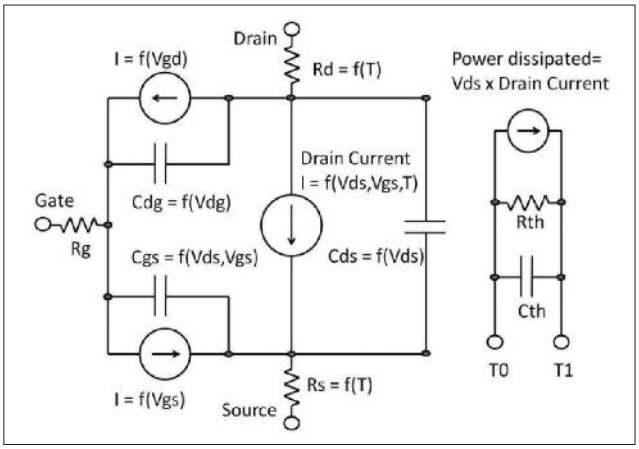
The CMOS circuit was designed to conform to the design rules of a conventional 1 micron CMOS fabrication foundry. SPICE models were supplied by the CMOS foundry and a SPICE model was developed for the GaN transistor. Particular care was taken to include within the GaN model a thermal network that includes several elements that enable the on-resistance and saturation current to dynamically track active area temperature. The model includes the thermal resistance of the GaN transistor and it also allows the user to include the package thermal resistance (Figure 6).

Keeping the model compact, and restricting it to a small number of nodes, allows for quick convergence in highly non-linear simulations such as power switching transients. In order to populate the model parameters with appropriate values, the GaN device has been characterized using pulsed IV and CV measurements over bias and temperature.

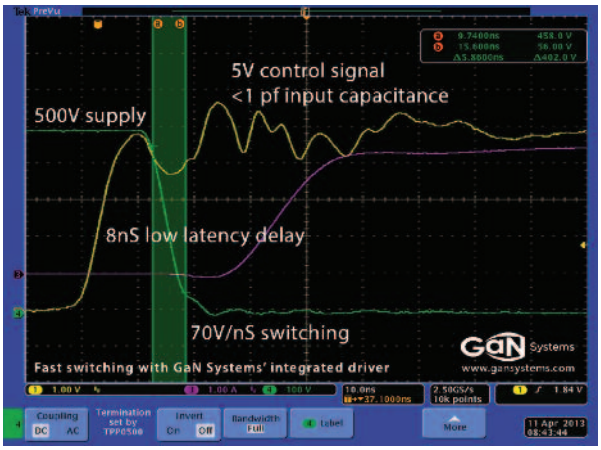
Consideration was given to process corners and statistical variations. Systematic verification of the device behavior under various modes of operation, including power switching load lines, completes the modeling process. Co-simulating the transient response of the GaN transistor with the CMOS driver and the package parasitics provides a realistic prediction of the electrical and thermal performance of the device in a power switching application. The CMOS / GaN hybrid was designed to be capable of being driven by an isolating pulse transformer. Galvanic isolation allows for the device to be used in the upper section of a half bridge. This isolation, if

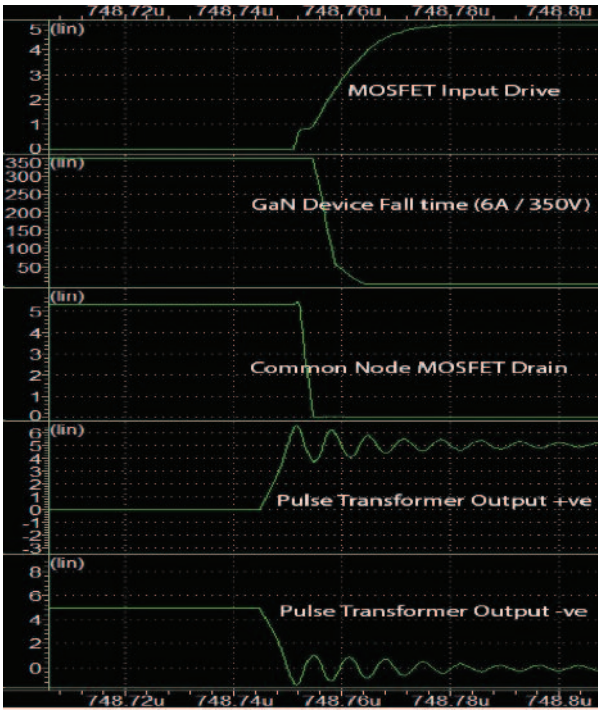


ABOVE Figure 5: **Thermal resistance and surface temperature of GaN devices**



LEFT Figure 6: **Block diagram illustrating the elements used in the electro-thermal non-linear model developed for the GaN HEMT**





ABOVE & RIGHT Figure 7: Simulated and measured results including an isolation pulse transformer (above), CMOS circuit and GaN transistor

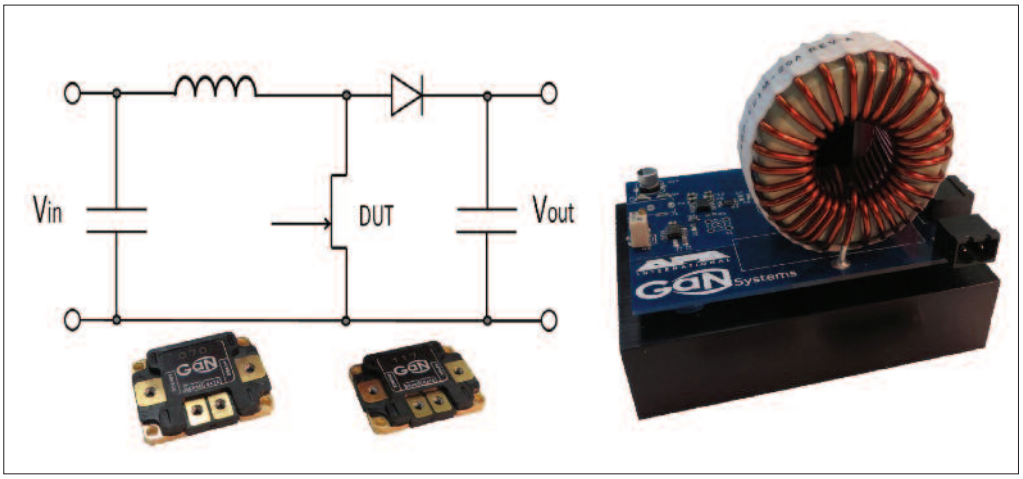
achieved at low cost can also be used to alleviate ground loop problems that may occur when driving the lower section. The simulated results include the pulse transformer SPICE model.

The delay from the rise of the input to the Schmitt circuit to the MOSFET turning-on is less than 5 ns. The GaN transistor is fully on within 15 ns of the input signals reaching the trigger levels of the Schmitt circuits. The input capacitance of the Schmitt circuits is less than 1 pf (Figure 7).

The GaN transistor and CMOS circuit were assembled in a prototype PQFN package. Given a resistive load of 60 Ω the 1200 V GaN transistor cascoded with the CMOS / MOSFET is able to achieve a 350 V transition within 10 ns. The delay from the pre-driver transition to the completed output swing is less than 15 ns. The overall delay time from the output of the isolating pulse transformer is approximately 20 ns – the CMOS circuit having added 5 ns as shown in the screen shot of Figure 7 (right).

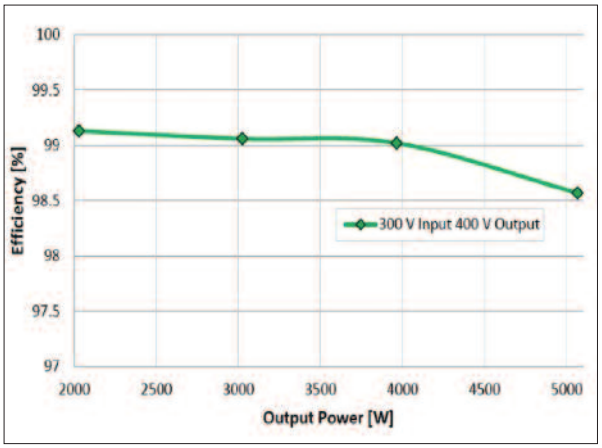
PV boost converter performance

The typical operating points for the Photo Voltaic (PV) string using central maximum power point (MPP) tracking can be between 150 and 350V. A simplified schematic of the test circuit used to evaluate the performance of the GaN transistor, the PQFN GaN transistor and CMOS circuit, and the realized converter are shown in Figure 8.



LEFT Figure 8: Basic schematic, PQFN GaN semiconductors, and realized PV boost converter

The converter was tested under two operating voltage conditions. First, a 200 V input was applied and a 400 V output was established. The output power was then swept from 750 W to 2 kW. The system maintained an efficiency of greater than 98.2 % over the entire operating range. Since there is so little loss in the converter power stage, only passive air cooling is necessary. Another series of tests were conducted where a 300 V input was applied and a 400 V output was established. Here, the output power was



LEFT Figure 9: Boost converter efficiency from 2 kW to 5 kW output power

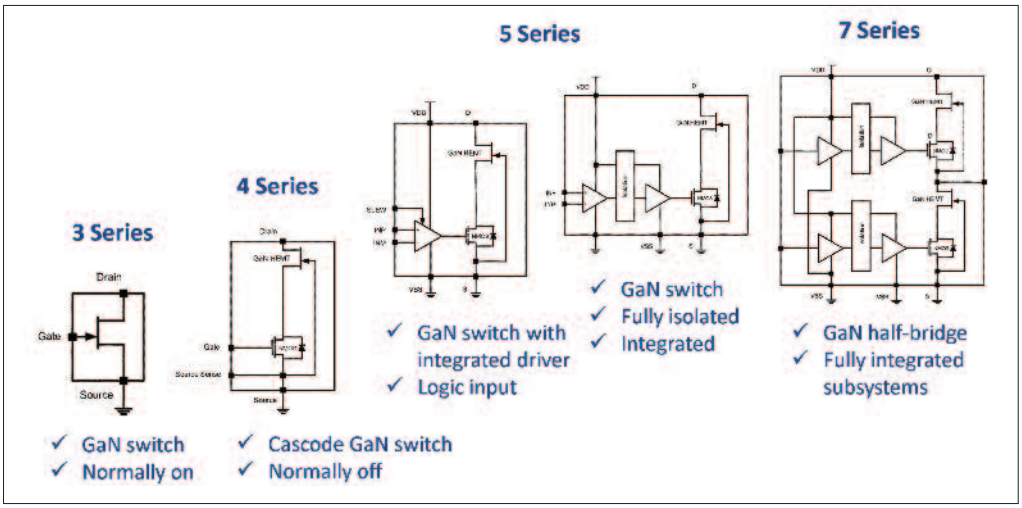


Figure 10: GaN Systems roadmap

swept from 2 kW to 5 kW. The system maintains over 99 % efficiency from 2 kW to 4 kW, and then dips slightly to 98.5 % at 5 kW (Figure 9). The converter has an approximate mass of 487 grams which equates to a gravimetric power density of approximately 10 kW/kg.

Figure 10 shows the roadmap, from individual GaN switches to fully integrated subsystems.

Conclusion

The described combinations of GaN switches and CMOS or SOS custom driver devices serve to accelerate the adoption of the advantages of GaN switches into power conversion and control systems by providing the system designer with a single device that is easily driven from logic signals. The inclusion of feedback from on-chip sensors and the ability to control switching slew rate open the prospect of tailoring the switch performance for given applications. In solar applications the high voltage operation, embedded galvanic isolation and high speed operation of these devices offer the prospect of higher switching speeds with improved conversion efficiency, lower component count, smaller size and reduced conversion loss.

Literature

"Development of Gallium Nitride Switches for Efficient Converters", PEE Special Session Power GaN for Highly Efficient Converters, PCIM Europe 2013, Nuremberg