New Thermal Design Options Drive Power Density

With every generation, electronic products shrink while functionality expands and performance improves. Despite efforts to hold the line on product power dissipation, pressure to increase power density in energy-management subsystems continues unabated. This trend, unfortunately, exacerbates the challenging thermal design task product development teams already face. A new packaging approach delivers more power in reduced space. **Gary Gill, Director VI Chip Product Line, Vicor, USA**

Heat from power components causes several problems - underperforming thermal designs result in high operating temperatures, which can reduce power-component reliability and, in dense applications, reliability of other nearby devices. In high-temperature environments, power derating reduces the amount of current a power component can deliver - a trait that can force system designs to be larger, heavier, and more expensive. Thermal designs that are inefficient near heat generating components - be they in the power-sourcing components or power loads - can force design changes elsewhere in the system. These include increased airflow requirements to maintain dissipative devices within their safe operating temperature range. Increasing a cooling system's airflow requirement also increases its energy use, increasing the system's operating costs.

Minimizing heat generation

The first line of defense, then, is to minimize heat generation throughout the power subsystem design. Minimize I?R losses, starting at the power entry point. For example, 400-VDC power distribution in data centers reduces copper losses in power feeds by a factor of 69 below those of 48-V distribution systems for the same size copper feeds. Smaller power savings are available with smaller feed dimensions, allowing system designers to split the savings between a system's acquisition and operating costs. 270-VDC distribution provides similar benefits in airborne systems.

Efficient power-subsystem designs minimize the number of conversion stages from power entry to point of load. They also take advantage of highly efficient power-conversion topologies. These include ZVS (zero-voltage switching) and ZCS (zero-current switching).

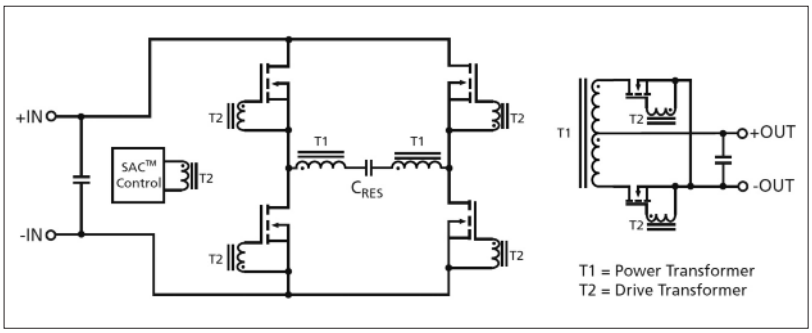
Minimizing the number of conversion stages while efficiently accommodating high power-entry voltages challenges traditional converter designs. Fortunately, high voltage-ratio applications have inspired alternative power architectures and conversion topologies.

A SAC™ (Sine Amplitude Converter [1]) illustrates architectures that can provide high voltage-ratio conversion, high efficiency, and low output ripple (Figure 1). For example, Vicor's VTM implementation of the SAC topology can provide fixed voltage ratios between 1:1 and 40:1 allowing single-stage 48- to 1.2-V conversion for POL applications at up to 98 % efficiency.

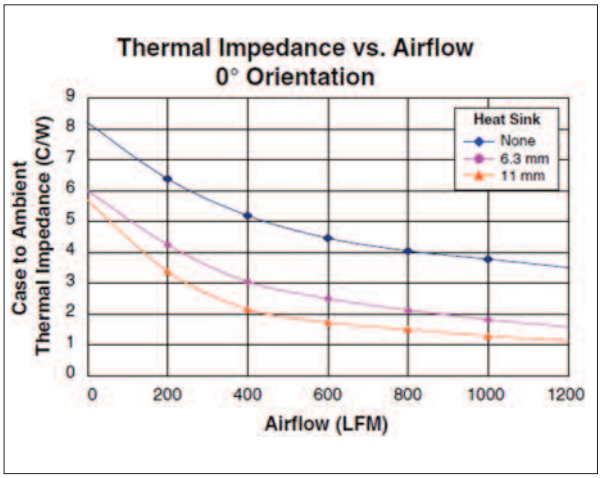
This approach reduces output ripple by about 1/3, substantially reduces the noise energy at harmonics of the switching frequency, and provides about five times faster load-step response than traditional topologies. Such performance reduces the need for output bulk capacitance, it also allows for a tighter circuit-board layout, which helps reduce I^2R losses in the highest current section of the power subsystem - the point of load. Overall, taking advantage of such technologies can reduce heat-generating conversion losses by as much as 40 % compared to traditional power-conversion schemes.

Improving thermal design

No matter how efficiently your power



ABOVE Figure 1: A SAC™ (Sine Amplitude Converter) is a resonant topology that switches its power MOSFETS at fixed frequency at zero-crossing points. The topology reduces power dissipation and high-order harmonics



LEFT Figure 2: Heatsinks reduce case to ambient thermal impedance, shown here as a function of airflow over a representative encapsulated power module

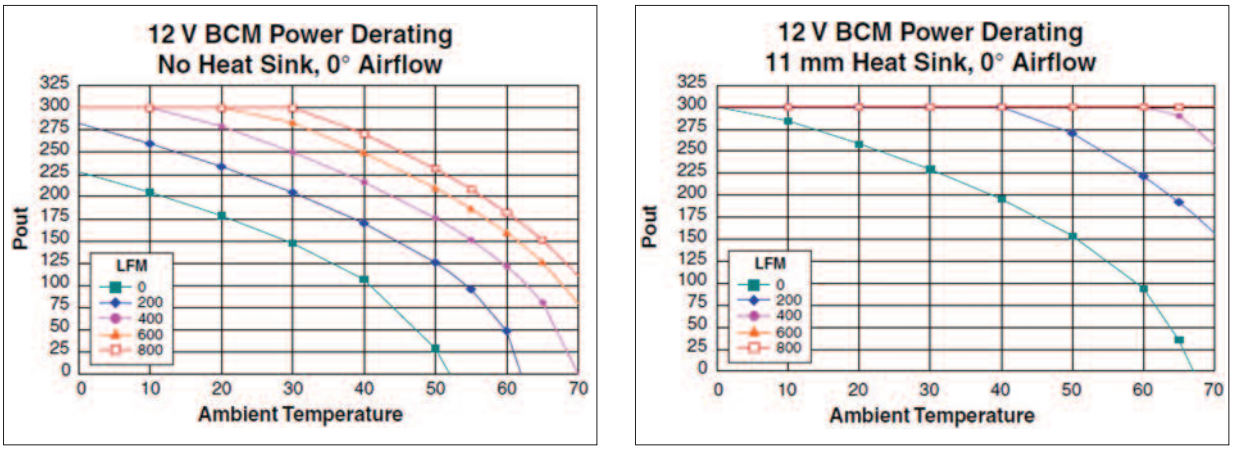


Figure 3: Derating curves, such as these for a Vicor 12-V BCM show the effect of airflow on realizable power capacity in designs with no heat sink (left) and with an 11-mm heat sink (right)

subsystem delivers energy, the residual dissipation and your ability to remove heat from the system limits power density. Once generated, there are two basic methods of removing heat from the power subsystem: convection and conduction.

The effectiveness of convection cooling - blowing air across the device's top surface - is a function of inlet air temperature, air flow rate, air flow impedances or disruptions, and the device's case temperature. Conduction cooling depends on a thermo-mechanical connection to draw heat from a high-temperature region to a cooler one. Its effectiveness derives from the device temperature, heat sink size and material, the thermal interface material and thickness, and the cool-region temperature (Figure 2).

For devices that use heat sinks contained within the system chassis, cooling is ultimately a two-stage process: conduction from device to heat sink and convection from heat sink to ambient. Thermal calculations must consider both stages. Some power-converter manufacturers mitigate this issue by providing heat sinks or references to commercial suppliers' catalog parts.

Design-support tools can range from simple tables and charts to sophisticated simulation software. Manufacturer's thermal-performance graphs can provide quick and useful insight into a power component's performance under a variety of configurations and operating conditions. Derating curves for no-heat-sink operation (Figure 3 left) and for operation with manufacturer-specified heat sinks (Figure 3 right) allow to align thermal and electrical designs. They help coordinate these two aspects of product's performance at the very start of the design cycle and give the electrical- and thermo-mechanical-designers important data with which to balance design trade-offs.

General-purpose tools, such as FEA (finite-elements array) analyzers, can model and simulate virtually any configuration and thermal design. But FEA tools tend to be expensive and require specialized knowledge to use effectively. Product-centric analysis tools, by contrast, are often free of charge and take mere minutes to learn.

The trade-off is that these tools are usually specific to a particular manufacturer's product lines and may limit the thermo-mechanical configurations which can be simulated. This restriction, however, has a silver lining: by limiting the thermo-mechanical design, the manufacturer-supplied simulation tools can guide the user to those that the manufacturer has developed and proven effective, potentially saving a substantial fraction of the thermal-design schedule and engineering costs.

One example of such simulation tools is Vicor's PowerBench™ simulator, which provides seven simulation types: VIN startup, EN (enable) startup, EN shutdown, V_{IN} step, load step, steady state, and thermal. The Power Bench simulation environment provides an application circuit with user settable operating conditions for source and load and adjustable parameters for input- and output-circuit components (Figure 4). The thermal simulation shown provides means to select between designs using a 6.3-mm or 11-mm heat sink or a cold plate. The ambient temperature, circuit board temperature, air velocity, interface thickness, and interface conductivity can also be set. Among the output data the thermal simulation provides are the output power, power loss, efficiency, heat loss through the case, heat loss through the circuit board, and device operating temperature.

The simulation results from Figure 4 report that the circuit delivers 326 W to its load with an efficiency of 95.54 %, resulting in 15.21 W of power loss. The simulation calculates the power

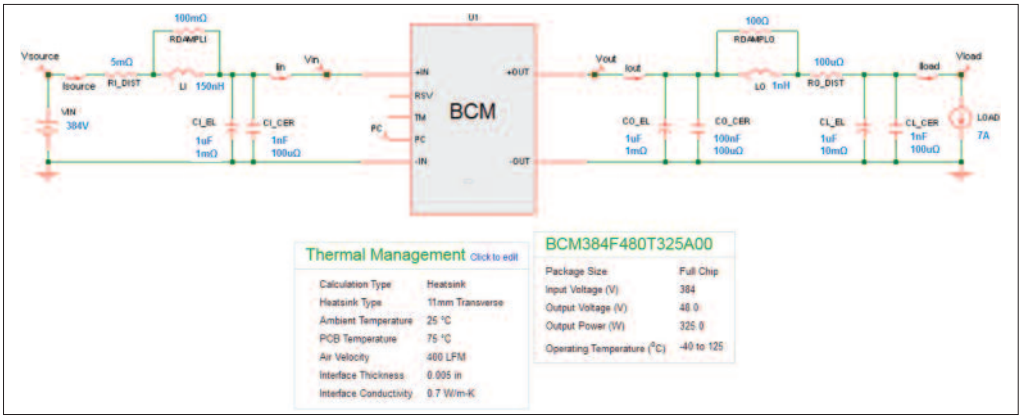


Figure 4: Vicor's Power Bench™ simulator is a powerful online design-support tool that includes thermal simulation among its seven simulation types

component's operating temperature under the stated conditions at 80°C - only 5 K warmer than the circuit board, indicative of the power converter's high efficiency and the heat sink's efficacy.

Power packaging

Most components, and certainly most power-dissipating components, within power conversion modules mount to the top side of the converter module's PCB. For simplicity, most product designs cool power modules and power ICs through their top surfaces.

There are, however, multiple heat sinking paths available. As product requirements drive power densities higher, thermal designs more sophisticated than simple topside cooling take advantage of other options.

In many power-converter structures, the majority of dissipated energy comes from power MOSFETs and power-carrying electromagnetic components. Fortunately, these parts usually connect directly to the pins that form the device's electrical and mechanical interfaces to the application PCB. The same pins can conduct heat out of a power converter's package if the underlying PCB design provides appropriate thermal features.

Through-hole mounting is more efficient than surface mount for heat conduction through the power package's pins, but both technologies can contribute to the product's thermal performance. The PCB's design must account for the additional heat from the power devices and the proximity of those devices to other dissipative components, such as processors.

New power packaging technologies and materials allow OEM designers to depart from topside dominant cooling. Power-train designs that arrange dissipative components symmetrically on both sides of a module's PCB coupled with highly thermally conductive packaging materials allow substantial cooling through the package's top and bottom surfaces. Additionally, this arrangement can shrink the module's layout, increasing power density while increasing efficiency by reducing I^2R losses in the interconnecting copper traces.

One example of packaging currently available for two-sided cooling is Vicor's new ChiP (Converter housed in Package) technology, which presents similar thermal resistances through top and bottom surfaces. ChiP packaging supports power-management functions such as AC/DC conversion with PFC (power-factor correction); isolated bus conversion; DC/DC conversion; buck, boost, and buck-boost regulation; and PoL current multiplication (Figure 5).

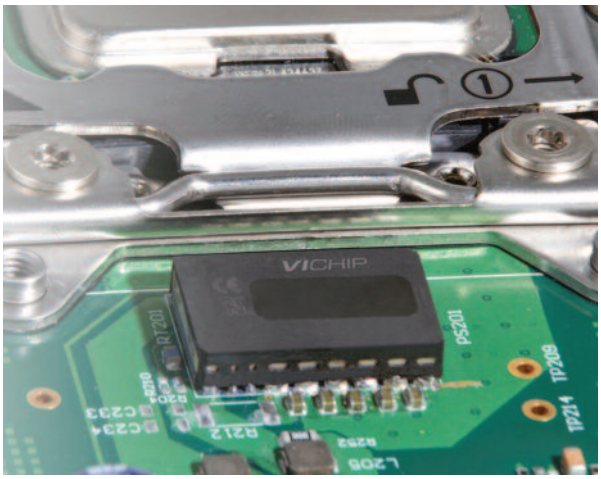


Figure 5: A 1323 size VTM current multiplier ChiP supports a tight layout, supplying a processor directly from a 48-V bus with no PoL bulk capacitors

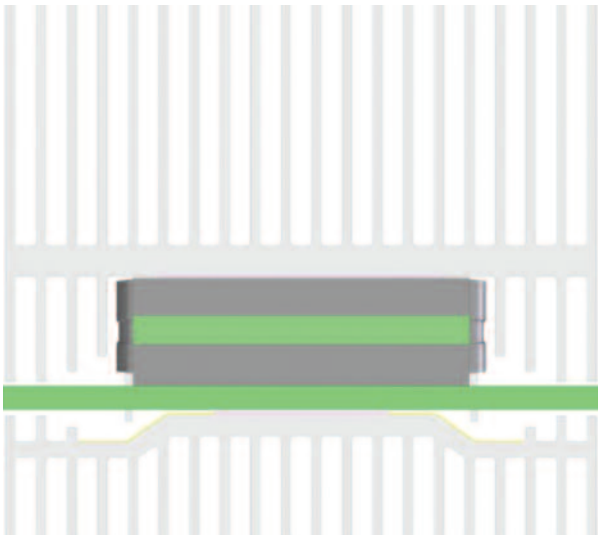


Figure 6: A thermal management cell-based design supports power densities in excess of 200 W/in³ and power outputs to 1.8 kW/cell. The design readily scales for larger systems of multiple cells

Power components exploiting ChiP technology can provide exceptional thermal performance in two-sided cooling applications [2] (Figure 6). The thermal-management cell, depicted schematically in the figure, targets an $R_{\theta J\text{-}A}$ (junction-to-ambient thermal resistance) less than 0.66 K/W, allowing for dissipation greater than 60 W at 70°C ambient. The thermal-management cell concept supports power densities in excess of 200 W/in³ and outputs to 1.8 kW/cell with 400 VDC inputs under the same ambient conditions. The cell uses a single 40- x 40-mm fan to cool both top and bottom heat sinks and is inherently scalable for larger outputs.

Literature

[1] Salato, Maurizio, The Sine Amplitude Converter™ Topology Provides Superior Efficiency and Power Density in Intermediate Bus Architecture Applications, Vicor Corporation, June 2011. http://cdn.vicorpower.com/documents/whitepapers/wp_sac.pdf.

[2] Oliver, Stephen, 3D Cooling of New High Density DC-DC Converters, APEC 2013 Conference, Long Beach CA, March 2013.

New ChiP packaging platform

The initial lineup of Vicor components based on the ChiP packaging platform includes five different package sizes, with more on the way. This is enabled by the underlying scalability of the ChiP manufacturing process.

Analogous to semiconductor wafer fabrication, individual ChiP-based components are arrayed to utilize 100 % of the PCB material, with no area lost to lead/pin attach. The array is then sawn into individual 'chip-scale' components with no superfluous, non-value-added packaging, thus minimizing space used in customer designs. The sawing process exposes "bar codes" from which interconnect terminals are formed. X- and y-dimensions are flexible, allowing low- or high-power converters, with additional flexibility in the z-axis to allow optimized magnetic transformer or inductor designs. The first entry in ChiP-based power component portfolio will arrive to market later this year, and will be targeted at datacenter, telecom and industrial applications.