Practical Use of SiC Power Semiconductors

Silicon Carbide (SiC) power devices are enabling components mainly in the context of higher switching frequencies and/or small footprints in power electronics. However, this trend imposes new challenges on the packaging of the chips. Typical stray elements like inductances become crucial elements in the circuit. In addition, different considerations regarding the thermal design in power modules arise when SiC chips are taken into consideration. Furthermore, the aspects of power density as well as the general utilization of SiC's high temperature capability are important factors in reliable implementation of SiC-based power semiconductors in modern systems. The article will give an insight into how these boundary conditions can be implemented in innovative solutions using SiC chips. **Peter Friedrichs, Senior Director SiC, Infineon AG, Erlangen, Germany**

SiC power technology, predominantly in form of Schottky diodes, is meanwhile established in the market. High-power solutions using power-module technologies have recently become available. Usually, the aim of such components is to enable system benefits, for example by increasing the switching frequency or reducing losses. If this is successful, the high cost of SiC-based components can be compensated by reduced efforts for passive elements and/or cooling.

While the discrete, unipolar SiC devices as single chips are more or less ready to achieve higher frequencies (>100 kHz in PFC units), this is still a challenge for power modules. Solutions in a power range with traditional modules have high stray inductances and thus the di/dt is increased if combined with an increase in the frequency. A plug and play between SiC and Silicon at chip level in existing modules could devaluate the theoretical SiC performance. It is necessary to improve high-current modules in order to get the full benefit of SiC in the frequency range above 20 kHz.

Current and power density considerations for state-of-the-art SiC devices

Whilst the reduction of parasitic elements in power modules using SiC chips is in line with the approach also used for future Silicon solutions, it might happen that different optimization criteria will apply for the thermal design. The reason for this is that the cost contribution of chips in a power module with SiC is different from one with Silicon. Thus, the best solution for a given frame size with respect to semiconductor area placed in the module could be different. Furthermore, it is expected that the die size of a SiC transistor at 1200 V, for example, comes down to one tenth or less of the area needed in the current Silicon-based IGBT technology, assuming the same total losses for both options. This will result in a huge increase in power and current density, and will require more efforts with respect to an effective heat removal and the connection of chips to terminals.

SiC diodes

Several new generations of SiC Schottky diodes have been introduced since the first launch in 2001, each leading to a further increase in power density. Since 2006, Infineon has been using a Merged-Pin-Schottky (MPS) structure [1] for 600/650 V diodes, mainly in order to offer a sufficient surge-current capability. Other devices on the market are designed as JBS (Junction Barrier Schottky) diodes; from a design point of view, the layout is similar, the difference being that the main purpose of a JBS is to shield the electric field in reverse mode from the Schottky interface in order to keep the leakage current low, while in an MPS the main purpose is to offer surge current. In these diodes, only a part of the active area is used for the current flow; the rest is passive, being in operation in the MPS for only a short period of time (pulse mode). This again represents a further local increase in the current density, as shown in Figure 1 using the basic principle of the MPS diode as an example.

The shown values today are close to the highest current densities for silicon power parts, which are known from low voltage transistors (e.g. 25 V at around 1300 A/cm²).Taking into account the voltage drop at operating temperature (which can

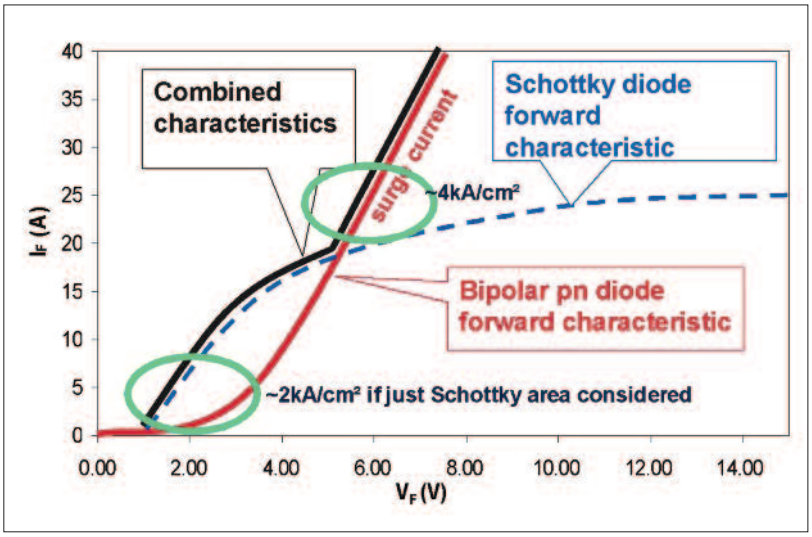


Figure 1: Current densities in recent generations of Infineon's 650 V MPS diodes (3G and 5G devices)

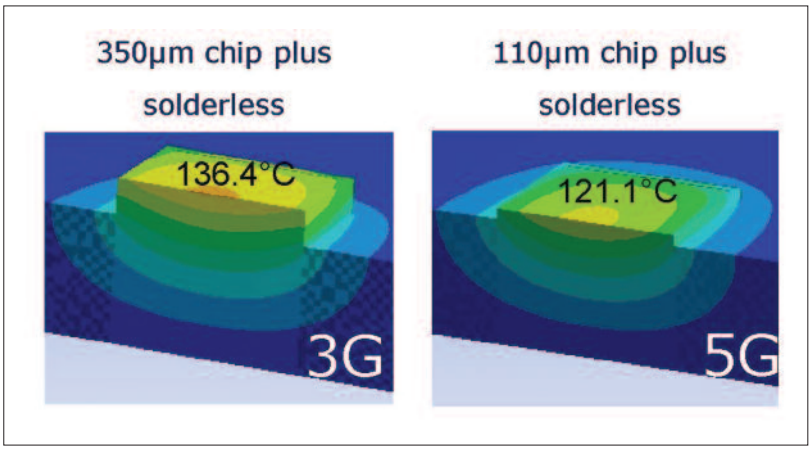


Figure 2: Chip thickness shrink effect on the maximum temperature of an SiC diode with 5.1mm² area on a copper lead frame and a power stress of 170 W; due to the smaller die thickness, the effective R_{th} is reduced

be > 2V), it becomes obvious that heat generated by the power density at the chip with >2kW/cm² can be effectively removed only if effective heat spreading is implemented between junction and case.

Another aspect of modern device design is the reduction of the die thickness. In the special case of vertical SiC devices, the active layer is just a few µm thick, and thus any additional material below it is merely an increase in the (differential) on-resistance and the thermal resistance of the chip [2]. It is thus reasonable to thin the wafers down to the smallest possible value, often defined by the handling capability in manufacturing. Infineon introduced thin (110 µm) wafer devices with its 5th diode generation (5G), offering a further step in power density, as shown in Figure 2.

But this benefit has a drawback – the thermal capacitance, which is important under pulse current stress, is also reduced due to the shrunken volume of the semiconductor. Technologies must therefore be developed to compensate for this, otherwise only reduced pulse ratings are possible. One approach is a good thermal connection of the chip to the lead frame, e.g. by solderless assembly technique, enabling the utilization of the underlying copper as a support for pulsed operation [3].

SiC transistors

The focus today is on the implementation of unipolar high-voltage (600 V … 1700 V) transistors, offering threshold-free linear I-V characteristics, integrated body diodes, and negligible dynamic losses compared to the competing Si-IGBT technology. The Ron x A values expected for 600 V components that seem to be achievable long term are around 1mΩcm² [4]. The benchmark with the above-mentioned low-voltage Silicon technology shows that such values are still a factor of 20 higher than the best-in in-class devices for 25 V today. So it seems that experience with Silicon is sufficient to handle high current densities for SiC transistors.

Nevertheless, one mode of operation will need closer attention. It seems to be mandatory for the success of SiC transistors in industrial applications to operate the internal body diode as a freewheeling diode. There might be some concerns regarding efficiency in this operation mode, because the forward voltage drop is too high; however, one can turn on the channel after a short dead time and then the I-V characteristic in reverse mode is identical to or even slightly better than in forward mode (see Figure 3).

Anyway, there might be a critical situation should the driver circuit fail when diode mode is required by the system. To cope with this mode, one may be forced to define the actual current rating, not from the attractive threshold-less forward I-V, but out of the power handling capability in reverse mode. Thus, lowest VF is required, or alternative solutions for designing the diode function in the 3rd quadrant mode must be developed.

High-frequency optimization

Real power circuits with SiC chips inside contain inductance and capacitance as major parasitic elements, and these cause serious deviations from perfect switching. Basic effects of parasitic inductance are:

- a voltage dip during turn-on of a transistor, caused by rise of current
- a voltage spike during turn-off of a transistor, caused by current fall
- the parasitic capacitance together with the inductance form resonant circuits, which show damped oscillations after each switching transition

The effect of parasitics is already more pronounced when a combination of an IGBT with an SiC freewheeling diode is considered, since the diode performance also speeds up the transistor and thus, under improper conditions, oscillations could be observed as seen in Figure 4 (left side) when no special precautions are taken. Therefore, an optimum circuit design with minimum parasitic inductance is a prerequisite for the optimization of power semiconductors towards lowest losses [5].

To meet these demands, rules were

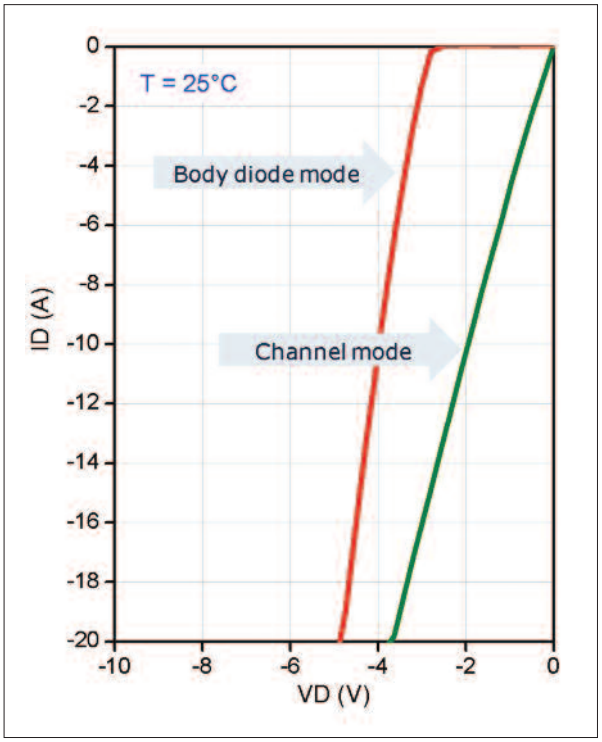


Figure 3: SiC transistors (example SiC JFET from Infineon) in 3rd quadrant – channel mode possible to reduce losses by turning on the channel in freewheeling operation; however, in critical modes the I-V in diode mode might define the current handling capability

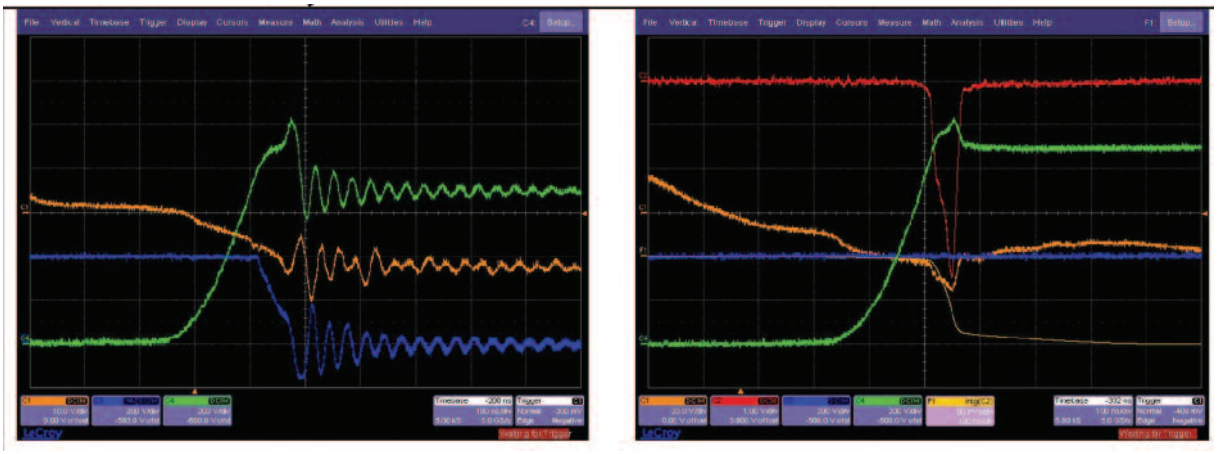


Figure 4: **Left - standard module switched with 400 A (turn-off) and a DC link bias of 700 V; the green trace shows the voltage; blue (left) or yellow (right) the current; and orange the gate signal. Right - new module approach, DC link bias now 900 V**

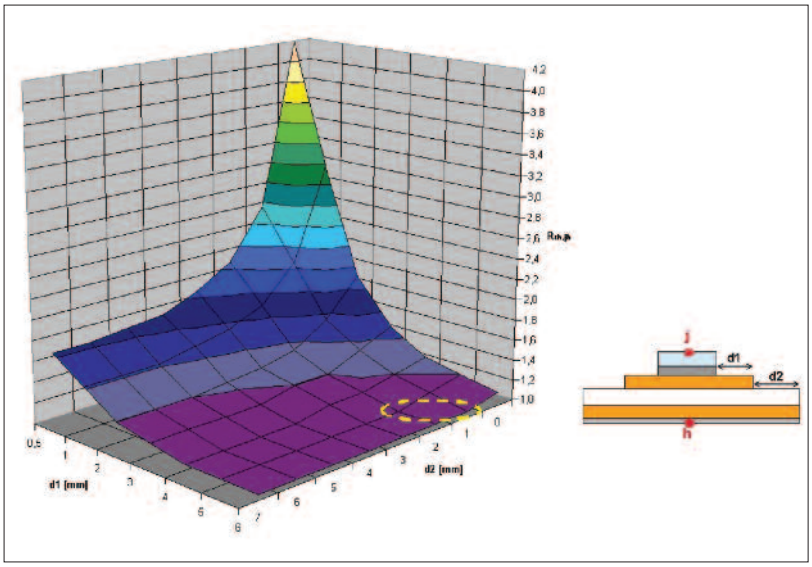
developed at Infineon [6] for the design of power modules. It is well known that a strip-line type of circuit design brings parasitic inductance to a low value, depending on width and distance of the strip line [7]. The graph on the right in Figure 4 shows the effect on the switching performance of power semiconductors of an improved module layout, taking these considerations into account. Whereas, in the standard module, a severe over-voltage peak plus oscillations are observed, the new solution can eliminate these effects almost completely. It has to be noted that the improvement was achieved without changing the chip technology, but simply by a more careful design of the package. These considerations will also take into account the fact that, on the midterm scale, paralleling of a high number of dies will be the preferred method of achieving higher power levels in SiC.

In order to avoid a degradation of the high performing SiC chips by an unsuitable environment, Infineon will drive the implementation of SiC semiconductors only in module platforms that enable this approach.

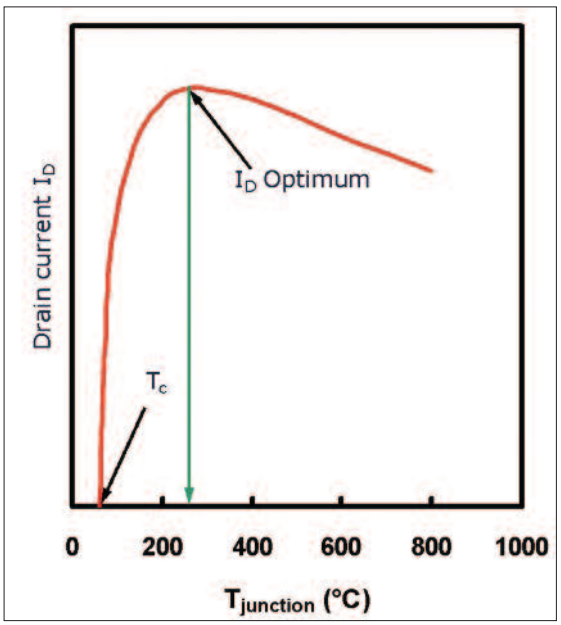
Thermal considerations

The final power-handling capability of a semiconductor module is defined by the chip area inside the module combined with the thermal performance expressed by the R_{th}. For Silicon chips, as much as possible chip area is usually placed on a given footprint in a power module, because normally the area cost per chip is not so much different from the cost per module area, mainly for larger power ratings.

In the case of SiC, different considerations apply. The chips are much more expensive than Silicon ones, so it is beneficial to choose a different ratio of chip area to module area to get the optimum solution with respect to the price/power ratio for a given footprint. The reason for this is that, by proper design, the effective R_{th} per chip can be reduced by a factor of up to 4 due to heat spreading effects, as shown in Figure 5 (base-plate-free module).



ABOVE Figure 5: **Effective thermal resistance for a configuration in a base-plate-free module. Setup shown on the right side. A 0.32 mm thick ceramic with 0.6 mm Cu on both sides is assumed**



LEFT Figure 6: **Extractable current from a system with a given R_{th} and T_c, the component having a dependence of its on-resistance on temperature with an $R \sim T^2$ law**

In addition, there is a trend towards higher maximum chip temperatures, in order to increase the removable heat for a given die area, and thus its current-handling capability. It must be mentioned that doing this will increase the absolute losses, so that efficiency targets could be violated, depending on the ratio of loss increase to increase in power-handling capability. In contrast to IGBTs, this loss increase might be huge for unipolar SiC devices, because now a resistive component with a heavy increase in the R_{on} with temperature is in place, mostly with a power law in the form of $R_{on} \sim T^X$, with x values between 2 and even 2.5, as recently presented for high voltage SiC MOSFETs.

Taking this into account, one can see that, for unipolar devices, a continuous increase of Tj can even lead to a reduction in current-handling capability, because more power is dissipated than can be removed by the increase of T_j. Figure 6 shows this result for a typical dataset, assuming x=2 as the exponent in the power law for the increase of the resistance with temperature.

In addition to these considerations, it is known that the reliability of power systems, mainly the power cycling capability, is degraded when the temperature swing between off state and maximum temperature is increased [8]. Thus, for the sake of both efficiency and reliability, it might be wiser to offer good cooling and keep the temperature differences in the thermal stack low.

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