Fine Tuning of Digital Control in POL Regulators Optimize Dynamic Response and Minimize Component Count

Power system design encompasses many requirements and criteria. This article is about perhaps the most basic of all requirements – a stable voltage supply of the operating circuitry. **Patrick Le Fèvre, Ericsson Power Modules, Sweden**

Each electronic circuit on the printed circuit board (PCB) is designed to operate over a limited range of DC voltage, outside of which circuit operation or performance is not guaranteed. A generalized view of the static voltage and associated tolerance is shown in Figure 1.

In order to achieve high speed and low power dissipation, recent microprocessor , DSP and FPGA chips require voltage levels of 1 to 3.3 VDC with a tolerance of as little as ±30 mV. These types of requirements place severe demands upon the power system.

Dynamic response

Most types of circuits demand dynamic input current for short periods of time. The power system is designed to handle fast dynamic current by means of decoupling capacitors located in proximity of the electronic circuits, while the power supply handles low frequency and longer duration dynamic demands (see Figure 2).

The power supply control loop, the distribution impedance and the decoupling capacitors decides how the dynamic current is shared between the decoupling capacitance and the power supply.

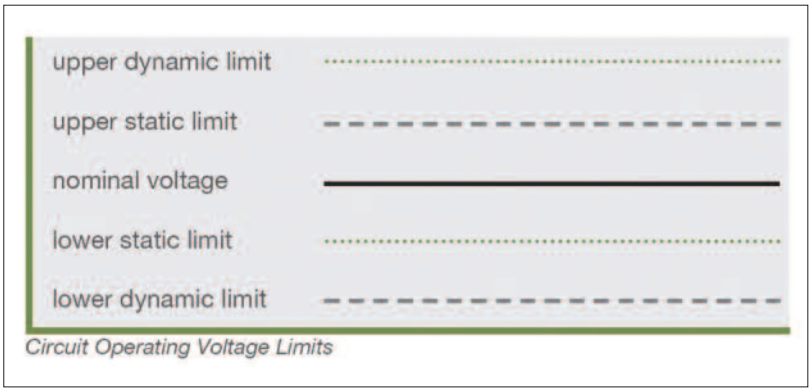


Figure 1: **Circuit operating voltage limits**

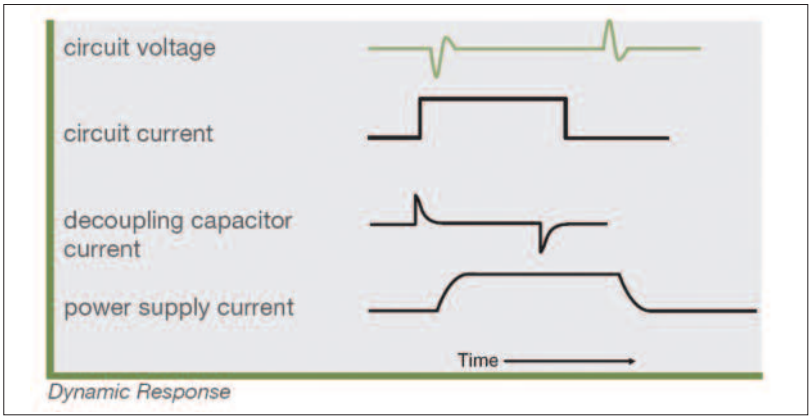


Figure 2: **Principals of dynamic response**

Digital control of POL regulators

Digital control is not a magic wand that can twist the physical laws, but it makes it possible to improve and optimize the dynamic response performance because the digital protocol does not have to take into account any tolerance problems which are the case for the capacitive and resistive networks used in analog control loops.

Ericsson now offers a useful software tool that designs, simulates, analyses and configures the POL regulator within minutes. It includes simple tools for robust design of control loops, together with more advanced design and analysis tools to optimize the dynamic response performance and minimize the number of decoupling capacitors needed for a certain load transient requirement. The tools are integrated in the DC/DC Power Designer software, enabling quick and efficient automated design and analysis.

Modelling of the POL regulator

The most common topology for POL

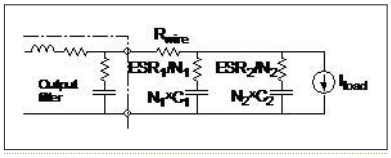


Figure 3: **Model of the power module with external decoupling capacitors**

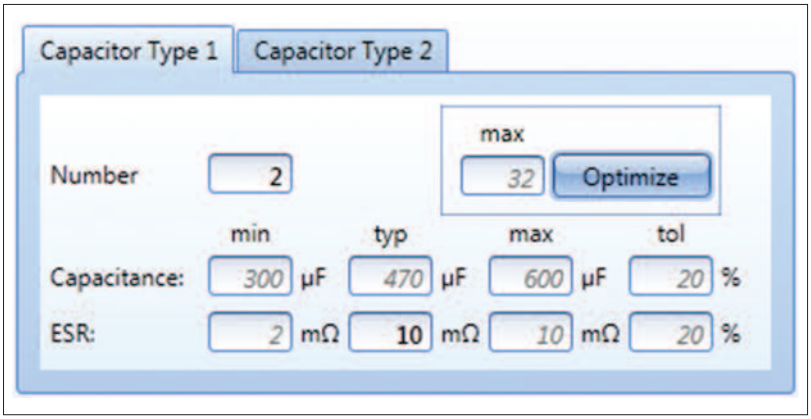


Figure 4: Capacitor description

regulators is the buck converter. The output filter of the POL regulator consists of an internal output capacitance and an additional mix of different types and sizes of decoupling capacitors on the PCB in proximity of the electronic circuits. Figure 3 shows the fundamental schematic. As the decoupling capacitors become a part of the system that should be controlled, they must be included in the model. The model also includes a resistance, R_{wire}, for modelling of the lead resistance on the PCB. Two different types of capacitors are included in the model.

System analyzes and component tolerances

The decoupling capacitors are entered into the tool with capacitance and ESR, including tolerances. Tolerances are important because they define the 'corners' of the system. This is handled by calculating all the corner cases for the power train filter. Figure 4 shows the enter field for capacitor data.

Using two different capacitors, each with tolerances for the capacitance and the ESR, yields a total of 16 corner systems and one typical system. All 17 systems (16 combinations of min/max values, plus one with typical values) are then simulated and evaluated. Each system's natural frequency and damping ratio are then calculated and the results are used as input to the control loop design.

Control loop design

The tool uses a linearized model of the power train and a system transfer function based on a sampled state-space model and the control loop design is fairly straight forward using standard control theory. In today's digital control circuits, the PID regulator is often implemented as second order digital filter, where the integrator part is fixed and in many cases impossible to remove. Hence, the software tool is designed to define the placement of two zeros and the total gain in the loop.

A common tool for open loop design is the Bode plot, shown in Figure 5, in which the compensation zeros are placed to obtaining the proper behavior and adjust the gain to meet the robustness requirements in terms of phase and gain margins. Common values for these requirements are 60°, and 6 dB, respectively.

The tool plots the typical system, analyses all 16 corners systems, and plots the systems with the minimum and maximum values for the phase and gain margin. If all design requirements are fulfilled, a green signal together with the word 'Stable' is shown in the upper left corner, which gives quick answer of the loop stability.

However, the phase and gain margins are not enough for a robust control loop. This cannot be observed in the open loop Bode plot only, but becomes obvious in the closed Bode plot, see Figure 6, and can be handled with additional design requirements.

If the gain becomes too high the system attenuation at higher frequencies stops to be monotonically increasing, and instead starts to increase towards the Nyquist frequency. The Nyquist frequency is $f_s/2$, where fs is the switching frequency. Another indication is that the gain around the system's resonance frequency forms a peak. This results in a sensitive system and output voltage oscillations during transients. This can be avoided if restrictions are put on the peak gain and the gain at the Nyquist frequency. The rules (peak gain < 1 dB; gain at Nyquist <

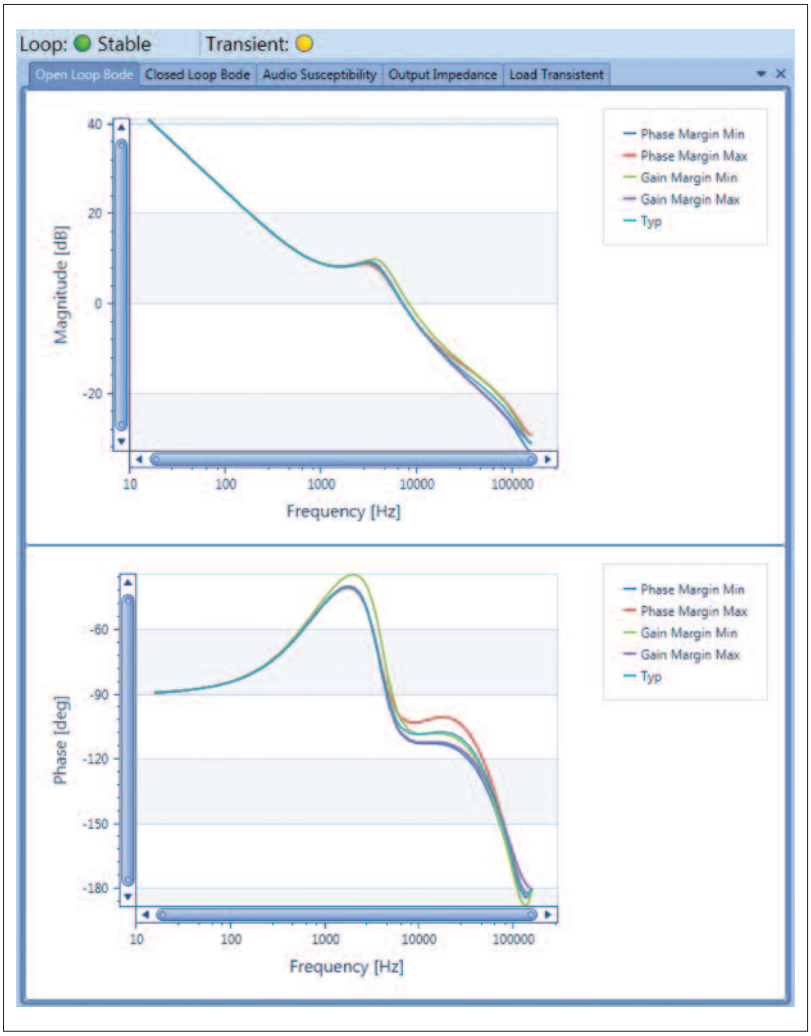


Figure 5: Open loop Bode plot

-6 dB) have been shown in practice to work well.

An additional key figure that is a little coinciding with these former key figures is the bandwidth, which in the past has earlier been used as a rule of thumb (bandwidth < f_s/10) for avoiding oscillations.

This rule of thumb describes the benefits of high switching frequency. Besides the advantage of smaller capacitive and inductive components, higher switching frequency will make it possible to increase the bandwidth of the control loop and thereby improve the dynamic response.

The tool plots the typical system, analyses all 16 corners systems, and plots the systems with the minimum and maximum values for Peak gain, Bandwidth, and Gain at Nyquist frequency.

A common 'rule of thumb' for placement of the control loop's zeros that is robust and gives good transient behavior is:

- Place first compensation real zero at the systems typical resonance frequency
- Place the second real zero one octave below the first zero

This is implemented in the tool for a simple and robust design, which will in many cases be good enough.

The tool also has an Auto gain function, which automatically maximize the loop gain for maximum performance with the design requirements fulfilled for the typical system. This makes the manual design of the zero's placement much easier and quicker.

Dynamic response optimization

In the case of a known system the load transient can be optimized by placing the compensation zeros differently compared with the rule of thumb described above.

A goal function is defined as the weighted sum, w_x, of the voltage deviation, dV, and recovery time, T_{rec}, during load transients and each normalized with the corresponding system requirements:

$$Goal = w_1\left|\frac{dV}{dV_{req}}\right| + w_2\left|\frac{T_{rec}}{T_{req}}\right|.$$

The tool picks zero pairs around the systems resonance frequency and uses an iterative method to find the zero pair which gives the smallest Goal value. First a coarse search is made and then a second fine tuning to find the optimum placement.

For each zero pair placement the control loop's gain is designed based on the closed loop Bode analyses described earlier. Then a load transient simulation is performed with the following user defined load transient key figures:

- Low current level [A]
- High current level [A]
- Slew rate [A/µs]
- Load transient period [ms]

The zeros placements with the smallest Goal value will result in a design with optimized dynamic response.

Minimizing the decoupling capacitance

The tool can also be used in the design of the decoupling capacitance network by determining the type and number of capacitors and capacitance that is needed in order to meet the load transient requirements. Decoupling capacitors occupy expensive area on the PCB and is also adding to the system cost. Therefore it is important to optimize the system design for minimum decoupling capacitance and number of capacitors.

Design examples

The first example shows the difference between dynamic response at load transients with standard PID settings and optimized settings. The conditions are:

- 2 pieces of 470 µF, 10mΩ
- 8 pieces of 100 µF, 5mΩ
- Input voltage is 12V, output voltage 1.0 V.

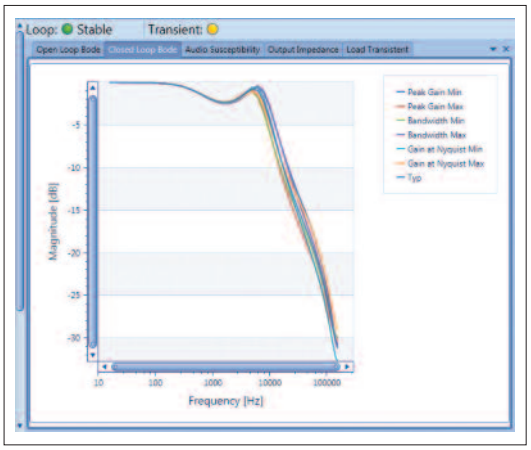


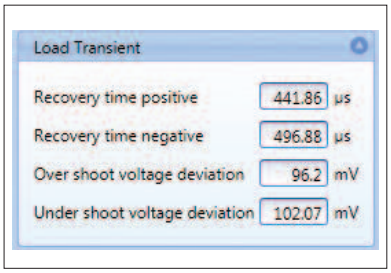
Figure 6: **Closed loop Bode plot**

With the default PID settings and a 5-15 A load step, with a slew rate of 10 A/µs, gives the voltage deviations and recovery time shown to the left in Figure 7. Using the tool's rule of thumb for placement of the controller's zeros gives the result shown to the right. This shows the potential of optimizing PID for a known load, where in this case, the voltage deviations are halved and the recovery times are reduced with a factor of three.

Using the load transient optimization with equal weights for voltage deviations and recovery time yields the following results shown in Figure 8, which shows that the recovery time can be improved further without significantly increasing the voltage deviations.

The second design example shows how it is possible to reduce the decoupling capacitance and number of capacitors and still improve the dynamic response performance.

Using the tool's 'rule of thumb' PID



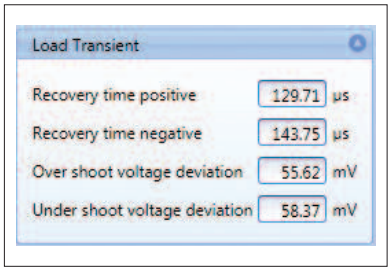


Figure 7: **Default PID setting (left) vs. "rule of thumb" PID setting**

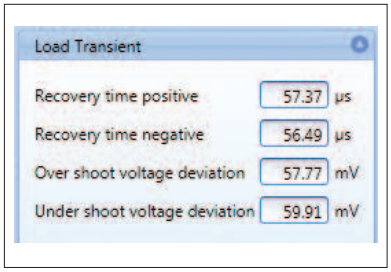


Figure 8: **PID settings optimized for best dynamic response**

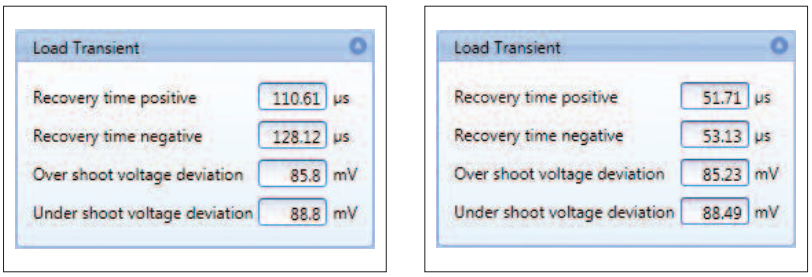


Figure 9: Optimized PID for minimum decoupling capacitance (left), further improvements could be done with the optimized PID settings as shown to the right

settings the number of capacitors can be reduced to one 470 µF and six 100 µF. As the tool runs the optimization for the worst case system, the load transient on the typical system has a margin compared with the load requirements, shown to the left in Figure 9. Further improvements could be done with the optimized PID settings as shown to the right in Figure 9. The result shows that the recovery times are halved and still with maintained voltage deviations.

Figure 10: V_{out} deviation with default PID settings and 5,000 µF

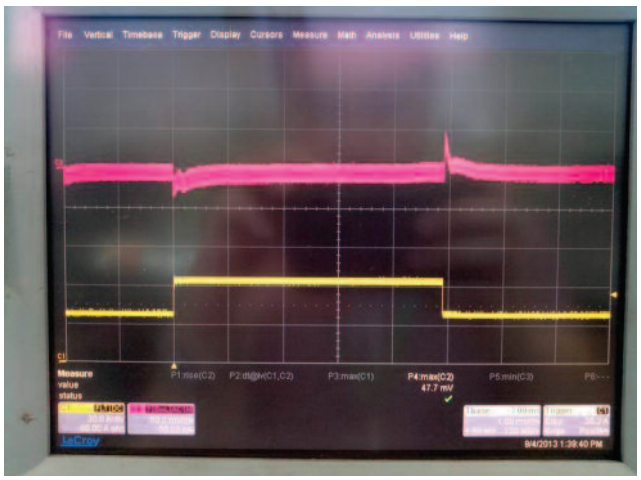
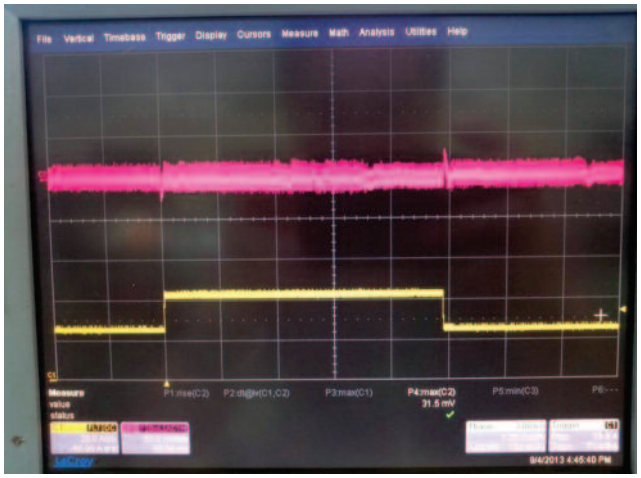


Figure 11: Dynamic response with optimized PID settings and reduced decoupling capacitance



Customer application example

The tool has been used in actual customer applications with very good results. This example shows the improvements achieved using two paralleled Ericsson BMR464 POL regulators with optimized PID settings compared with the default settings.

System requirements:

- V_{in} = 12 V
- V_{out} = 1.0 V
- Current transient 26 to 44 A with 1.8 A/µs slew rate
- V_{out} tolerance = ±3 % (±30 mVp-p)

With the default PID settings and 5,000 µF electrolytic capacitors the measured Vout deviation was 48 mV (see Figure 10).

With optimized PID settings and reduced decoupling capacitance with 1,000 µF ceramic capacitors and two electrolytic capacitors with 1,000 µF respective 470 µF capacitance the V_{out} deviation is improved to 32 mVp-p (see Figure 11).

Conclusions

The default wide range PID that Ericsson POL regulators are delivered with is designed for robust and stable operation. With the described tool integrated in the Ericsson DC/DC Power Designer software it is possible for the power system designer to fine tune the POL regulator's control loop in the particular application and significantly improve and optimize the dynamic response performance and/or reduce the required decoupling capacitance.

Fewer output decoupling capacitors can be used to insure a given voltage tolerance which means lower component cost and most importantly it will also have a huge impact and pay-off in terms of reduced time-to-market and increased system packaging density.