How 600 V GaN Transistors Improve Power Supply Efficiency and Density

High performance power supplies today are already very efficient. For at least two years, "Titanium" efficiency server power supplies have been announced with greater than 96 percent overall energy efficiency at half load (per 80 PLUS®* standards). These power supplies achieve this high efficiency level using today's available technology including high performance Si FETs and SiC Schottky diodes. So what comes next? With several companies announcing the availability of GaN on Si 600-650 V transistors, how will these new devices take power supplies to even higher levels of efficiency, and density?

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To begin, consider the limitations of existing Silicon FET technology, and what power supply designers would want in a more ideal switching device. Controlling conduction loss is straightforward: a larger area FET or several FETs in parallel will reduce effective $R_{DS(on)}$ to negligible levels. But there is of course a tradeoff here. More FETs also means more capacitance (and, therefore, charge), thus increasing frequency-dependent switching losses. So for a given frequency range, power supply designers must balance conduction and switching losses to achieve the overall lowest total loss. Moreover, the dynamic characteristics of a FET body diode have a significant impact on frequency-dependent losses in certain topologies. This is where new technologies like GaN can add value. For a given $R_{DS(on)}$, GaN switches have lower output charge Q_{oss}, lower gate charge Q_g, and vastly lower reverse-recovery charge

Q_{rr}, than the best available Silicon FETs. Moreover, GaN devices have a much more linear charge versus voltage characteristic than superjunction FETs (superjunction is the dominant high-voltage FET technology used in power supplies today). The linearity of Q_{oss} plays a key role in reducing deadtime and, therefore, enabling high efficiency at high frequencies.

New solutions ahead

The new breed of GaN devices are High Electron Mobility Transistors (HEMTs), which have been described in numerous publications recently. To be cost-effective, HEMTs are manufactured on Silicon substrates, rather than Silicon Carbide or pure GaN which are both easier, but considerably more expensive.

HEMTs are lateral devices that can be manufactured as either enhancement or depletion-mode transistors [1]. For power

electronic designers, a normally-off power switch (meaning the FET is off when the gate voltage is zero) is much preferred over a normally-on device, even if the normally-on device could provide some additional performance. This is because normally-on devices make it challenging to control current during power-up and power-down for example, requiring a master enable switch or a pre-bias arrangement to make sure the normally-on devices don't turn-on randomly when the control circuit is booting-up or powering-down. Early 600 V GaN HEMTs developed for power electronics were depletion-mode devices. To solve the normally-on issue, the depletion-mode HEMT was combined with a low-voltage Silicon MOSFET to form a normally-off hybrid device known as a GaN cascode [2,3] (see Fig. 1). Enhancement-mode GaN HEMTs at 600 V (which are intrinsically normally-off) were perhaps
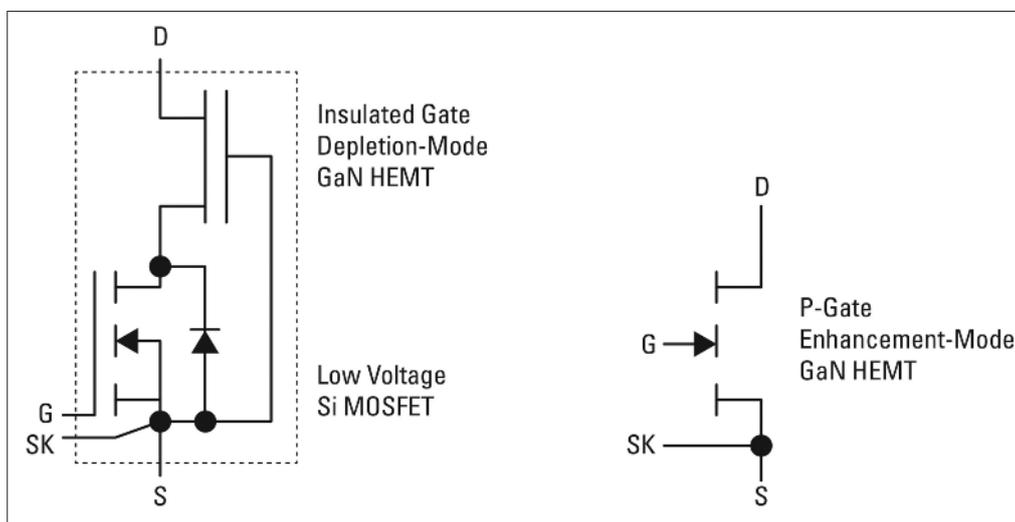
Figure 1: Normally-off 600 V GaN transistors: Cascode and enhancement-mode HEMT

Parameter 600 – 650 V, 100 mΩ	Best Si Superjunction	GaN Transistor range
Typical Q_g	40 nC	3 – 12 nC
Typical Q_{oss} @400V	260 nC	24 – 60 nC
Typical E_{oss} @400V	4.5 µJ	3.7 – 7.5 µJ
Typical Q_{rr}	7 µC	0.0 – 0.06 µC

Table 1: Comparison of Si Superjunction versus GaN transistor key attributes (normalized to 100 mΩ)

more challenging to develop, but are also now just becoming available on the market.

Enhancement-mode and cascode are two different approaches to providing a high performance 600 V normally-off GaN-based switch. While there are differences between the two devices (mainly in the gate drive circuit and the reverse conduction characteristic), both devices provide vastly improved "body diode" performance Qrr, and significantly lower Q_{oss} and Q_g compared to the best available Silicon FETs with similar voltage and $R_{DS(on)}$ ratings. The key attributes of these devices are outlined in the comparison chart above. The data is gathered from recently published articles, papers and datasheets, and normalized to 100 mΩ typical $R_{DS(on)}$ assuming R x Q product is constant. It is not necessarily representative of a particular device, but shows the performance trends between these technology platforms from multiple vendors (see Table 1).

In search of higher efficiency
How do these attributes translate into a benefit for power supplies? The answer is that it depends strongly on the topology. For example, consider traditional boost PFC, which is the most common PFC circuit used today for server power supplies (Figure 2):

this is a unipolar topology, so the FET only conducts current in the forward direction – the body-diode is never used. Since this topology is mostly operated below 100 kHz, the gate charge losses are relatively low, so any benefit in Qg is minimal. The two dominant parameters that most affect efficiency are $R_{DS(on)}$ for conduction losses, and the energy dissipated each switching cycle due to the discharge of Q_{oss} when the FET turns on (E_{oss}).

This is where things get confusing: even though the Q_{oss} of the GaN HEMT is significantly lower that the best superjunction, the E_{oss} (the energy stored in C_{oss}) difference between superjunction and GaN is much smaller. The lowest E_{oss} superjunction can be better than cascode GaN, but not as good as enhancement-mode GaN. This paradox occurs because the bulk of the charge stored in superjunction is injected at low voltage (<50 V). Above this, from 50 V to 400 V, the effective charge is lower, but the energy is much higher since

$$dE = \frac{C(V)}{2} dV^2 \qquad (1)$$

(note the V^2 term and the value of C is a function of V). As a result, even though the

charge Q_{oss} at 400 V is 5 to 10x lower for GaN than SJ, the *energy* difference is much smaller: the best superjunction is better than cascode GaN and within 15 % of enhancement-mode GaN (see Table 1). The net result is this: if you simply drop-in the same $R_{DS(on)}$ GaN switch into a high-performance superjunction socket like this PFC example, the overall efficiency change is barely measurable.

To get to higher levels of efficiency, one must look more closely at how power loss is distributed in each topology: The main source of loss in traditional boost circuit is not typically from the switch – loss is dominated by the input bridge rectifier which always contributes two (2) diode drops over the entire line cycle.

To utilize the full benefit that GaN transistors offer, consider instead the totem-pole bridgeless boost circuit shown in Figure 3. In this topology, there is no input bridge rectifier, and, therefore, no diode drops (except 1 briefly during deadtime). The low-frequency half-bridge on the right flips the polarity of the line every half-cycle, so switching loss is negligible, only conduction loss matters (this can, therefore, be low cost superjunction). The half-bridge on the left operates at high frequency (typically Continuous Conduction Mode CCM in the 50 – 100 kHz range), with one transistor serving as the boost switch, and the other as the synchronous rectifier – and they swap roles each half-cycle. Besides eliminating all diode voltage drops, this topology has the additional advantage that it can be operated in CCM, CrCM, DCM and even ZVS mode, which enables much higher operating frequency while maintaining outstanding efficiency.

The totem-pole bridgeless boost is not a new topology; it has been around for many years. But until now, the high

Figure 2: Traditional boost PFC circuit (typically Q1 is superjunction and D5 is SiC Schottky)
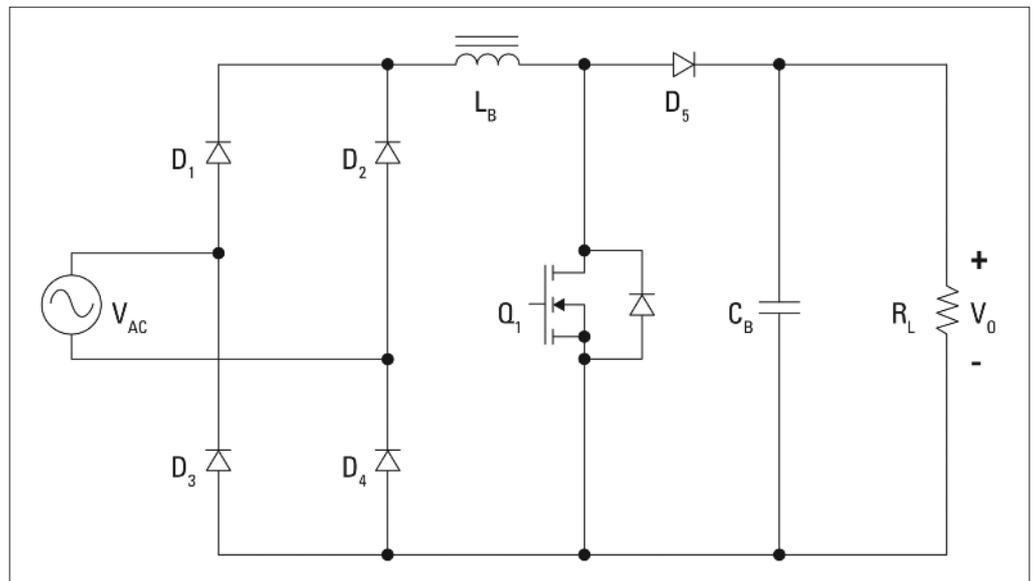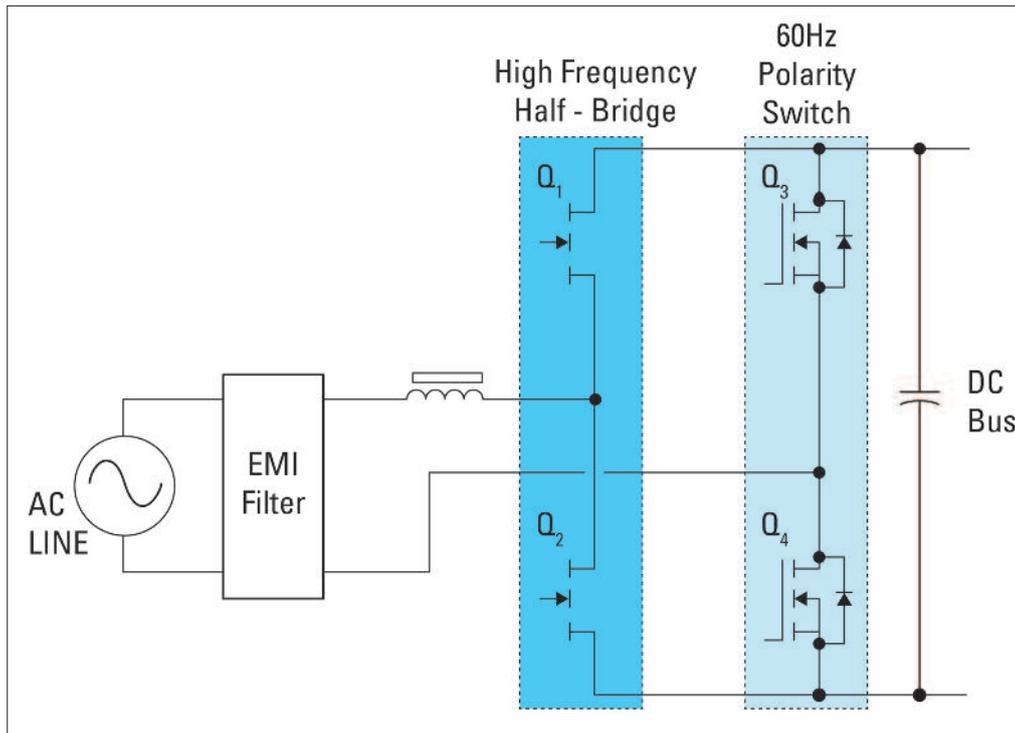
Figure 3: Totem-pole bridgeless boost topology (full-bridge, no diodes)

performance FETs (with low or zero Q_{rr}) have not been available to enable practical implementation. Now with GaN transistors in this topology, several papers have recently reported energy efficiency of the PFC stage exceeding 99 % at standard operating frequencies in CCM. Moreover, a recent CPES presentation from Virginia Tech demonstrated this topology operating in ZVS mode into the MHz range, also exceeding 99 % peak efficiency [4]. This level of performance is quite compelling, and will clearly drive development in the next generation of high performance, high density power supplies using GaN transistors.

The isolated DC/DC stage in power supplies can similarly benefit from GaN transistors. But just like the PFC example above, the benefit is not fully realized by simply dropping a GaN transistor into a FET socket in an existing power supply design, especially in hard-switching unipolar topologies where superjunction already does very well (Flyback, two-transistor forward). The topology, control strategy, magnetics, and operating

frequency all need to be considered in the overall design when optimizing for GaN devices. GaN is particularly well-suited for soft-switching and resonant topologies like LLC half and full-bridge, and ZVS phase-shifted full-bridge. The low charge of GaN devices reduces the circulating currents necessary to achieve soft switching, reduces deadtime and therefore rms currents, and reduces gate drive power, while still enabling efficient operation at higher frequencies with smaller passive components [5].

Conclusion

Power supply designs can benefit from GaN transistors now using existing controllers and drivers for LLC and ZVS Phase-Shifted Full-Bridge topologies, operating efficiently at frequencies extending beyond the reach of superjunction. Look for advanced controllers for totem-pole bridgeless PFC and even higher frequency resonant and soft-switching topologies to compliment a broadening portfolio of GaN transistors in the future. By combining these topologies

with state-of-the-art drivers and GaN transistors, tomorrow's power supplies will be able to take full advantage of the efficiency and density gains made possible by high voltage GaN transistors.

Literature

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