GaN FET Module Performance Advantage over Silicon

Gallium Nitride (GaN) FETs are increasingly finding use as next-generation, high-power devices for power electronics systems. GaN FETs can realize ultra-high power-density operation with low power loss due to high carrier mobility in the two-dimensional electron gas (2DEG) channel, and high breakdown voltage due to large critical electric field. GaN FETs are a majority carrier device, therefore, the absence of reverse recovery charge creates a value proposition for high-voltage operation. **Narendra Mehta, Senior Systems Engineer GaN products, Texas Instruments, Dallas, USA**

With GaN devices now being grown on affordable Silicon substrates, compared to GaN on Sapphire or bulk GaN, power GaN FETs will find an increasing rate of adoption for highly efficient and form factor constrained applications in the 30 V and higher DC/DC voltage conversion space. In this article the loss mechanisms in a hard-switched DC/DC converter and how a GaN FET power stage can outperform Si MOSFETs will be investigated and a 80V GaN FET power stage to 80V Si devices compared.

80-V GaN halfbridge

A GaN FET power stage device such as the LMG5200 is an 80 V GaN half-bridge power module. This device integrates the driver and two 80V GaN FETs in a 6 mm x 8 mm QFN package, optimized for extremely low-gate loop and power loop impedance. The inputs are 3 V CMOS and 5V TTL logic compatible. Due to GaN's intolerance for excessive gate voltage, a proprietary clamping technique ensures that the gate voltage of the GaN FETs is always below the allowed limit. This device extends the advantage of discrete GaN FETs by offering a user-friendly package, which is easy to layout and assemble into the final product.

The LMG5200 meets the IPC-2221B and the IEC 60950 pollution degree 1 clearance and creepage requirements without any need for underfill. This is because the minimum spacing between high-and low-voltage pins is greater than 0.5 mm. This eliminates the need for boards to be manufactured with underfill and simplifies board design. The pin-out also eliminates the need for a via-in-pad design as there is adequate spacing between the power pins for via placement. Additionally, this helps in to reduce board complexity and cost (Figure 1).

DC/DC converter losses

In this section mechanisms that cause losses in hard switched converters will be briefly discussed.

A synchronous buck converter (Figure 2) is used as a DC/DC converter to compare the losses in a hard-switched converter. The approach for comparing the loss mechanism can be applied to other hard-switched converters as well. Losses in a switched-mode converter can be broadly divided into conduction losses and switching losses. The high-side MOSFET dissipates most of the switching losses. Conduction losses are

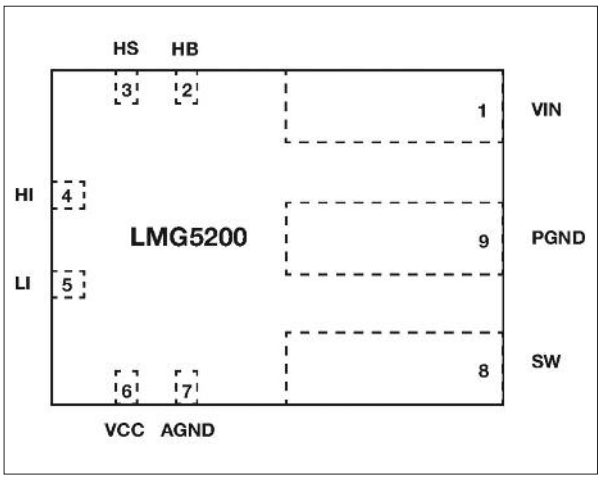


Figure 1: Top-down view of a GaN FET power stage device, showing pin-out

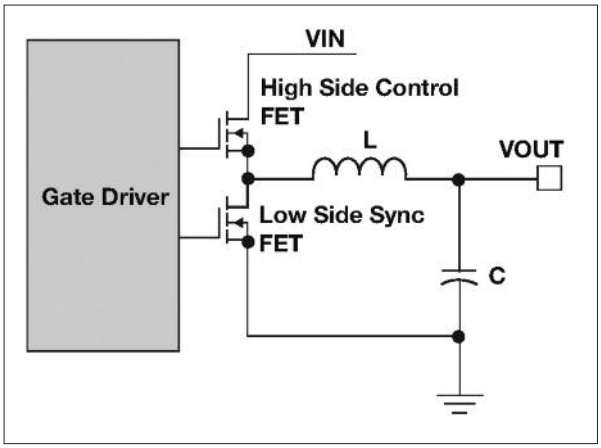


Figure 2: Simplified view of the buck power stage

a function of the duty cycle and are shared between the high- and low-side devices.

For low-duty cycle DC/DC converters, the low-side FET has a higher amount of conduction loss, which can be calculated as:

$$P_{COND(HS)} = R_{DS(ONHS)} \times I^2_{RMS(HS)} \quad (1)$$

$$P_{COND(LS)} = R_{DS(ONLS)} \times I^2_{RMS(LS)} \quad (2)$$

where $R_{DS(ONLS)}$, $R_{DS(ONHS)}$ is the low-side and high-side FET resistance, and $I_{RMS(LS)}$, $I_{RMS(HS)}$ are the low- and high-side RMS currents, respectively.

The switching loss (Figure 3) due to the

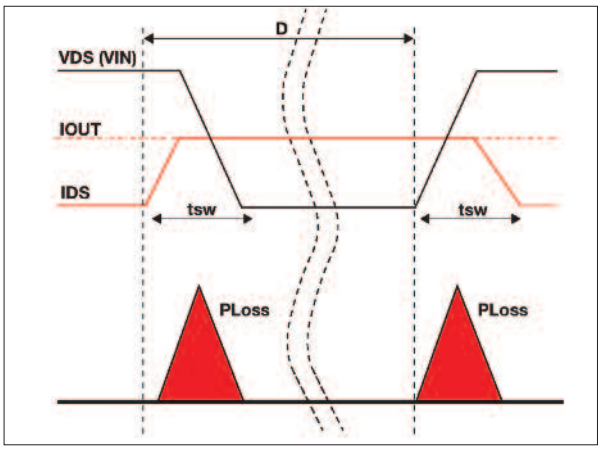


Figure 3: Turn-on and turn-off losses during inductive switching

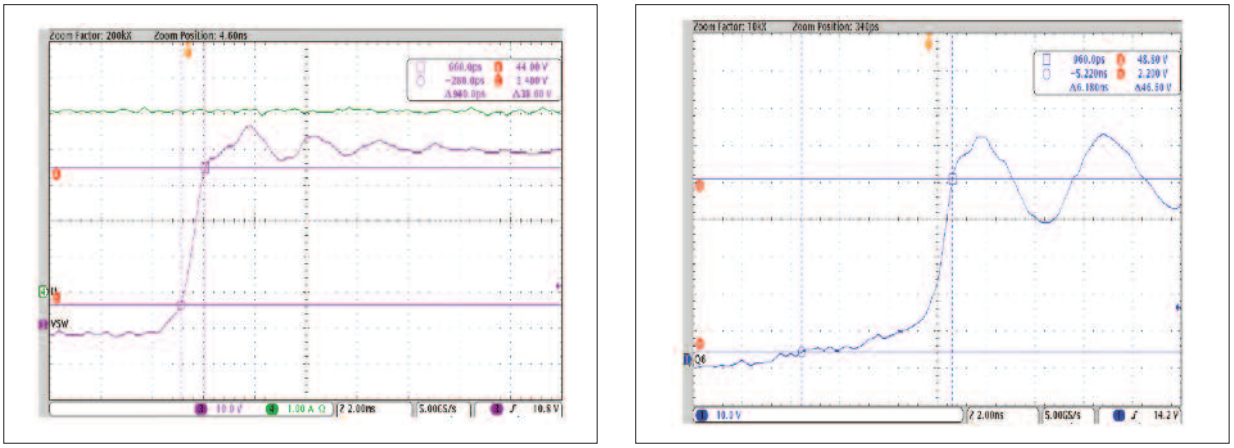


Figure 4: Comparison of a GaN FET power stage (LMG5200) switch-node (left) to Silicon (Si7852DP) switch-node voltage waveform

I_{DS} current and V_{DS} overlap is in the high-side of a buck converter and can be estimated as:

$$P_{SWHS} = V_{IN} \times I_{OUT} \times f_{SW} \times t_{SW} \quad (3)$$

where t_{SW} is the switching time. This includes the current commutation time through the FET and the time for the FETs drain-to-source voltage to rise / fall by V_{IN} during turn-off and turn-on, respectively.

The low-side FET does not have any switching loss due to zero voltage switching (ZVS) turn-on and turn-off. The actual waveforms for inductive switching are more complicated than those shown in Figure 3, however, the error in the calculated loss is acceptable as long as the correct switching time is used for the turn-on and turn-off.

The device construction of GaN allows very short switching times due to small gate and output capacitance for the same RDSON. As noted in Figure 4, switching time for the GaN FET power stage is less than 1 ns compared to 6 ns for a Si FET with a comparable breakdown voltage (Si7852DP).

Faster switching edges means the switching losses are significantly lowered in the GaN module compared to the Si MOSFET-based buck converter. Also there is minimal overshoot in the GaN FET power stage switch-node waveforms due to an extremely small (<300 pH) power loop inductance. The gate loop and common source inductance are also minimized in the GaN FET power stage package to be below 200 pH. High parasitic inductance in these loops can cause a significant power loss.

Besides the high-side turn-on and turn-off losses, forced commutation of the low-side MOSFETs body diode is a significant source of switching loss in high-voltage DC/DC converters. This loss is primarily due to the reverse recovery charge (Q_{RR}) in the freewheeling low-side FET. The power loss due to reverse recovery is given by:

$$P_{RR} = f_{SW} \times Q_{RR} \times V_{RR} \quad (4)$$

Because GaN is a majority carrier device, it does not have reverse recovery-based losses. The body diode of the low-side MOSFET conducts during dead time. This causes a power loss in the diode associated with the forward voltage of the diode. GaN has a higher third quadrant conduction voltage (V_{SD} of 2 V at 10 A for LMG5200) compared to ~1 V for Si FETs. Hence, the GaN device exhibits a higher power loss during dead time. It is critical to ensure that the dead time is small in order to minimize this loss. The power loss associated with the body diode can be calculated as:

$$P_{BD} = f_{SW} \times V_{SD} \times I_{OUT} \times (T_{DEADON} + T_{DEADOFF}) \quad (5)$$

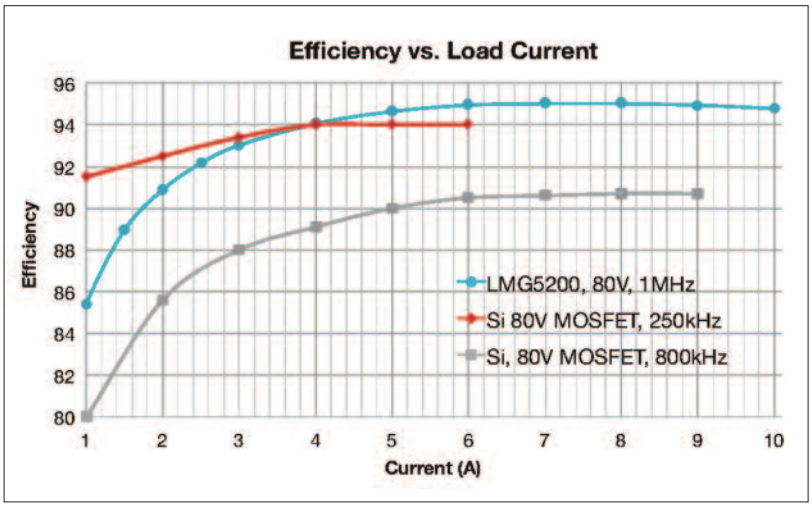
The energy stored in the output capacitance of the MOSFETs is dissipated during turn-on. Since the output capacitance is a strong function of the drain-to-source voltage, the proper way to calculate this power loss PC_{AP} is:

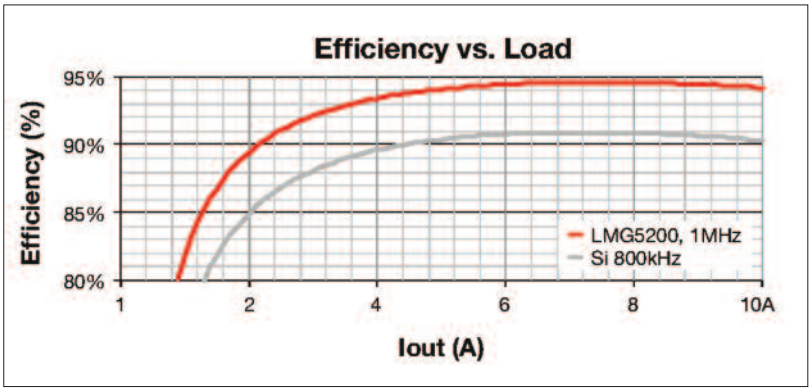
$$P_{CAP} = f_{SW} \times Q_{OSS(VIN)} \times V_{IN} \quad (6)$$

where $Q_{OSS(VIN)}$ is the output charge of the MOSFET, evaluated at the input voltage. GaN devices, due to their small output capacitance for the same R_{DSON} compared to Si, exhibit a much smaller P_{CAP} loss as well. Gate driver losses are another contributor to switching loss.

Besides the active device-related losses in a hard-switched buck converter discussed, there are losses associated with the inductor. These losses include core loss and AC- and DC-winding loss,

RIGHT Figure 5: **LMG5200 vs Si at different frequencies**





LEFT Figure 6: **Calculated efficiency comparison between the GaN FET power stage design at 1 MHz and Si FET design at 800 kHz**

which also should be taken into account when calculating system efficiency.

Efficiency improvements compared to Silicon

Figure 5 shows the efficiency delta between a 48 V:12 V LMG5200 buck and 80 V Si MOSFET- based buck. The LMG5200 is switching at 1 MHz while the Si-based implementation is switching at 250 kHz and 800 kHz, respectively. As shown, the LMG5200 has higher efficiency versus load than the Si solution switching at a lower frequency (1 MHz vs 800 kHz). This is indicative of the fact that switching and conduction losses in the GaN FET power stage are much lower compared to the similarly rated Si MOSFET. When the Si MOSFET-based converter is redesigned for a 250 kHz switching frequency, higher efficiency for Si designs at light loads as expected can be seen. However, as the load increases to 4 A, the GaN FET power stage switching at 1 MHz shows a much higher efficiency.

A comparison with Si at 800 kHz shows that the efficiency of the GaN FET power stage is much higher across a wide load range, even while switching at 1 MHz. A comparison of the efficiencies observed in the hard-switched buck with the calculated results indicates that the calculations are within the margin of error for the simplified model (Figure 6).

Conclusions

Power GaN FETs, due to their extremely low gate charge and output capacitance, can be switched at extremely high speeds with significantly reduced switching losses and improved efficiency compared to Silicon FETs. The LMG5200, an 80 V GaN FET power stage, has been optimized for applications requiring high efficiency and/or small form factor. Its advanced package greatly simplifies manufacturability and board design while reducing costs. The LMG5200 can improve the performance across a wide variety of applications while reducing adoption risk. These applications include multi-MHz synchronous buck converters, Class D amplifiers for audio, and 48 V to POL converters for data communications and telecommunications servers. GaN FET power stage devices provide significant efficiency benefits across a wide load range while improving switching frequency and power density.

Literature

Texas Instruments Enters GaN Power Market with 80-V Halfbridge (www.power-mag.com/news.detail.php?STARTR=10&NID=224)

TI White Paper: GaN FET module performance advantage over silicon

Texas Instruments Enters GaN Power Market with 80-V Halfbridge

Texas Instruments (TI) introduced on March 13 a 80-V / 10-A integrated GaN FET power-stage prototype, which consists of a high-frequency driver and two GaN FETs in a half-bridge configuration – all in a quad flat no-leads (QFN) package. TI does not introduce a GaN switch – instead the company relies on Enhancement-Mode GaN switches from Efficient Power Conversion (www.epc-co.com) and its already supplied GaN drivers.

According to TI Enhancement-Mode GaN power FETs can provide significant power density benefits over Silicon MOSFETs in power converters but pose new challenges for designers. TI solves the challenges of driving GaN power FETs with a family of drivers – UCC27611, a 4 A/6 A high-speed, optimized single gate driver, LM5114, a 7.6 A single low-side driver with independent source and sink outputs – and the LM5113, a 100 V integrated half-bridge driver for GaN power FETs. Compared to discrete implementations, these drivers provide significant PCB area savings to achieve high power density and efficiency while simplifying the task of driving GaN FETs reliably.

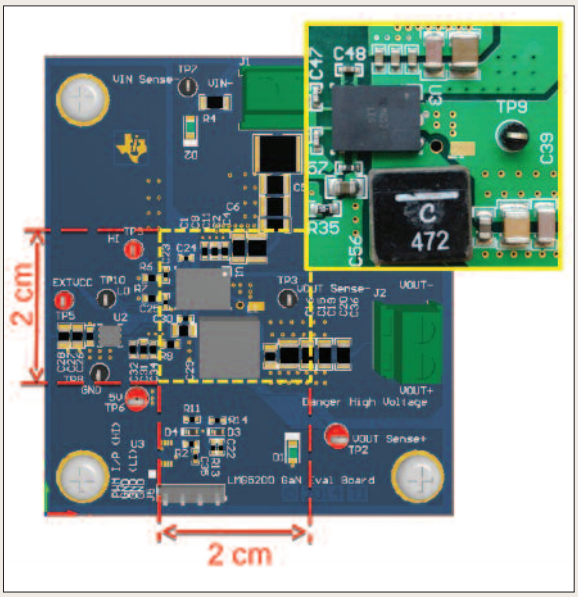
The new LMG5200 GaN FET power stage will help accelerate market adoption of GaN power-conversion solutions that provide increased power density and efficiency in space-constrained, high-frequency industrial and telecom applications.

Typically, designers who use GaN FETs that switch at high frequencies must be careful with board layout to avoid ringing and electromagnetic interference (EMI). The dual 80-V power stage prototype eases this issue while increasing power-stage efficiency by reducing packaging parasitic inductance in the critical gate-drive loop. The LMG5200 features multichip packaging and is optimized to support power-conversion topologies with switching frequencies up to 5 MHz.

Also the 6-mm x 8-mm QFN package requires no underfill, which significantly simplifies manufacturing. The reduced footprint solidifies the value of GaN technology and will help increase adoption of GaN power designs in many new applications, ranging from high-frequency wireless charging applications to 48-V telecom and industrial designs.

For quick evaluation the LMG5200 EVM board is a small easy to use power stage with an external PWM signal. The EVM is suitable for evaluating the performance of LMG5200 power stage in many different DC/DC converter topologies. It can be used to estimate the performance of LMG5200 to measure efficiency. The module is capable of delivering a maximum of 10 A of current however adequate thermal management (forced air, running at low frequency etc) should be followed to ensure that the temperature is not exceeded. The EVM is not suitable for transient measurements as it is an open loop board. In addition to ordering the EVM, designers can get started faster using PSpice and TINA-TI models for the LMG5200 to simulate the performance and switching frequency advantages of this technology. Prototype samples of the GaN power stage are available to purchase in the TI Store. The LMG5200 is priced at $50 each with a maximum purchase of 10 units. The LMG5200 EVM is available for $299.

GaN FET power-stage consisting of a driver and two GaN FETs in a half-bridge configuration – all in a quad flat no-leads (QFN) package



The LMG5200 EVM board is a small easy to use power stage (buck converter) with an external PWM signal