Next Generation in Digital Power Supply Control

The continued adoption of digital control in power conversion and distribution is accredited to the flexibility and increased efficiency it delivers. However, these gains do not come free; they are the result of complex and sophisticated algorithms working at increasingly higher processing speeds in order to optimize the efficiencies of switching power supplies. **Tom Spohrer, Product Marketing Manager MCU16 Division, Microchip Technology, Phoenix, USA**

The optimization of switch-mode power supplies is increasingly seen as a significant opportunity for manufacturers to deliver more efficiency in end-products. The challenge, however, is maintaining that efficient operation across a wide and varying array of load conditions. The introduction of Power Factor Correction (PFC) introduced a new age of efficiency targets – both regulatory and market-driven – and it has become a major focus for semiconductor providers, striving to continually improve their solutions to digital power control. Software-based algorithms provide the potential for more flexible and efficiency solutions, when coupled to the right hardware.

Digital control

Power conversion invariably starts with an AC source, which is then rectified to DC and further stepped down through various intermediate voltages until eventually reaching the Point of Load (POL). The Power Factor of a system is the ratio between the true and apparent power; the closer to unity the ratio the more efficient the system. PFC is the method employed to restore the ratio to unity (or as close as possible) and may be achieved using capacitors, but it is increasingly viable to apply PFC using Buck, Boost or Buck/Boost conversion under digital control. Moving between the analog and digital domains typically adds additional latency; the control loop delay, and it describes the total time taken to apply a change to the conversion and measure the effects of that change. Under steady-state conditions this would be relatively simple but under variable loads the speed with which the control loop executes directly influences the PFC and overall efficiency.

The challenge increases when the POL stage requires low voltage but high current levels, as is often the case in modern embedded systems. Today, microprocessors, FPGAs and ASIC invariably operate from low voltages – 3.3 V and below – but require much higher current in order to meet their overall power demands. Furthermore, the demands will vary significantly based on the operating requirements. As shown in Figure 1, the use of digital control can be applied throughout the entire power conversion flow in order to introduce not only greater efficiency but the flexibility to sustain that efficiency across a wide range of loads.

This is enabled though the continued development of sophisticated algorithms, including adaptive algorithms that can react to changes in load levels, and non-linear and predictive algorithms that can improve the dynamic response under transient conditions. And as semiconductor technology develops, manufacturers are able to employ this to increase the performance of digital control solutions, allowing higher switching

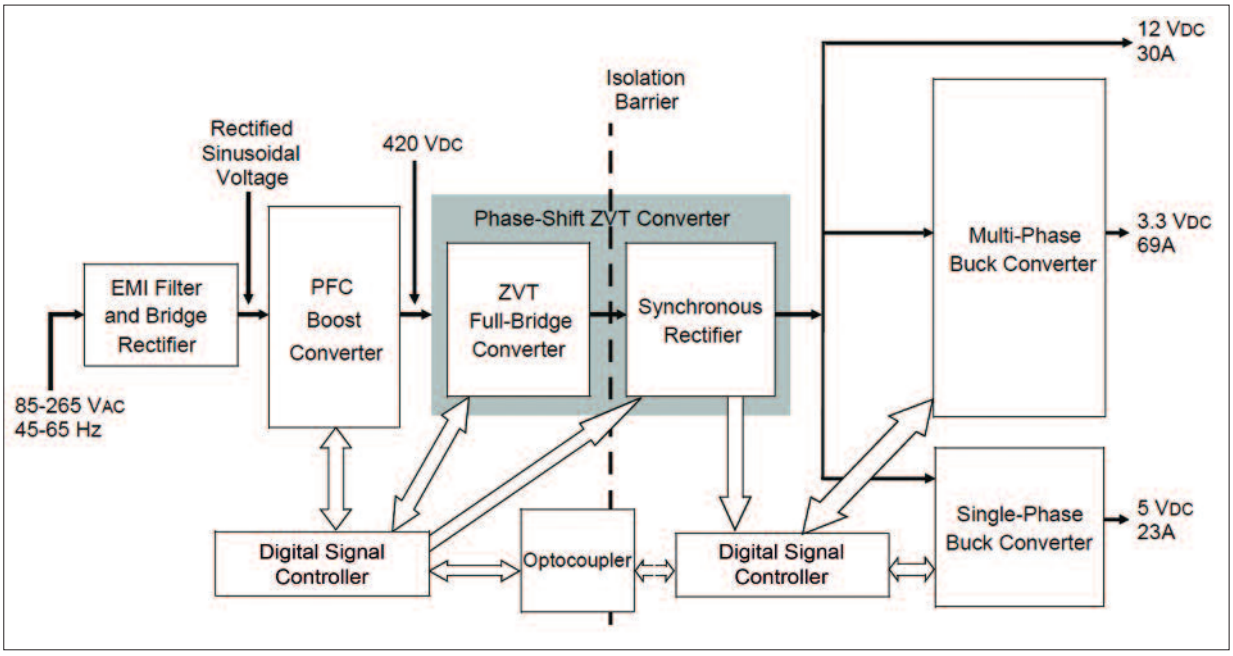

Figure 1: **Detailed SMPS AC/DC reference block diagram**

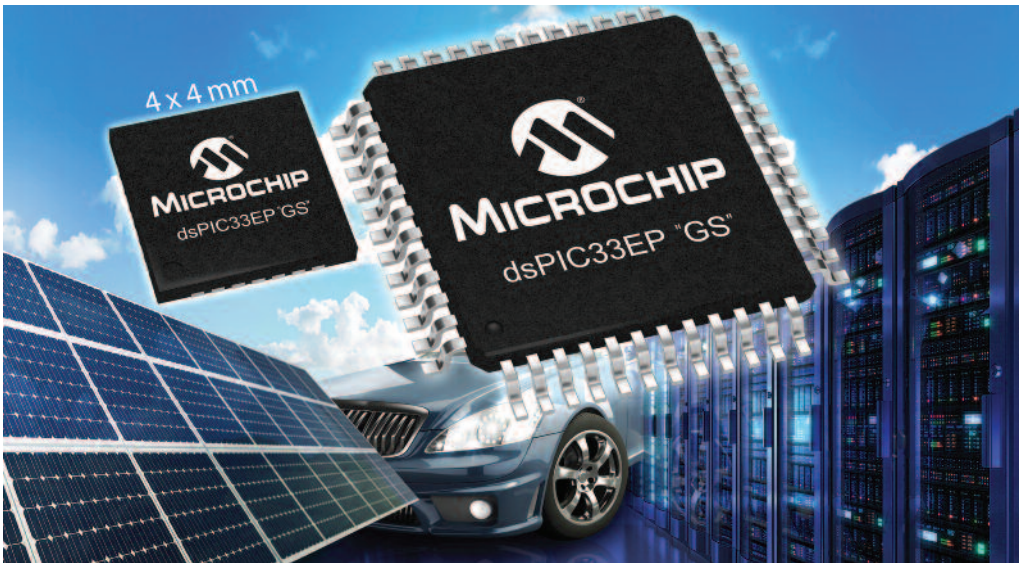

Figure 2: The third generation of Microchip's dsPIC33 GS family, delivers 70 MIPS and includes features such as context-selected working register sets that further increase performance for digital power applications

frequencies that result in not only greater efficiency but higher power density.

Digital signal controllers

The emergence of digital control in areas such as power conversion, motor drives and similar applications where adaptive control is advantageous, has led to the development of Digital Signal Controllers (DSCs). These devices merge the benefits of a Digital Signal Processor (DSP); extensively used in audio and video processing, and the venerable Microcontroller (MCU), to create a new class of device tuned to executing control algorithms that would be too complex for a traditional MCU, with the peripherals and interfaces not typically present in a DSP.

There is an increasing number of DSCs on the market, all of which strive to deliver on these demands. Those that best deliver exhibit a continued roadmap of architectural improvement, which allow developers to further improve the speed and accuracy of the control loop in their application, and enable them to take full advantage of the latest developments in control algorithms.

DCSs are essentially the definitive mixed-signal solution; they must combine digital processing with analog peripherals. Achieving an overall solution requires both domains to function together seamlessly, which is why fully integrated devices offer the best approach. Combining both analog and digital technology on a single device can, however, introduce design compromises, but improving performance in both domains in a balanced way is critical in delivering better solutions.

The essential components of a DSC are a core capable of efficiently executing signal processing algorithms, coupled with signal conversion in the form of one/multiple Analog/Digital Converters (ADCs), along with some form of Pulse Width Modulation (PWM) output used to drive power transistors such as MOSFETs in the Buck/Boost conversion circuit(s). Bringing these elements together in a single architecture that supports fast control loops is the key to building a successful DSC, which in turn is the heart of efficient AC/DC and DC/DC power conversion.

Mixed signal solution

The third generation of Microchip's dsPIC33 GS family, the dsPIC33EP GS (Figure 2), delivers increased performance in these critical areas over the second generation. The core now delivers 70 MIPS (up from 50 MIPS) but also includes features such as context-selected working register sets that further increase performance for digital power applications beyond what the increased raw MIPS rating might suggest. By adding two additional working register sets the core now supports almost instantaneous context switching.

The performance of the analog peripherals has also been improved relative to previous generations. For example, products in this family offer up to five 12-bit ADCs, with the ADC conversion latency reduced from 600 ns to 300 ns. Together, these improvements enable a three-pole-three-zero compensator latency to be reduced from around 2 µs to less than 1 µs thereby reducing phase erosion to improve stability. Faster control loops also allow for higher switching frequencies and better transient response. The resulting efficiency gains made possible by the increased performance also lead to increased power density; power supplies can be designed to be smaller, using fewer and smaller discrete passive components.

A further architectural improvement in the 'GS' is the introduction of dual flash memory partitions, supporting a feature known as Live Updates. This allows a control algorithm, or any other software executed by the DSC, to be updated in the field while the power supply remains fully operational; the new software is loaded in to the second, non-operational, flash partition and, when verified, the core switches to executing from the second flash partition. This is a feature that is particularly welcome in high-availability applications, such as server power supplies, where even small efficiency gains can result in large reductions in operational costs. Without the live update feature, such applications would be left with either updating the software during scheduled (or unscheduled) maintenance breaks in operation, or leaving the code unmodified and missing out on the potential benefits. Both of these options would be unwelcome in the server environments, of course.

Conclusion

The digital control of power conversion continues to develop, progressively replacing analog control due to the flexibility and potential efficiency gains it presents. While the complexity is undoubtedly a consideration for developers, the benefits can be persuading. Regulatory requirements aside, the use of digital control can clearly deliver better power conversion solutions and, with the introduction of Live Update, offer an upgrade path for solutions already deployed – even in high availability applications. DSCs represent the pinnacle of digital control in this and many other applications where complex algorithms meet high performance analog peripherals. The 'real world' of mixed signal solutions continue to offer an opportunity for performance gains at every level; fully integrated, advanced programmable solutions like the dsPIC33EP GS family represent the leading-edge of DSC technology, and will provide power supply developers with the next generation in control.