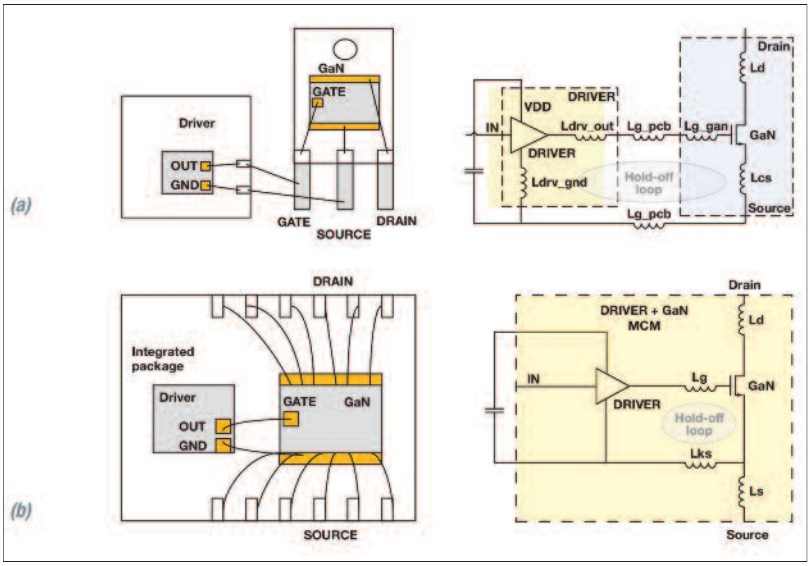
Optimizing GaN Performance with Integrated Driver

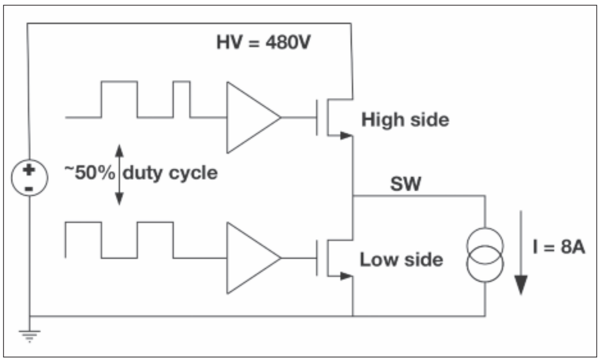
Gallium Nitride (GaN) transistors can switch much faster than Silicon MOSFETs, thus having the potential to achieve lower switching losses. At high slew rates, however, certain package types can limit GaN FET switching performance. Integrating the GaN FET and driver in the same package reduces parasitic inductances and optimizes switching performance. Integrating the driver also enables the implementation of protection features. **Yong Xie, IC design engineer; Paul Brohlin, Design and system manager, GaN and Next team, Texas Instruments, USA**

GaN transistors have switching performance advantages over Silicon MOSFETs given their lower terminal capacitances for the same on-resistance and lack of a body diode with reverse-recovery loss. Because of these features, GaN FETs can switch at higher frequencies, improving power density and transient performance while maintaining reasonable switching losses.

GaN devices are packaged as a discrete device and driven with a separate driver, because GaN devices and drivers are based on different process technologies and may come from different manufacturers. Each package will have bond wires and/or leads that introduce parasitic inductance, as shown in Figure 1a. When switching at high slew rates of tens to hundreds of volts per nanosecond, these parasitic inductances can cause switching loss, ringing and reliability issues.



ABOVE Figure 1: **A GaN device driven by a driver in a separate package (a); and an integrated GaN/driver package (b)**



RIGHT Figure 2: **Simplified diagram of the half-bridge circuit for simulations**

Integrating the GaN transistor with its driver (Figure 1b) eliminates common-source inductance and significantly reduces the inductance between the driver output and GaN gate, as well as the inductance in driver grounding. package parasitics. Optimizing these parasitics in an integrated package reduces parasitic issues and enables excellent switching performance at slew rates higher than 100 V/ns.

Simulation setup

To simulate the effects of parasitic inductances, we used a depletion-mode GaN half-bridge power stage in a direct-drive configuration (Figure 2). We set up the half bridge as a buck converter, with a bus voltage of 480 V, a 50 percent duty cycle with 50 ns of dead time (V_{OUT} = 240 V) and an inductor current of 8 A. The GaN gate is directly driven between the on and off voltage levels. A resistive drive sets the turn-on slew rate of the GaN device. A current source emulates an inductive load attached to the switch (SW) node in a continuous-conduction-mode (CCM) buck converter.

One of the most important parasitic elements in high-speed switching is the common-source inductance (L_{CS} in Figure 1a), which limits the slew rate of the device's drain current. In a conventional TO-220 package, the GaN source is brought out through bond wires to a single lead, where both the drain current and gate current flow. This common-source inductance modulates the gate-source voltage as the drain current changes. The common source inductance – including bond wire and package lead – can be higher than 10 nH, limiting the slew rate (di/dt) and increases switching losses.

With the integrated package shown in Figure 1b, the driver ground is wire-bonded directly to the source pad of the GaN die. This Kelvin source connection

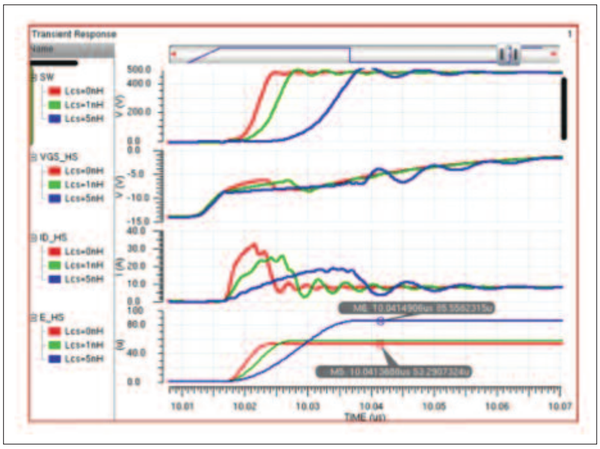


Figure 3: High-side turn on with different common-source inductance (red = 0 nH, green = 1 nH, blue = 5 nH). E_HS is the integration of V_{DS} and I_{DS} of the high-side device over time (energy consumption)

minimizes the common-source inductive path shared between the power loop and gate loop, allowing the device to switch at much higher current slew rates. A Kelvin source pin can be added to a discrete package; however, the additional pin makes it a nonstandard power package. The Kelvin-source pin also must be routed on the PCB back to the driver package, increasing gate-loop inductance.

Figure 3 shows hard-switching waveforms when a high-side switch turns on. With a 5-nH common-source inductance, the slew rate is cut in half due to the source degeneration effect. A lower slew rate translates to a longer transition time and leads to higher cross-conduction losses, as seen in the energy consumption plots. With a 5-nH common-source inductance, the energy loss increases from 53 µJ to 85 µJ, a 60 percent increase. Assuming a 100-kHz switching frequency, the power loss increases from 5.3 W to 8.5 W.

Gate-loop inductance includes both gate inductance and driver ground inductance. The gate inductance is the inductance between the driver output and GaN gate. With separate packages, gate inductance includes the driver output bond wire (L_{drv_out}), the GaN gate bond wire (L_{g_gan}) and the PCB trace (L_{g_pcb}), as illustrated in Figure 1a. Depending on package size, gate inductance can range from a few nH for a compact surface-mount package (for example, a quad flat no-lead) to more than 10 nH for a leaded power package (for example, the TO-220). If the driver is integrated with the GaN FET on the same lead frame (Figure 1b), the GaN gate is directly bonded to the driver output, which can reduce the gate inductance to less than 1 nH. Package integration also can significantly reduce driver ground inductance (from $L_{drv\_gnd} + L_{s\_pcb}$ in Figure 1a to L_{ks} in Figure 1b).

The reduction of gate-loop inductance has a great impact on switching performance, especially during turn-off when the GaN gate is pulled down with a resistor. The resistor needs to be low enough so that the device does not turn back on when its drain is pulled high during switching. This resistor forms an inductor-resistor-capacitor (L-R-C) tank with the gate-source capacitance of the GaN device and the gate-loop inductance. Equation 1 expresses the Q factor as:

$$Q = \frac{1}{R}\sqrt{\frac{L}{C}} \qquad (1)$$

With a larger gate-loop inductance, the Q factor increases and ringing becomes higher. This effect is simulated with a 1-Ω pull down to turn off the low-side GaN FET, which appears around 9.97 µs in Figure 4 where the gate-loop inductance is varied from 2 nH to 10 nH. In the 10-nH case, the low-side V_{GS} rings 12 V below the negative gate bias. This significantly increases the stress on the GaN transistor gate.

Gate-loop inductance also has a significant impact on hold-off capability. When the gate of the low-side device is held at the turn-off voltage, and the high-side device is switched on, the low-side drain-gate capacitance sources a large current into the gate's hold-off loop. This current pushes the gate up through the gate-loop inductance. Figure 4 illustrates this event at around 10.02 µs. As inductance increases, the low-side V_{GS} is pushed higher increasing the shoot-through current, which is visible from the high-side drain current plots (ID_HS). The shoot-through causes the cross-conduction energy loss (E_HS) to increase from 53 ?J to 67 µJ.

One way to mitigate gate stress is to increase the pull-down resistance which in turn reduces the Q factor of the L-R-C tank, according to Equation 1. Figure 5 shows simulations with a 10-nH gate-loop inductance and pull-down resistance (R_{pd}) swept from 1 Ω to 3 Ω. Although the gate undershoot is limited to within a few volts below the negative bias with a 3-Ω pull down, hold-off capability becomes worse, causing larger shoot-through current. This

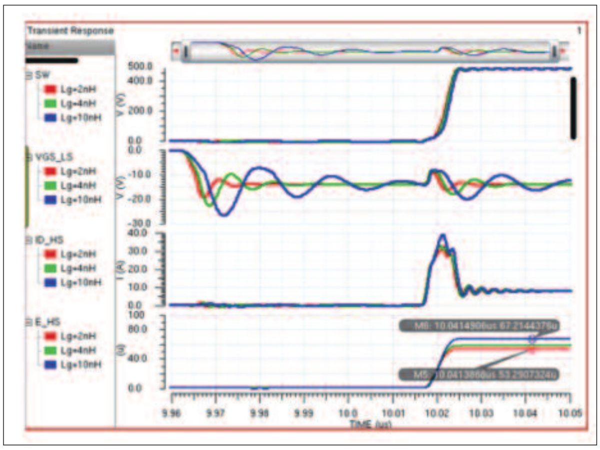


Figure 4: Low-side turn-off and high-side turn-on waveform at different gate-loop inductances (red = 2 nH, green = 4 nH, blue = 10 nH). E_HS is the high-side energy consumption

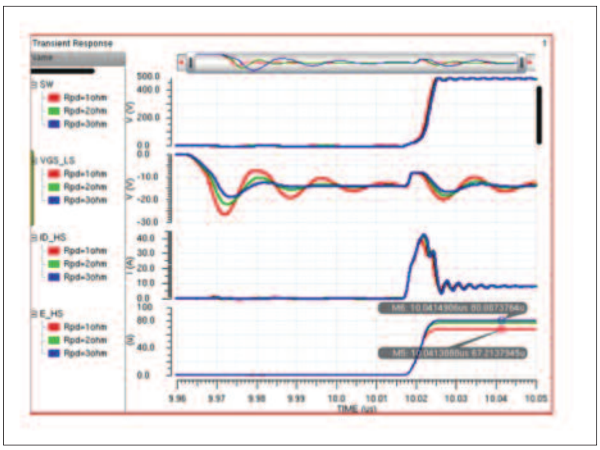


Figure 5: Simulation with 10-nH gate-loop inductance and pull-down resistance (R_{pd} = 1 Ω (red), 2 Ω (green) and 3 Ω blue). E_HS is the high-side energy consumption

is evident in the drain current plots. The E_HS energy plots show an additional 13-μJ loss in each switching cycle, an almost 60 percent increase from 53 ?J compared to a 2-nH gate-loop inductance and 1-Ω pull down (Figure 4).

Assuming a 100-kHz switching frequency, the power loss on the high-side device increases from 5.3 W to 8 W due to shoot-through caused by both high gate-loop inductance and high pull-down resistance. This additional power loss can make it very difficult to manage heat dissipation in the power devices and increases packaging and cooling costs. area An integrated GaN/driver package provides low gate-loop inductance and minimizes both gate stress and shoot-though risks.

GaN device protections

Having the driver mounted on the same lead frame as the GaN transistor ensures their temperatures are close, since the lead frame is an excellent heat conductor. Thermal sensing and over-temperature protection can be built within the driver that shuts the GaN FET down when the sensed temperature goes beyond the protection limit.

A series MOSFET or a parallel GaN sense FET can be used to implement over-current protection. Both require low-inductance connections between the GaN device and its driver. Since GaN is usually switched very fast with large di/dt, extra inductance in the interconnection can cause ringing and requires a long blanking time to keep the current protection from misfiring. Integrating the driver ensures minimal inductive connections between the sensing circuit and the GaN FET so that the current-protection circuit can react as fast as possible to protect the device from over-current stress.

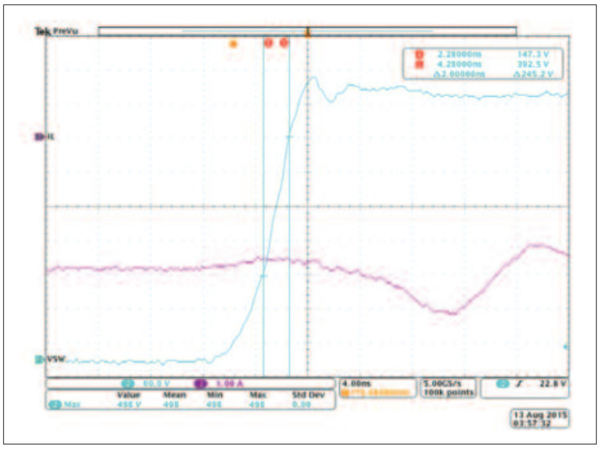


Figure 6: SW-node waveform of high-side turn on in a half-bridge buck (channel 2)

Figure 6 is the switching wave of a half-bridge created with two GaN devices in 8-mm by-8-mm quad flat no-lead (QFN) packages with an integrated driver. Channel 2 shows the SW-node when the high-side device is hard-switched at a slew rate of 120 V/ns at a bus voltage of 480 V. The optimized driver-integrated package and PCB limits the overshoot to under 50 V (waveform was captured with a 1-GHz scope and probes).

Conclusion

The package integration of a GaN transistor with its driver eliminates common-source inductance, thus enabling high current-slew-rates. It also reduces gate-loop inductance to minimize gate stress during turn-off and improves the device's hold-off capability. Integration further allows designers to build effective thermal- and current-protection circuits for GaN FETs.

Literature

"48 V GaN Point-of-Load Converter", Michael Seeman, Texas Instruments, Dallas, USA, Power Electronics Europe, July 2015, pages 29-31

TI showcased 600 V discrete GaN power FET and driver

At APEC, TI announced that they have leveraged existing manufacturing infrastructure and capabilities to qualify a 600-V GaN process. First product is an E-GaN FET with integrated driver in 8x8 QFN package. Building on years of expertise in manufacturing Silicon process technologies, TI has established a GaN-specific qualification methodology and application-relevant testing. With this 600-V process, TI will build out the portfolio of companion parts that will support high-voltage applications and new topologies such as UCD digital controller enabling 99 + percent efficient PFC – demonstrated at APEC. This 1 kW Totem-Pole PFC at 100-kHz frequency enables 30 percent lower volume vs. traditional designs and feature adaptive deadtime control due to UCD digital controller.

The TPS53632G is an analog controller, optimized for GaN in a 48 V/ 1 V POL application. Paired with TI GaN power stages and drivers, the controller can switch up to 1 MHz to minimize magnetic component size and reduce overall board space. The LMG5200 GaN power stage is designed specifically for this controller to achieve high frequency and efficiency as high as 92 percent with 48-V to 1-V conversion. Emerging applications such as 48 V-POL had a lot of interest. Google joined the Open Compute Project a few weeks ago and proposed a computer server-rack architecture based on a 48 V power-distribution bus to improve overall system efficiency. While the 48 V bus has been around for a long time, the push (and challenge) is for high-efficiency 48 V voltage regulators. EPC showcased TI's 48V-to-1V EVM which uses the LMG5200 GaN module (driver and FETs), announced at APEC last year, and the new TPS53632G.

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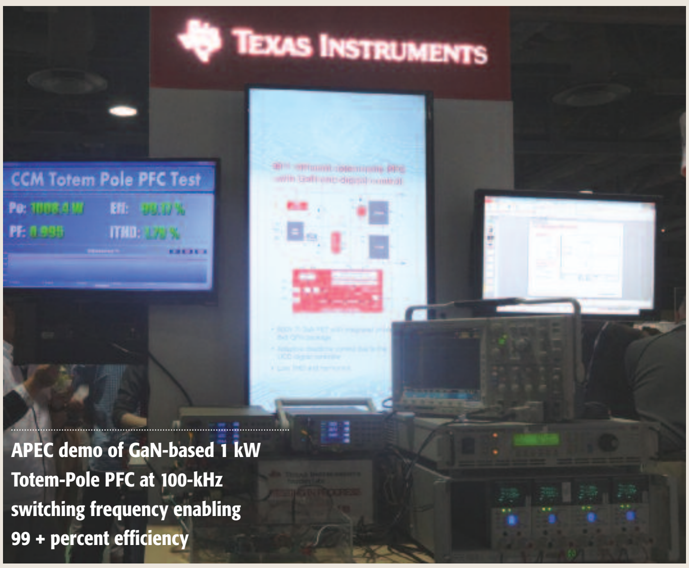

APEC demo of GaN-based 1 kW Totem-Pole PFC at 100-kHz switching frequency enabling 99 + percent efficiency