High Quality 150 mm SiC Substrates for Power Electronics Applications

Silicon Carbide (SiC) technology is being more broadly adopted by the power electronic market within applications rated at voltages of 600V or above, whereas silicon-based technology is still preferred for lower voltage class devices. The benefits of SiC devices over silicon-based counterparts are very well-known by the industry and reside in the high temperature resistance, high thermal conductivity and high critical field of SiC. All of these benefits translate into final systems with smaller form factors, higher efficiencies and lower requirements in cooling performance. This article will provide a current picture of the tremendous improvements made over the past few years in order to provide today a commercially available 4H-SiC 150 mm technology approaching and even overpassing the 100 mm technology performance.

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The emergence of 150mm SiC wafers has been a critical element to explain the wide market adoption of this technology, allowing economy of scale at a manufacturing standpoint together with the use of depreciated 150mm silicon production lines that could be converted to accommodate the silicon carbide specificities.

In order to gain even broader market adoption (using larger devices, bipolar devices, higher voltage rating devices) special attention has to be given to the decrease of extended crystal defects and the control of the surface shape and flatness which are key elements needed by lithography tools or designs used by the device manufacturers.

Figure 1: **The control of crystal stress during the growth process is key in order to minimize extended defect densities**

Control of defect densities

The control of crystal stress during the growth process is key in order to minimize extended defect densities and also to ensure proper control of the shape and the surface flatness of the sliced wafers used for device processing (figure 1). Different extended defects are known to be detrimental to the reliable operation of SiC devices: micropipes (MP), basal plane dislocations (BPD), threading screw dislocations (TSD) and threading edge dislocations (TED):

- Micropipes are killer defects which provoke a premature catastrophic device breakdown;
- BPD have an impact on the generation of stacking faults during the epitaxy process, leading to a drift in the forward voltage drop in bipolar PiN diodes;
- TSD and TED densities impact the reverse leakage current in Schottky barrier diodes.

The summary of the current status of Dow Corning defect density control is presented in Table 1.

Micropipes are no longer a problem to manufacture large area devices. We can achieve a mean micropipe density of less than 0.3/cm^2, very comparable to the low density observed in 100 mm wafers. Through optimization of the growth and seed selection processes very good control of the low micropipe defect density has been achieved.

In terms of basal plane dislocations,

Bulk Crystal			
Defect Metrics	**Units**	**100mm**	**150mm**
Median BPD density	cm^{-2}	400	800
Median TSD density	cm^{-2}	300	200
Median TED density	cm^{-2}	5200	3100
Median EPD density	cm^{-2}	5900	4100

Table 1: **Comparison of defect densities in 4H-SiC 100mm and 4H-SiC 150mm substrates**

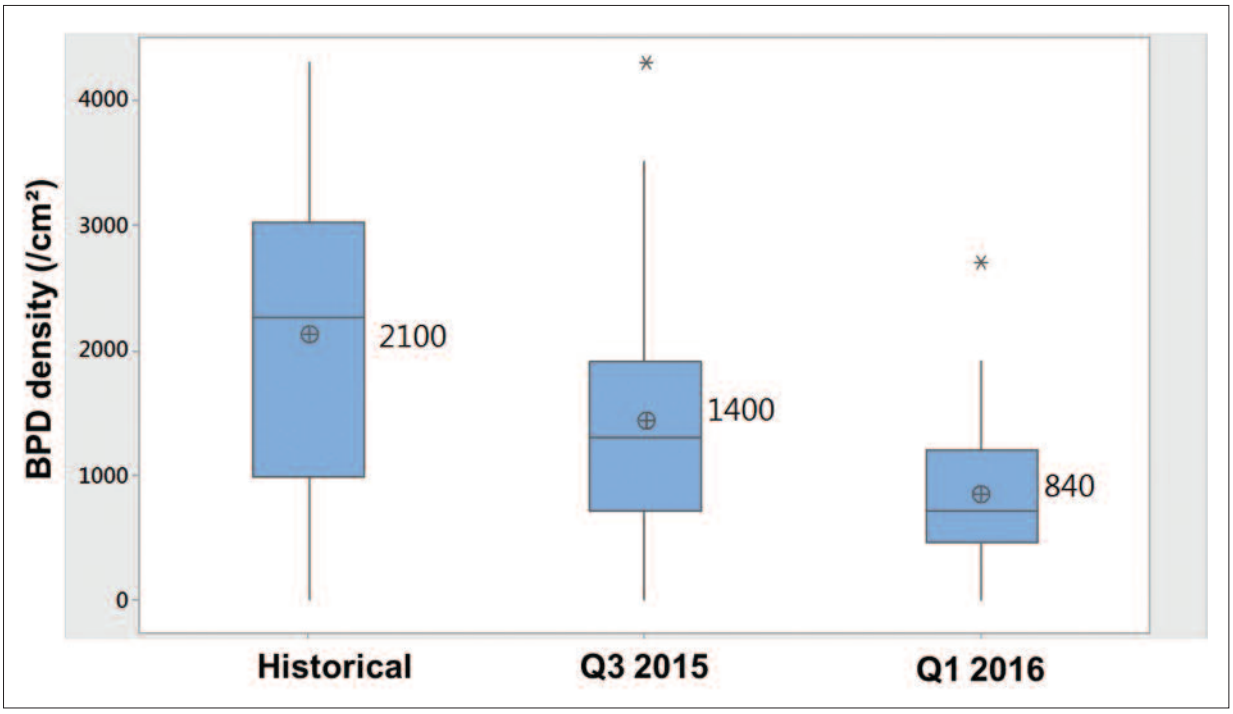

Figure 2: **Evolution over time of BPD density in 4H-SiC 150mm substrates**

the improvements made over the past months in the crystal growth process and wafering control have significantly decreased the median density and the manufacturing distribution has been drastically reduced (Figure 2). The current values are still twice higher than the median BPD density measured on 100 mm wafer, but based on the continuous decrease from the past, we expect that the BPD density will ultimately by at least on par with the 100 mm wafers in a near future.

The threading screw dislocation is very well controlled with a median value of 200/cm^2, better than the value for the 100 mm technology.

The threading edge dislocations dominate median total etch pit density of 150 mm substrates (similar behavior is true for 100 mm wafers). However, the 150 mm technology provides a lower median value compared to the 100 mm products.

The conclusion from this section is that the 150 mm technology developed by Dow Corning presents an overall lower defect density compared to the 100 mm substrates. The strong focus in reducing the defect density is a critical factor to ensure the broader adoption of SiC materials in the market.

Control of the shape and flatness

Together with the reduction of extended defects, it is important to optimize the shape of the wafers via optimized crystal growth, wafering, and polishing processes. This has been specifically challenging for the 150 mm SiC substrates as the thickness of the substrates (350 µm) has been kept identical while switching from the 100 mm wafers to the 150 mm diameter. This constraint is different from what has occurred in the Silicon technology where the wafer thickness increases together with the expansion of the diameter. Maintaining thickness while increasing diameter brings additional crystal stress control requirements for 150 mm SiC.

Nevertheless, Dow Corning has overcome these challenges and 150 mm SiC substrates are now available with bow, warp, and thickness variation metrics meeting the industry requirements for handling in the processing lines (Table 2). Typical bow and warp median values achieved in the mass production lines are -3 µm and 17 µm respectively whereas the total thickness variation falls to a median of less than 5 µm and the local thickness variation (SBIR) median reaches less than 2.5 µm.

Conclusions

Dow Corning has developed a 4H-SiC 150 mm growth and wafering process in order to meet the challenges of the electronics industry. The defect density is continuously decreasing, with today's 150 mm technology surpassing the incumbent 100 mm technology. This focus is a key factor to ensure a reliable device and high yield through the device processing and electrical wafer sorting steps. In parallel, the shape of the 150 mm wafers remain unchanged compared to the 100 mm substrates, even while the thickness has been kept constant, for an easy transfer of manufacturing processes from 100 mm to 150 mm technology.

Bulk Crystal			
Shape Metrics	**Units**	**100mm**	**150mm**
Median bow	µm	-0.9	-2.8
Median warp	µm	7.9	17.1
Median TTV	µm	2.4	4.7
Median SBIR	µm	1.3	2.4

Table 2: **Comparison of shape metrics in 4H-SiC 100 mm and 4H-SiC 150 mm substrates**