High Power with Complete Digital Control

It should come as no surprise to anyone that a the continuing adoption of Digital Power System Management (DPSM) within the communications and computer industries continues to be driven, in large part, to the high current levels demanded by the sub-20 nm ASICs and/or FPGAs that are at the core of their system architecture. **Tony Armstrong, Director of Power Product Marketing, Linear Technology Corporation, USA**

By way of example, consider the newest ASICs being used in the next generation data center switches; they enable a more flexible set of interfaces for ports carrying 100 Mbit to 100 Gbit/s Ethernet and 32 Gbit/s fiber channel traffic. This allows higher density of 100G ports to be placed into a single rack unit. Coupled with this, these sub-20 nm processes allow 20 plus Mbytes of memory to be placed on the ASIC itself, thereby potentially eliminating the need for external memory, saving board space and cost.

Nevertheless, the system architects of this type of communications equipment are constantly being pushed to increase the data throughput and performance of their systems as well as add functionality and features. Simultaneously, pressure is being applied to decrease the systems overall power consumption. For example, a typical challenge is to reduce overall power consumption by rescheduling the work flow and moving jobs to underutilized servers, thereby enabling shutdown of other servers. To meet these demands, it is essential to know the power consumption of the end-user equipment. Thus, a properly designed digital PSM can provide the user with power consumption data, allowing for smart energy management decisions to be made. This is a key requirement for data centers where the electricity costs for the HVAC systems that keep the internal ambient temperatures under control are significant.

System challenges

When digital power is done correctly, it can reduce equipment power consumption, shorten time to market, have excellent stability and transient response, and increase overall system reliability.

Complex multi-rail systems can be efficiently developed using a comprehensive development environment with intuitive graphical user interface (GUI). Such systems also simplify in-circuit testing (ICT) and board debug by enabling changes via the GUI instead of soldering in "white wire" fixes. Another benefit is the potential to predict power system failures and enable preventive measures, thanks to the availability of real-time telemetry data. Perhaps most significantly, DC/DC converters with digital management functionality enable designers to develop "green" power systems that meet target performance (compute speed, data rate, etc.) with minimum energy usage at the point of load, board, rack and even installation levels, reducing infrastructure costs and the total cost of ownership over the life of the product.

Many telecom and datacom systems are powered via a 48 V backplane. This voltage is normally stepped down to a lower intermediate bus voltage of typically 12 V to 3.3 V to power the racks of boards within the system. However, most of the sub-circuits or ICs on these boards are required to operate at voltages ranging from sub-1 V to 3.3 V at currents ranging from tens of milliamps to hundreds of amps. As a result, point-of-load (PoL) DC/DC converters are necessary to step down from the intermediate bus voltage to the desired voltage required by the sub-circuits or ICs. These rails have strict requirements for sequencing, voltage accuracy, margining and supervision.

There can be as any many as 50 PoL voltage rails in a telecom system and system architects need a simple way to manage these rails with regards to their output voltage, sequencing and maximum allowable current. Certain processors demand that their I/O voltage rise before their core voltage, alternatively certain ASIC and DSPs require their core voltage rise before their I/O. Power down sequencing

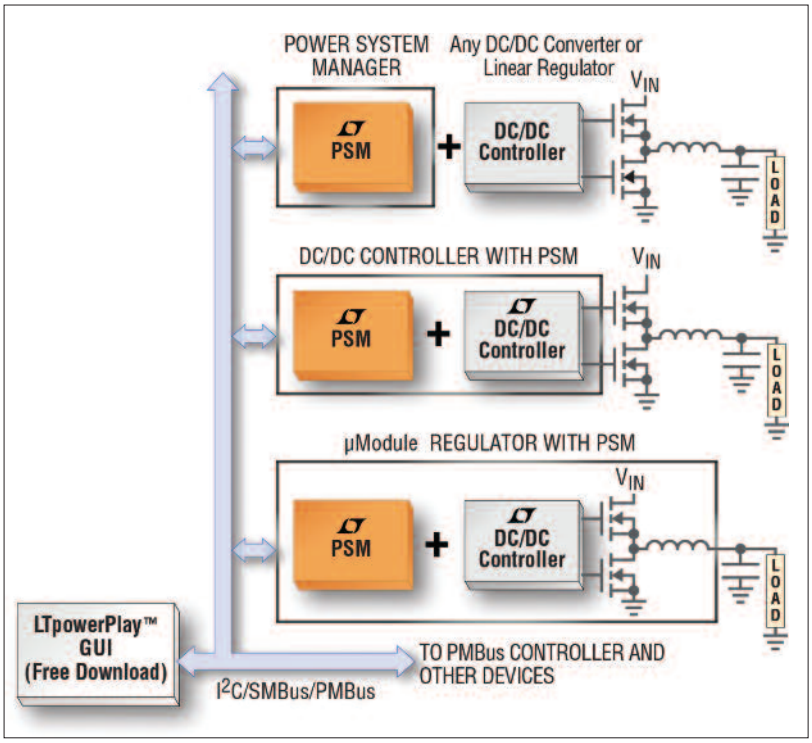

Figure 1: Typical digital power system management system configuration

is also necessary. Designers need an easy way to make changes to optimize system performance and to store a specific configuration for each DC/DC converter in order to simplify the design effort.

Furthermore, in order to protect expensive FPGAs, ASICs and DSPs from the possibility of an over-voltage condition, high-speed comparators must monitor the voltage levels of each rail and take immediate protective action if a rail goes out of its specified safe operating limits. In a digital powered system, the host can be notified when a fault occurs via the PMBus alert line and dependent rails can be shut down to protect the powered devices such as an FPGA. Achieving this level of protection requires reasonable accuracy and response times on the order of tens of microseconds.

It was because of these challenges that a PSM product line that includes synchronous step-down DC/DC controllers with integrated power FET gate drivers and comprehensive power management features accessed via the I²C-based PMBus has been developed. These include precision references and temperature-compensated analog current-mode control loops offering ±0.5% DC accuracy, easy compensation that is calibrated to be independent of operating conditions, cycle-by-cycle current limit, and fast and accurate current sharing and response to line and load transients without any of the ADC quantization-related errors found in products utilizing "digital" control. Some of these also incorporate 16-bit data acquisition systems that provide digital read back of input and output voltages and currents, duty cycle and temperature. Also included is a fault logging capability via an interrupt flag along with a "black box" recorder that stores the state of the converter operating conditions just prior to a fault. Finally, multi-rail system development is facilitated though LTpowerPlay® development software and GUI interface.

Simple solutions for complex problems

So what does the system architect have to do in order to configure a digital power

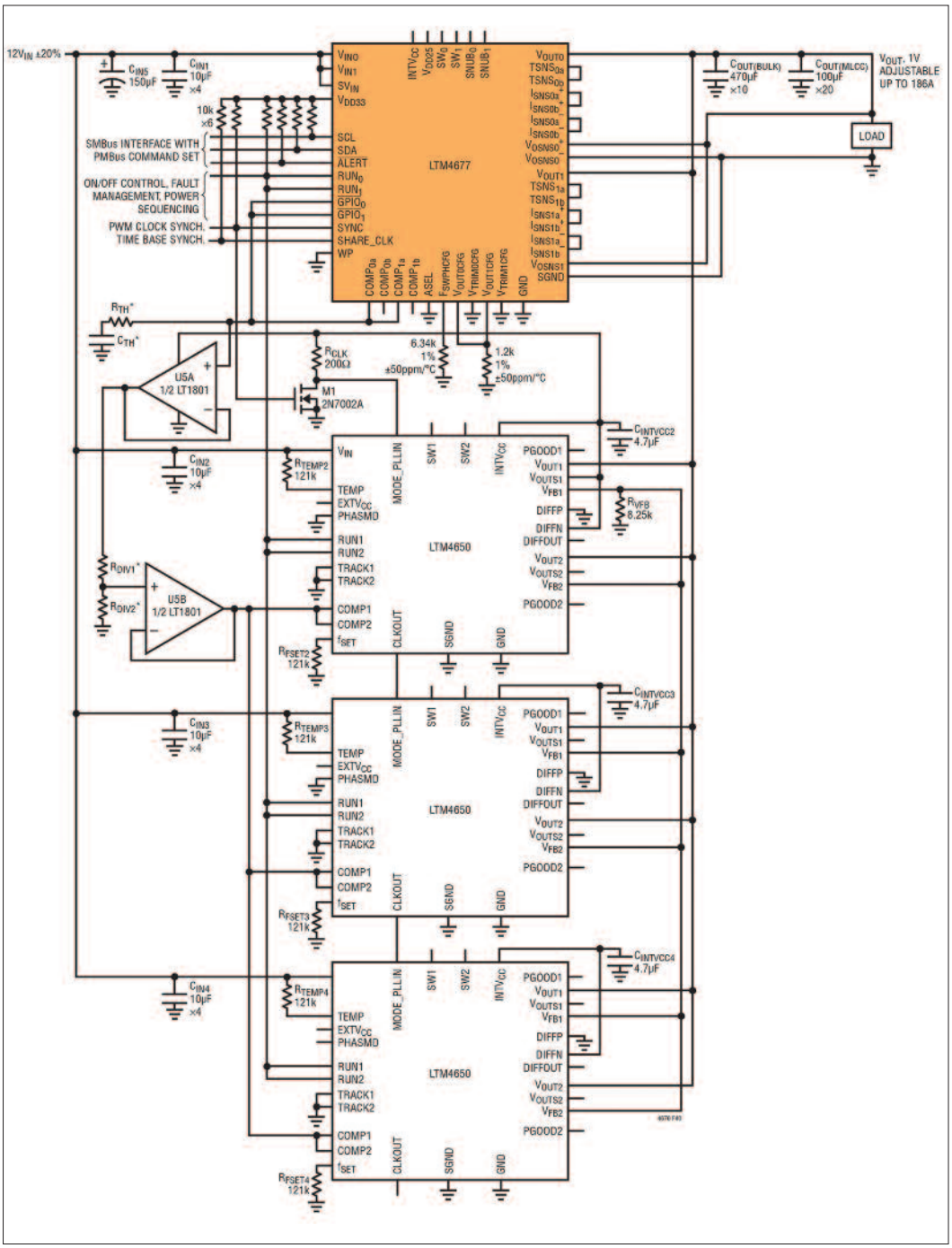

Figure 2: A combination of 1 LTM4677 DPSM module & 3 LTM4650 modules delivers 186 A at 1 V from a nominal 12 V input

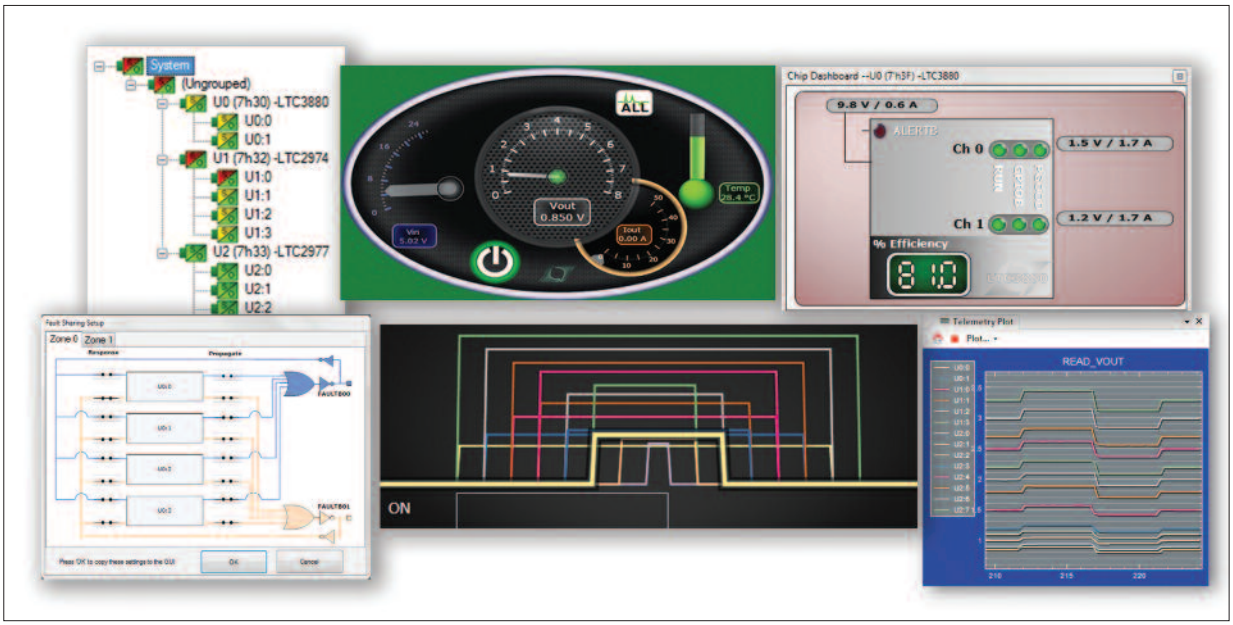

Figure 3: A snapshot of a typical dashboard screen shot of the LTpowerPlay GUI

system management solution for their end product? One of the primary objectives will be to design a system so that it can be easily configured and monitored via a digital communications bus. This will be achieved by utilizing one of the following; I²C, SMBus or PMBus. Either of these buses can enable on-demand telemetry capability to set, monitor, change and log power parameters of any PoL converter configuration within the system. A simplified snapshot of such a system is shown in Figure 1.

As can be seen in this example, the PoL converters illustrate 3 different topology configurations. At the top of the figure, a power system manager chip is used alongside a conventional DC/DC converter. The DC/DC converter can be of any topology and have any degree of integration since it is the power system manager that will allow it to be interfaced, controlled and monitored via the communication bus. The middle PoL converter demonstrates an increased level of integration, namely, that the DC/DC converter has the power system management built-in (in the same package). And finally, the bottom PoL converter is a compact module which incorporates the power system manager, the DC/DC converter and all its associated external components into a single form factor (Linear calls these a µModule® regulator).

Linear's µModule DC/DC regulators can provide a simple and effective way to deliver both high power outputs and DPSM capability. Since many of the regulators can be easily paralleled for high current outputs with per channel current matching within a nominal 1 % of each other, thereby mitigating the potentials for hot spots. Moreover, only one of the µModule regulators needs to contain DPSM capability, since it can supply the complete digital interface even if the uModules in parallel does not have DPSM inherent within them. Figure 2 shows an application schematic of one LTM4677 (36 A DPSM µModule) in parallel with 3 LTM4650s (50 A µModules).

Universal GUI for DPSM

A key advantage of a system architected with DPSM products is that with the right GUI it is easy to communicate with each individual PoL converter within in the system. So, from the onset, Linear decided to develop a GUI that was a complete development platform which could be easily used with all of the different types of products it offered in its DPSM product portfolio – the LTpowerPlay windows based development environment.

Not only does this software make is easy to control and monitor multiple Linear PMBus-enabled devices simultaneously, it also allows modification of the DC/DC converters configurations in real time be downloading system parameters to the internal EEPROM of the individual devices. This reduces design development time by allowing system configurations to be adjusted in software rather than resorting to the time honored tradition of swapping out components and rewiring boards. Once an end system has been deployed in the field, such as a data center, then the system can be adjusted real time by an overseer by simple updating operation parameters of the PoL converters via an applicable interface using this GUI. Figure 3 shows a typical screen shot of LTpowerPlay dashboard that a user would see when interrogating their system.

All Linear PMBus products are supported by this software development system which can help designers quickly debug systems both during initial development and then when they are installed at a user's site. It quickly and easily allows monitoring, control and adjustment of supply voltages, limits and sequencing. Furthermore, production margin testing is easily performed using a couple of standard PMBus commands.

Conclusion

Having DPSM capability in today's datacom and telecom systems provides a system architect with an simple and powerful way to deliver over 180 W of power to the 1.xV core voltages of the newest sub-20 nm ASICs and FPGAs with just 4 µModule regulators. Utilizing a combination of the LTM4677 and 3 LTM4650s in a multiphase configuration as shown in Figure 2, not only saves expensive PCB real estate, but reduces the amount of required cooling due to its overall operating efficiency. Furthermore, the software programmability of DPSM significantly reduces the debug time normally associated with such endeavors. This reduces infrastructure costs, as well as the total cost of ownership over the life of the product. And while it might take the fun out of the traditional solder iron and rewiring approach to debugging hardware systems, its convenience and time saving attributes are too compelling to be ignored.