Fast Heat Distribution Simulation And Visualization

A commonly used simulation method for heat distribution within the power module is the 3D FEM analysis. After the meshing of the solid model of the power module, entering power stimulus values and launching the simulation the heat distribution can be obtained. However the excitation signals are highly dependent on the application parameters. If an application parameter is changed the simulation must be run again, which can take a relatively long time for a full analyses. An alternative method is described below, that uses the linearity and superposition property of the heat equation for a quasi real time solution of the heat distribution problem. **Ernó Temesi, Application Engineering, and Vince Zsolt Szabó, Sr. Development Engineer, Vincotech. Hungary**

The life time of power modules is inversely proportional to the operating temperature of the semiconductors. The semiconductors should work at possible lowest temperature in the given application to minimize the power losses and thus the size of the required cooling equipment.

The semiconductors produce heat during operation that increases the temperature of the semiconductor chip and have an influence on the operating temperature of the other chips placed near them as well. This is called heat coupling. In case of dense layout the coupled thermal resistance can be significant. It is difficult to measure the exact value of heat coupling between chips, however it is easy to calculate using 3D finite element simulation software.

Heat equation solution

The heat distribution can be defined with a partial differential equation which describes the distribution of heat (or variation in temperature) in a given region over time.

$$\frac{\partial T}{\partial t} = \alpha\left(\frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} + \frac{\partial^2 T}{\partial z^2}\right) + \frac{1}{c_p \rho} q$$

where:

α - thermal diffusivity

$\frac{\partial T}{\partial t}$ - derivate of the temperature

$\left(\frac{\partial^2 T}{\partial x^2} + \frac{\partial^2 T}{\partial y^2} + \frac{\partial^2 T}{\partial z^2}\right)$ - Laplace operator (divergence of the gradient)

$\frac{1}{c_p \rho} q$ - heat source

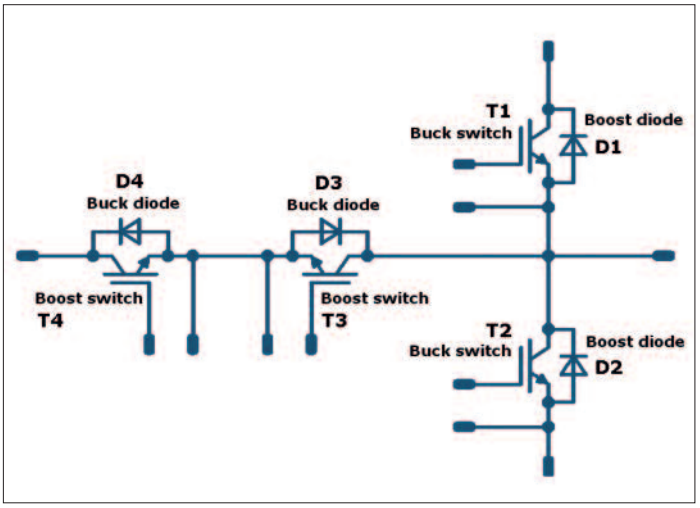


Figure 1: M260 schematic as a modeling example

From the equation arises the linear dependency between the heat source and the temperature rise:

$$q \rightarrow dT$$
$$2 * q \rightarrow 2 * dT$$

That is two times more heat will result in two times higher temperature rise. And the superposition of two heat sources:

$$q_1 \rightarrow dT_1$$
$$q_2 \rightarrow dT_2$$
$$q_1 + q_2 \rightarrow dT_1 + dT_2$$

That is the temperature rise generated by two heat sources is equal to the sum of the temperature rises generated by each heat source separately.

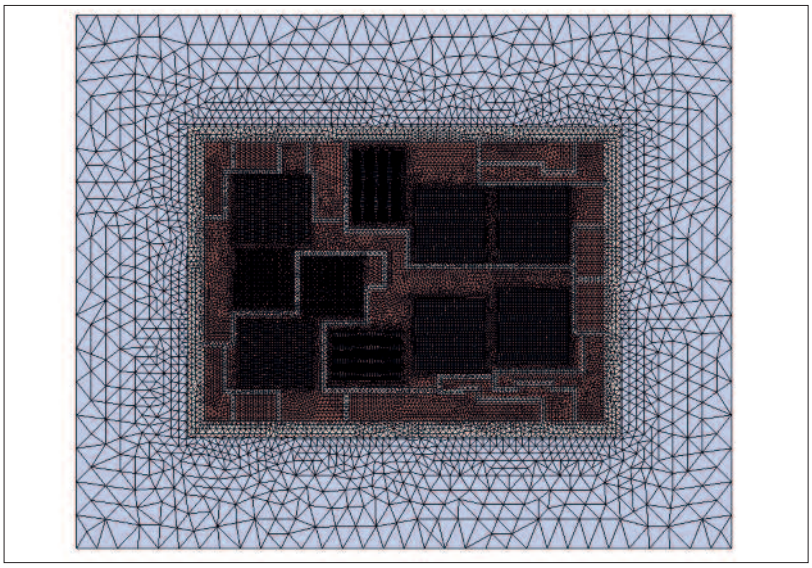
It is possible to modulate the temperature rise distribution caused by each heat source linearly with the actual power loss and finally superposition the temperature rises caused by all chips to get the total temperature rise distribution.

Temperature distribution and thermal resistance

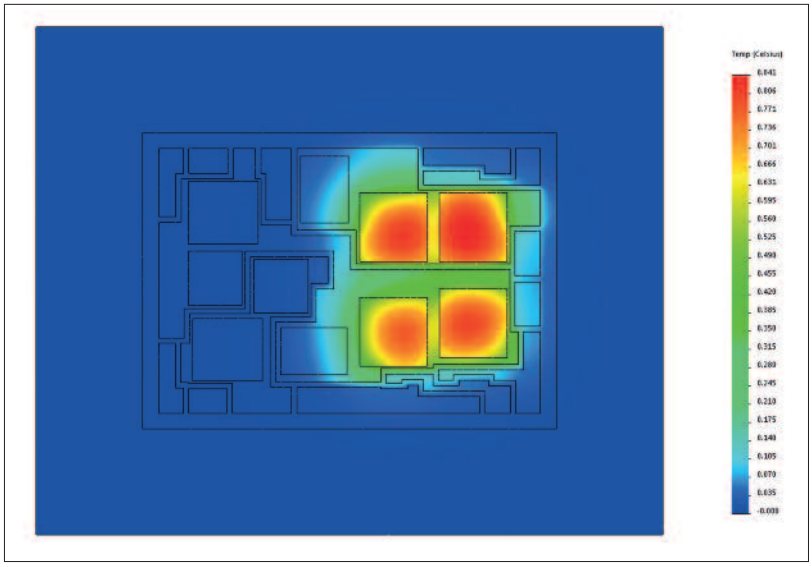
A three level MNPC inverter (M260) will be used as an example to show the procedure (Figure 1).

This module implements four different component electrical functions such as:

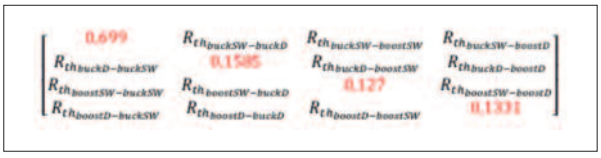
- 2 x buck switch (1200V; 2x40A chips paralleled)
- 2 x buck diode (600V; 75A)
- 2 x boost switch (600V; 75A)



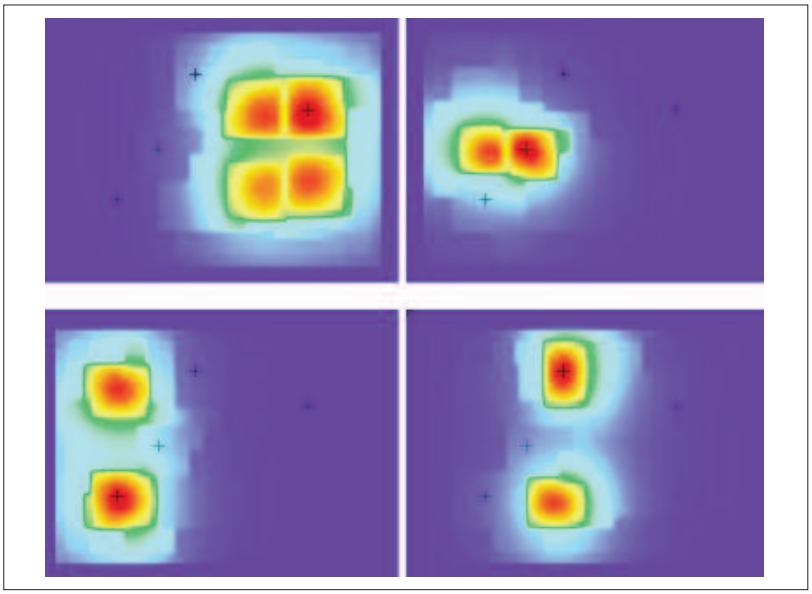
RIGHT Figure 2: **Mesh of the power module**



LEFT Figure 3: **Self R_{th} value of buck switch from 3D FEM simulation**



LEFT Figure 4: **Self R_{th} in the matrix**



LEFT Figure 5: **Maximum points for different electrical functions**

■ 2 x boost diode (1200V; 50A)

The following steps need to be done to get the heat distribution within the module:

1) Importing the modul layout into 3D FEM simulator;
2) creating the mesh (Figure 2);
3) exciting the chips of the same electrical functions by the same load conditions with unity power (1 W);
4) running one simulation for each function separately;
5) get maximum temperature to define R_{th} of chip and the temperature distribution (Figure 3).

The coordinates of maximum heated points can be obtained separately for the different electrical functions and the values define the self R_{th} values in the heat coupling thermal resistance matrix (diagonal) – see Figure 4.

The remaining values (coupled R_{ths}) in the matrix describes the measure how the components heat each other.

Defining cross-coupled thermal resistances

Knowing all the chip positions and the temperature rise caused by the neighboring chips the coupled R_{th} values can be also gained by reading color codes of the different positions for all electrical functions (Figure 5). The black crosses indicate the coordinates of the virtual maximum temperature points.

The R_{th} matrix gives an easy and fast way for calculating each chip temperature of the power module under any load

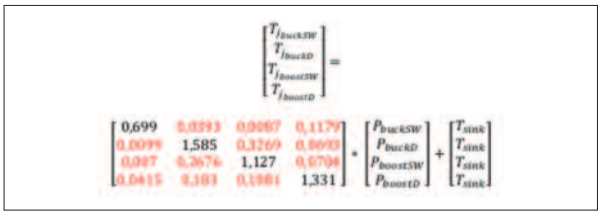


Figure 6: **Self (black) and cross-coupled (red) R_{th} matrix**

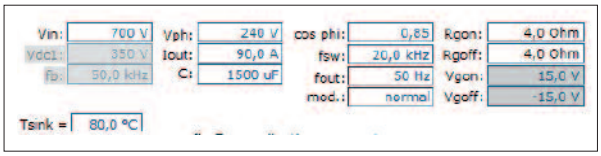


Figure 7: **Application parameters**

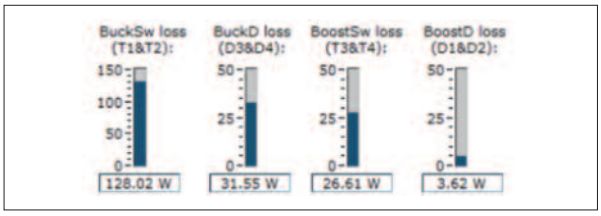


Figure 8: **Heat power excitation values**

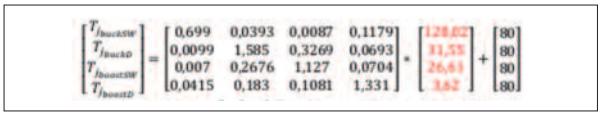


Figure 9: **Full matrix equation**

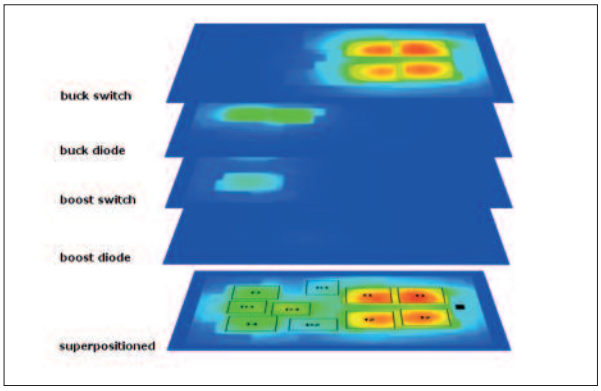


Figure 10: **Layered and superpositioned thermal distributions**

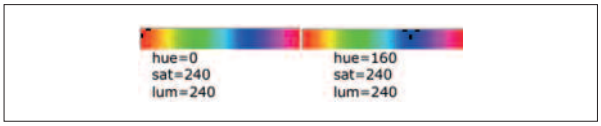


Figure 11: **Define linear color range**

condition (Figure 6).

Additionally by superimposing the temperature distributions caused by all functional components the total temperature distribution within the module is obtainable. The heating power for each function types is obtained from flowTHERM-M260 simulation launched with given application parameters (Figure 7). Heat powers for the specific application case is shown in Figure 8.

The temperature values for the functions are determined by substituting the heat power excitation values (Figure 9). By the superposition of all distribution layers caused by the functional components the total distribution can be gained (Figure 10). In the final distribution the colors are normalized to the T_{sink} heatsink (min) and to the allowed T_j maximal chip temperature (max) as shown in Figure 11. Thus each pixel temperature of the superpositioned picture can be read by a resolution of 1/160 due to the hue=0 ($T_{jmaxtot}$) and hue=160 (T_{sink}) range.

Conclusions

An alternative method as described above, which uses the linearity and superposition property of the heat equation, allows building power module loss and temperature simulators with very fast response to adjustments or changes in the application parameters. The simulation tool can easily be programmed to map the relations between virtual junction temperature of semiconductor chips inside the power module and a temperature sensing device (Figure 12). This information used in a real time temperature calculation of the application can be used for an accurate estimation of the virtual chip temperatures. As next steps the visualization of the fluctuation of the chip temperatures with the converters basic frequency is to be solved.

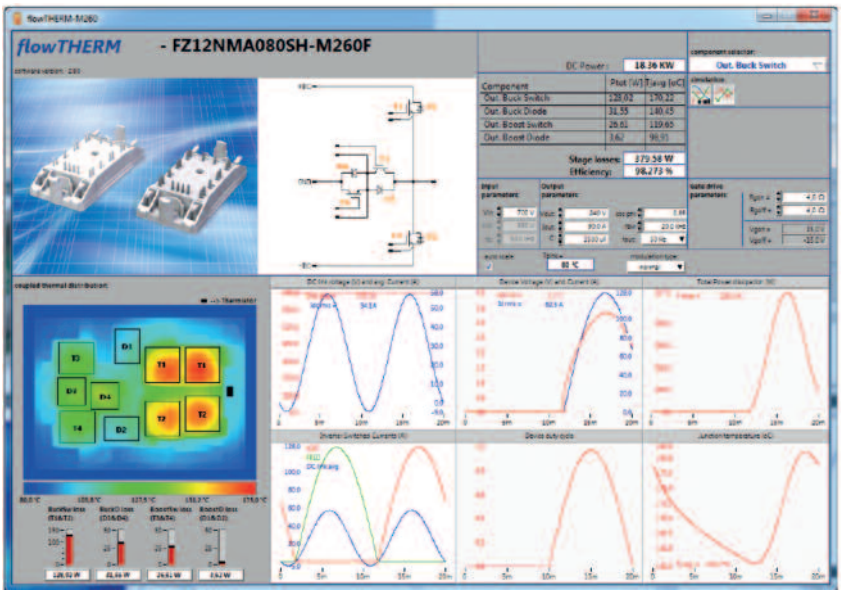


Figure 12: **Power module simulator with thermal distribution inside**