# 94%-Efficient Offline Flyback Switcher IC Family

Power Integrations announced its InnoSwitch™3 family of offline CV/CC flyback switcher ICs. The new devices achieve up to 94 % efficiency across line and load conditions, slashing power supply losses by a further 25 % and enabling the development of compact power supplies up to 65 W without heatsinks, according to the introduction of the new device family by **Andy Smith, Senior Product Marketing Manager, Power Integrations, Milpitas, USA[1]**

**InnoSwitch3 devices are intended for** power supplies with challenging energy consumption, footprint or thermal constraints, particularly those targeting mandatory Total Energy Consumption (TEC) specifications.

The InnoSwitch3 IC family is optimized into three application-specific series:

- CE: Current External. Includes accurate CC/CV regulation with external output current sense for optimum design flexibility. Targets compact single-voltage chargers, adapters, IoT and building automation.
- CP: Constant Power. Ideal for USB Power Delivery (PD), rapid charging and other applications where a dynamic output voltage is required.
- EP: Embedded Power. Features the family's highest-rated MOSFET (725 V) and provides full line and load protection with excellent multi-output cross-regulation for demanding industrial applications and appliances.

These flyback switcher ICs employ isolated digital communications technology, called FluxLink™, plus synchronous rectification, quasi-resonant switching and a precise secondary-side feedback sensing and control circuit. This results in highly efficient, accurate, reliable power supply circuits without the need for optocouplers. InnoSwitch3 devices are CCC, UL and VDE safety-certified to bridge the isolation barrier, and the InSOP™-24 package provides a low-profile, thermally efficient solution with extended 11.5 mm creepage and clearance between primary and secondary sides for high reliability, surge and ESD robustness. The new devices also incorporate protection features as well as output rectifier short-circuit protection and feature on-chip high-voltage MOSFETs.

Samples are available now, priced at $1.11 (CE) and $1.15 (CP), in 10,000-piece quantities. InnoSwitch3-EP parts will be available in November 2017 at $1.18 per 10,000-pieces.

## Innovative architecture

The InnoSwitch3-EP combines a 1 Ω high-voltage power MOSFET switch (rated at 650 V for the CP and CE series and 725 V for the EP series), along with both primary-side and secondary-side controllers in one device. Typical switching frequency is in the range of 100 MHz.

The architecture incorporates the novel inductive coupling feedback scheme (FluxLink) using the package lead frame and bond wires to provide a safe, reliable, and cost-effective means to transmit accurate, output voltage and current information from the secondary controller to the primary controller.

The primary controller is a Quasi-Resonant (QR) flyback controller that can operate in continuous conduction mode (CCM), boundary mode (CrM) and discontinuous conduction mode (DCM). The controller uses both variable frequency and variable current control schemes. The primary controller consists of a frequency jitter oscillator, a receiver circuit magnetically coupled to the secondary controller, a current limit controller, 5 V regulator on the PRIMARY BYPASS pin, audible noise reduction engine for light load operation, bypass over-voltage detection circuit, a lossless input line sensing circuit, current limit selection circuitry, over-temperature protection, leading edge blanking, secondary output

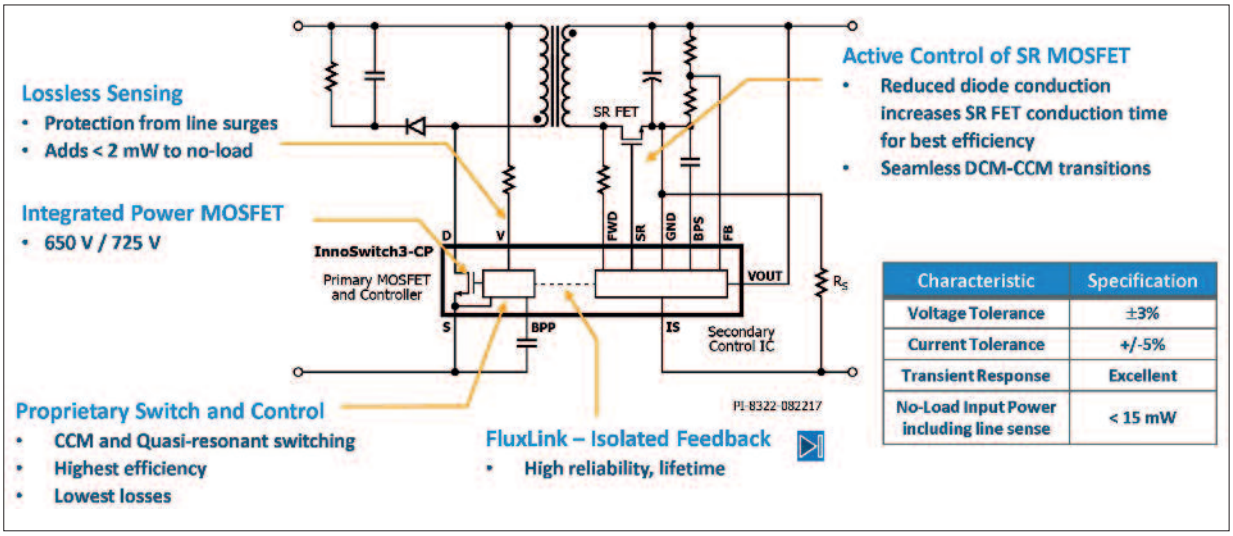


Figure 1: **Innoswitch3 properties – eliminating optocouplers via FluxLink digital feedback**

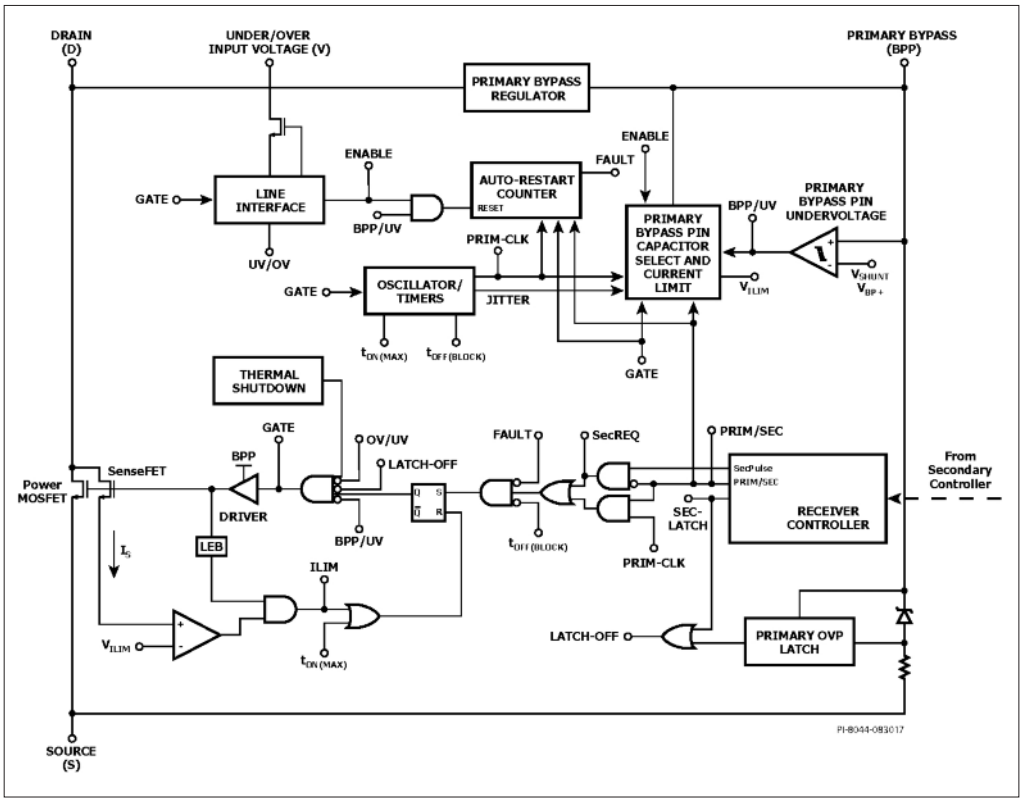


**Figure 2: Primary controller block diagram**

diode / SR FET short protection circuit and a 650 V / 725 V power MOSFET.

The secondary controller consists of a transmitter circuit that is magnetically coupled to the primary receiver, a constant voltage (CV) and a constant current (CC) control circuit, a 4.4 V regulator on the SECONDARY BYPASS pin, synchronous rectifier FET driver, QR mode circuit, oscillator and timing circuit, and numerous integrated protection features. Figures 1 and 2 show the functional block diagrams of the primary and secondary controller, highlighting the most important features.

## Primary controller

The variable frequency QR controller plus CCM/CrM/DCM operation is intended for enhanced efficiency and extended output power capability.

The PRIMARY BYPASS pin has an internal regulator that charges the pin capacitor to $V_{BPP}$ by drawing current from the DRAIN pin whenever the power MOSFET is off. The PRIMARY BYPASS pin is the internal supply voltage node. When the power MOSFET is on, the device operates from the energy stored in the PRIMARY BYPASS pin capacitor. In addition, a shunt regulator clamps the PRIMARY BYPASS pin voltage to V when current is provided to the PRIMARY BYPASS SHUNTpin through an external resistor. This allows the InnoSwitch3-(EP) to be powered externally through a bias winding, decreasing the no-load consumption to less than 15 mW in a 5 V output design.

The user can adjust current limit ($I_{LIM}$) settings through the selection of the PRIMARY BYPASS pin capacitor value. A ceramic capacitor can be used, sizes of 0.47 µF and 4.7 µF for setting standard and increased ILIM settings respectively are selectable.

The PRIMARY BYPASS pin under-voltage circuitry disables the power MOSFET when the respective pin voltage drops below ~4.5 V ($V_{BPP}$ - $V_{BP(H)}$) in steady-state operation. Once the PRIMARY BYPASS pin voltage falls below this threshold, it must rise to $V_{SHUNT}$ to re-enable turn-on of the power MOSFET. This pin has also a latching OV protection feature. A Zener diode in parallel with the resistor in series with the PRIMARY BYPASS pin capacitor is typically used to detect an over-voltage on the primary bias winding and activate the protection mechanism. In the event that the current into the pin exceeds $I_{SD}$, the device will latch-off or disable the power MOSFET switching for a time $t_{AR(OFF)}$, after which time the controller will restart and attempt to return to regulation. $V_{OUT}$ OV protection is also included as an integrated feature on the secondary controller.

The thermal shutdown circuitry senses the primary MOSFET die temperature. The threshold is set to $T_{SD}$ with either a hysteretic or latch-off response. If the die temperature rises above the threshold, the power MOSFET is disabled and remains disabled until the die temperature falls by $T_{SD(H)}$ at which point switching is re-enabled. A large amount of hysteresis is provided to prevent over-heating of the PCB due to a continuous fault condition. Latch-off response: If the power MOSFET is disabled, latching is reset by bringing the PRIMARY BYPASS pin below $V_{BPP(RESET)}$ or by going below the $U_V$ ($I_{UV-}$) threshold.

The current limit threshold ramp is inversely proportional to the time from the end of the previous primary switching cycle (i.e. from the time the primary MOSFET turns off at the end of a switching cycle). This characteristic produces a primary current limit that increases as the switching frequency (load) increases (Figure 4). This enables the most efficient use of the primary switch with the benefit that this algorithm responds to digital feedback information immediately when a feedback switching cycle request is received.

At high load, switching cycles have a maximum current approaching 100 % $I_{LIM}$. This gradually reduces to 30 % of the full current limit as load decreases. Once 30 % current limit is reached, there is no further reduction in current limit (since this is low enough to avoid audible noise). The time between switching cycles will continue to increase as load reduces.

The normalized current limit is modulated between 100 % and 95 % a modulation frequency of fM this results in a frequency jitter of ~7 kHz with average frequency of ~100 kHz.

In the event a fault condition occurs (such as an output overload, output short-circuit, or external component/pin fault), the IC enters auto-restart (AR) or latches off. The latching condition is reset by bringing the PRIMARY BYPASS pin below ~ 3 V or by going below the UNDER/OVER

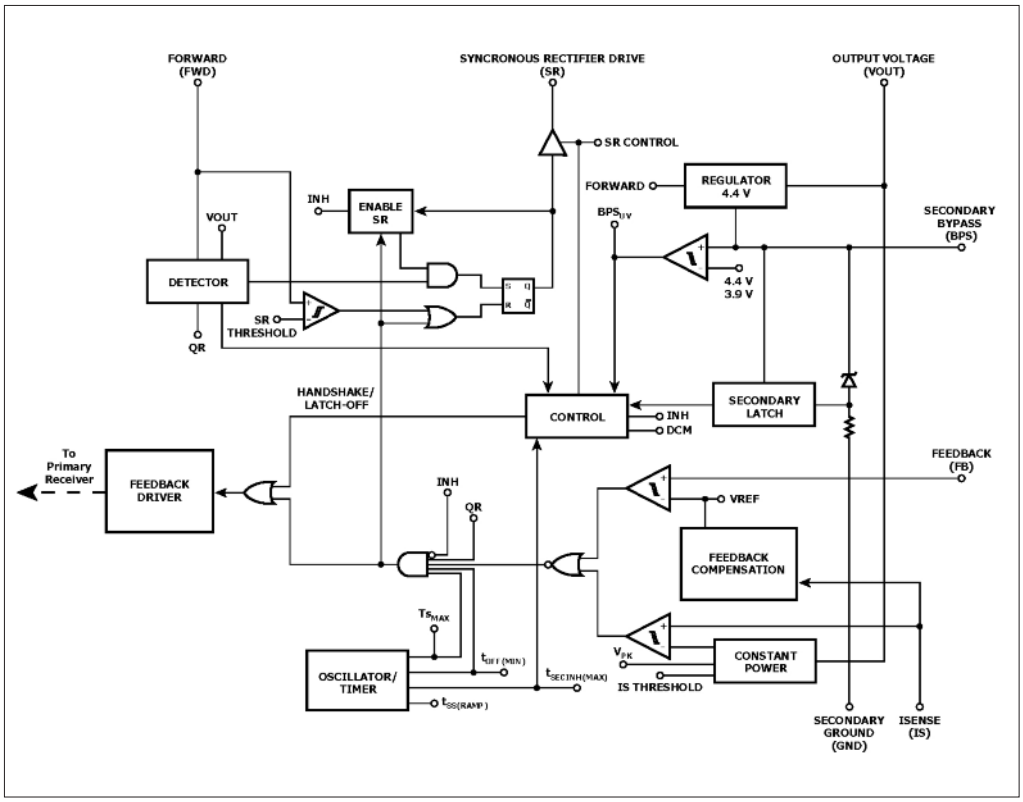


**Figure 3:** Secondary controller block diagram

INPUT VOLTAGE pin $U_V$ ($I_{UV}$) threshold.

In the event that there are two consecutive cycles where the $I_{LIM}$ is reached within ~500 ns (the blanking time + current limit delay time), the controller will skip 2.5 cycles or ~25 µs (based on full frequency of 100 kHz). This provides sufficient time (SOA protection) for the transformer to reset with large capacitive loads without extending the start-up time.

## Secondary controller

As shown in Figure 3, the IC is powered by a 4.4 V ($V_{BPS}$) regulator which is supplied by either $V_{OUT}$ or FWD. The SECONDARY BYPASS pin is connected to an external decoupling capacitor and fed internally from the regulator block.

The FORWARD pin also connects to the negative edge detection block used for both handshaking and timing to turn on the SR FET connected to the SYNCHRONOUS RECTIFIER DRIVE pin. The FORWARD pin voltage is used to determine when to turn off the SR FET in discontinuous mode operation. This is when the voltage across the $R_{DS(ON)}$ of the SR FET drops below zero volts.

In continuous conduction mode (CCM) the SR FET is turned off when the feedback pulse is sent to the primary to demand the next switching cycle, providing excellent synchronous operation, free of any overlap for the FET turn-off. The mid-point of an external resistor divider network between the OUTPUT VOLTAGE and SECONDARY GROUND pins is tied to the FEEDBACK pin to regulate the output voltage. The internal voltage comparator reference voltage is $V_{FB}$ (1.265 V). The external current sense resistor connected between $I_{SENSE}$ and SECONDARY GROUND pins is used to regulate the output current in constant current regulation mode.

## Innoswitch3-EP application example

Innoswitch3 ICs target adapters and open-frame power supplies for consumer, computer, communication and industrial applications. The circuit shown in Figure 5 is a low cost 5 V, 0.3 A and 12 V, 0.7 A dual output power supply which features high efficient design satisfying cross regulation requirement without post regulator.

Bridge rectifier BR1 rectifies the AC input supply. Capacitors C2 and C3 provide filtering of the rectified AC input and together with inductor L1 form a pi-filter to attenuate differential mode EMI. Y capacitor C10 connected at the power supply output with input help reduce common mode EMI. 0Thermistor RT1 limits the inrush current when the power supply is connected to the input AC supply. Input fuse F1 provides protection against excess input current resulting from

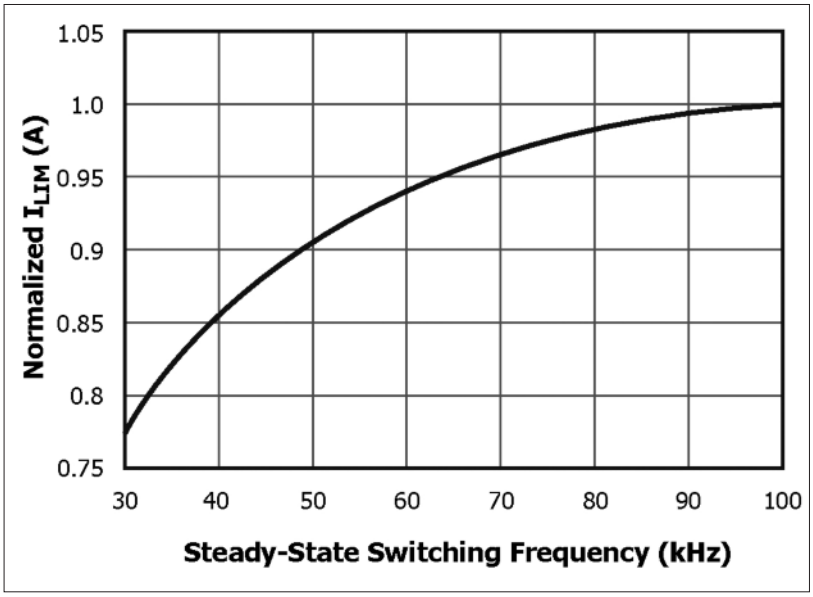


**Figure 4:** Normalized primary current vs. frequency