Versatile Gate Driver IC Featuring Unique Isolation Technique

The newest member of the SCALE-iDriver™ IC family, SID1102K is a single-channel, isolated, IGBT and MOSFET gate driver in a wide-body eSOP package. Featuring a peak drive current of up to 5 A, the new part is able to drive 300 A switches without boosters; external boosters can be used to cost-effectively scale gate current up to 60 A peak. Reinforced galvanic isolation is provided by Power Integrations' innovative, solid insulator FluxLink™ technology which eliminates the need for optocouplers. "This new gate-driver IC reduces time-to-market for designers by providing an easy-to-implement, scalable solution which includes critical safety and protection features in a single, compact, robust package", comments **Michael Hornkamp, Senior Director of Marketing for Gate-Driver Products at Power Integrations in Ense, Germany.**

The single channel SCALE-iDriver

SID1102K drives IGBTs and MOSFETs or other semiconductor power switches with a blocking voltage of up to 1200 V and provides reinforced isolation between micro-controller and the power semiconductor switch. Command signals are transferred from the primary (IN) to secondary-side via FluxLink isolation technology. The G pin supplies a positive gate voltage and charges the semiconductor gate during the turn-on process. During the turn-off process the G pin supplies the negative voltage and discharges the gate. Additionally, dedicated AUXGL and AUXGH output pins are available to drive external n-channel MOSFETs as booster stage that can be configured to provide increased peak output gate drive current. Therefore additionally AUXGL and AUXGH output pins can drive external n-channel MOSFETs as a booster stage. Controller (PWM) signals are compatible with 5 V CMOS logic, which may also be adjusted to 15 V levels by using external resistor divider.

FluxLink technology

The FluxLink technology is a high speed bi-directional communications link that sits across the isolation gap. It is a solution for the secondary side isolation and coupling replacing an optocoupler which degrades over time, but more importantly also to save cost. The idea is using the "parasitic" inductance of the bond wires (which can

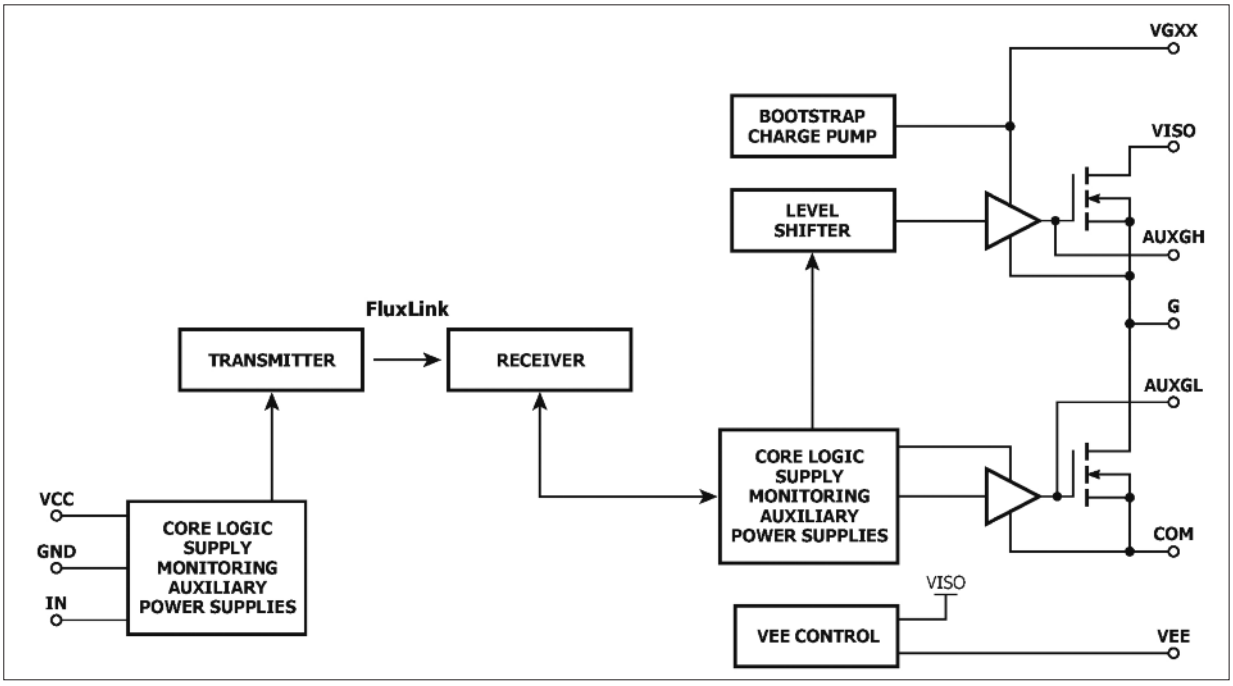

Figure 1: SID1102K functional block diagram

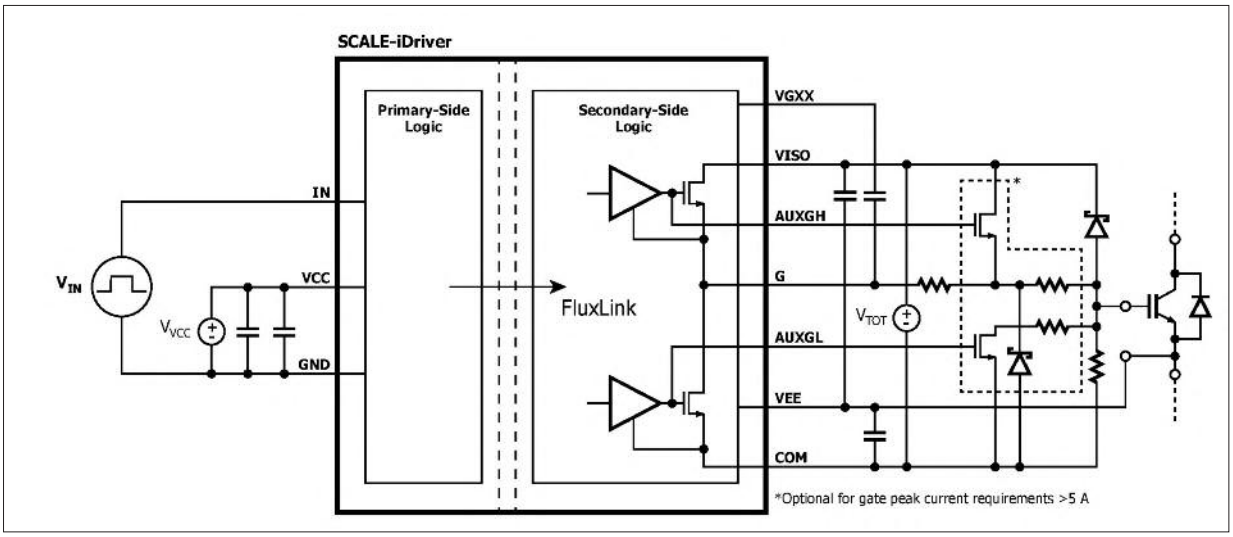

Figure 2: Typical application schematic highlighting FluxLink and with external N-channel MOSFET booster stage

be manufactured repeatable) and leadframe as a coreless pulse transformer, in particular optimizing its physical layout.

Using a robust signalling protocol, it provides very high EMI and magnetic field immunity and exceeds the standards IEC61800-4-8 and IEC61800-4-9 in all three axes. It features a very low propagation delay and a very low jitter of only +/-5ns. This link not only isolates the low voltage input control side of the device but also communicates back any fault conditions measured on the high voltage side of the device back across the barrier to a microcontroller responsible for control and monitoring the device operation.

Driver details

The SID1102K requires two power supplies. One for the primary-side (V_{VCC}), which powers the primary-side logic and communication with the secondary (insulated) side. The other supply voltage (V_{TOT}) is required for the secondary-side. V_{TOT} is applied between VISO pin and COM pin. V_{TOT} should be insulated from the primary-side and should provide at least the same insulation capabilities as the SCALE-iDriver. V_{TOT} should have a low capacitive coupling to the primary or any other secondary-side. The positive gate-emitter source voltage is provided by V_{VISO}, which is internally generated and stabilized to 15 V (typically) with respect to VEE. The negative gate-emitter source voltage is provided by VEE with respect to COM. Due to the limited current sourcing/sinking capabilities of the VEE pin, any additional load needs to be applied between the VISO and COM pins. No additional load between VISO and VEE pins or between VEE and COM pins is allowed.

The input (IN) logic is designed to work directly with micro-controllers using 5 V CMOS logic.

If the physical distance between the controller and the iDriver is large or if a different logic level is required, the resistive divider in Figure 3 is recommended. This solution adjusts the logic level as necessary and will also improve the driver's noise immunity.

Gate driver commands are transferred from the IN pin to the G pin with a propagation delay tP(LH) and tP(HL).

The gate of the power semiconductor switch should be connected to the iDriver output via pin G, using a suitable gate resistor RG as shown in Figure 4.

Note that most power semiconductor data sheets specify an internal gate resistor R_{GINT}, which is already integrated into power semiconductor switches. In addition to R_{GINT}, external resistor device R_G is specified to set-up the gate current level to the application requirements. Careful consideration should be given to the power dissipation and peak current associated with the external gate resistor.

The G pin output current source ($I_{G(H)}$, $I_{G(L)}$) is capable of sinking and sourcing

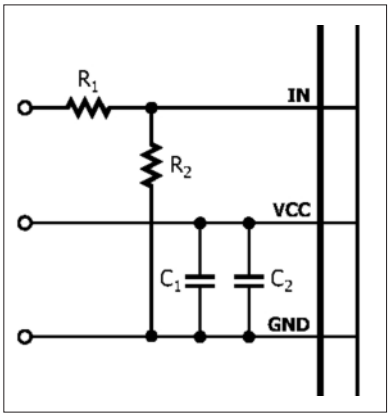

Figure 3: Recommended circuitry for increased IN logic levels (for R1 = 3.3 kΩ and R2 = 1 kΩ the IN Logic Level is 15 V)

(typically) 5 A at 25°C. The internal resistances are described as R_{GHI} and R_{GLI} respectively. If the gate resistor attempts to draw a higher peak current, the peak current will be internally limited to a safe value.

It is recommended during power-up and power-down that the IN pin stays at logic low. Any supply voltage related to VCC, VISO, VEE and VGXX pins should be stabilized using ceramic capacitors. After supply voltages reach their nominal values, the driver will begin to function after a time delay tSTART.

If command signals applied to the IN pin are shorter than the minimum specified by $t_{GE(MIN)}$, then SID1102K output signals at G, AUXGH, and AUXGL pins will extend to value $t_{GE(MIN)}$. The duration of pulses longer than $t_{GE(MIN)}$ will not be changed.

Application example and components selection without booster

Figure 4 show the schematic and typical components used for a SID1102K design without a booster stage, in which the primary-side supply voltage (V_{VCC}) will be connected between VCC and GND pins and supported through supply bypass ceramic capacitors C1 (4.7 ?F typically) and C2 (470 nF typically). If the command signal voltage level is higher than the rated IN pin voltage, a resistive voltage divider should be used (Figure 3).

Additional capacitor CF can be used to provide input signal filtering as shown in Figure 4. The filter time τ can be calculated according to equation (1):

$$\tau = \frac{R_1 \times R_2}{R_1 + R_2} \times C_F$$

The secondary-side isolated power supply

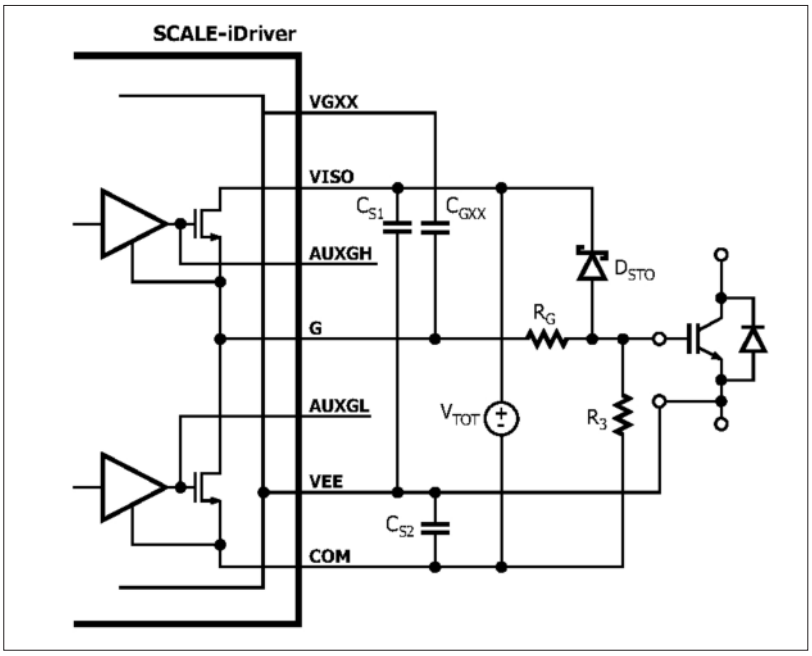

Figure 4: SID1102K without external booster stage incorporating gate resistor RG

(V_{TOT}) is connected between VISO and COM. The positive voltage rail (V_{VISO}) is supported through ceramic capacitor C_{S1}. The negative voltage rail (VVEE) is similarly supported through capacitor C_{S2}. Typically, C_{S1} and C_{S2} should be at least 3 µF multiplied by the total gate charge of the power semiconductor switch (Q_{GATE}) divided by 1 µC. A 10 nF capacitor C_{GXX} is connected between the G and VGXX pins.

To ensure gate voltage stabilization and collector current limitation during short-circuit the gate is connected to V_{VISO} through Schottky diode D_{STO}.

To avoid parasitic power-switch-conduction during system power-on the gate is connected to COM through 22 kΩ resistor R 3, as shown in Figure 4.

Gate resistors are located physically close to the power semiconductor switch. As these components can get hot, it is recommended that they are placed away from the SCALE-iDriver.

Literature

Hornkamp, Michael; 1200 V Gate Driver ICs Featuring FluxLink, Power Electronics Europe 3/2016

Clever Ideas Succeed in the Market, Power Electronics Europe 2/2016, Market News