# Leveraging Automotive-Quality 150 mm Si-CMOS Processes Makes SiC MOSFETs More Affordable and Reliable

Silicon IGBTs are suitable for voltage ranges in which a 1200 V-rated part is necessary, but they are limited to ~25 kHz in hard-switched applications. Si MOSFETs allow for operating frequencies well above 25 kHz, but design trade-offs start to limit their advantages at voltages higher than 600 V. In contrast, SiC MOSFETs switch up to five to ten times faster than Si IGBTs and can operate at higher junction temperatures, but at equivalent higher device cost. One way of getting improved SiC MOSFET costs requires a non-traditional wafer processing methodology - processing SiC wafers in parallel with Si wafers in a high-volume Si-CMOS foundry. **Dr. Sujit Banerjee, CEO Monolith Semiconductor and Corey Deyalsingh, Director of Power Semiconductor at Littelfuse, USA**

**Silicon-based MOSFETs and IGBTs** are the traditional options for semiconductor switches in power converter applications. However, these devices too often limit the performance capabilities of their intended applications. Silicon (Si) IGBTs are suitable for voltage ranges in which a 1200 V-rated part is necessary, but they are limited to a maximum operating frequency of ~25 kHz in hard-switched applications. Si MOSFETs allow for operating frequencies well above 25 kHz, but design trade-offs start to limit their advantages at voltages higher than 600 V.

In contrast, the newest Silicon Carbide (SiC) MOSFET switches offer designers of power conversion systems for applications such as photovoltaic inverters, energy storage systems, EV chargers, UPSs, industrial motor drives, and a rapidly growing array of other products significant performance advantages over traditional Si MOSFET and IGBT switches. SiC MOSFETs switch up to five to ten times faster than Si IGBTs and can operate at higher junction temperatures. Because they can switch on and off so quickly, they enable higher switching frequencies and therefore allow those designing inverters and other power converters to shrink the size and weight of other components in the system, which significantly improves power density and weight without penalizing system efficiency.

In spite of a price premium over Si MOSFETs and IGBTs, the SiC MOSFET is already seeing significant success due to cost-offsetting system-level benefits; the market share for this technology seems destined to expand rapidly over the next few years as the supply chain matures. One way of getting improved SiC MOSFET costs requires a non-traditional wafer processing methodology: processing SiC wafers in parallel with Si wafers in a high-volume Si-CMOS foundry. Littelfuse and Monolith Semiconductor have pursued this tactic as part of a strategic partnership begun in 2015, and are producing SiC Schottky diodes and MOSFETs in a 150 mm CMOS facility in Texas owned by X-FAB that also fabricates automotive-qualified Si devices. This fabless approach allows us to support power converter makers who require customized devices—customers that the major SiC suppliers aren't interested in working with.

## Fabless wafer production

This wafer production method offers a variety of advantages. For example, processing wafers in this CMOS facility allows sharing best manufacturing and quality practices used for automotive-qualified CMOS products and takes advantage of enormous economies of scale. Avoiding the high costs of operating our own fab allows for major cost reductions. In addition, fabricating SiC devices on 150 mm wafers rather than on 100 mm wafers (as is typical for SiC devices) allows for much more efficient leveraging of manufacturing costs. Even though processing larger wafers costs more than smaller ones, it also allows spreading the higher cost per wafer over a larger yield of die per wafer.

From a materials and equipment standpoint, SiC wafer processing is fundamentally compatible with CMOS processing. At the X-Fab facility, standard CMOS process steps are reused wherever possible, including implant masking steps and top-level interconnects. However, several challenges remain, including the requirement for high-temperature processing and the need to integrate CMOS and SiC-specific processing steps; for example, all metal and dielectric stacks must be compatible with a standard CMOS fab. SiC-specific processes were developed using CMOS production tools for certain steps like contacts, gate oxidation among others. The only steps for which special SiC-specific tools are used are implant activation and certain ion implantation steps. The semi-transparent nature of SiC wafers and the difference in wafer thickness vs. the facility's usual Silicon wafers required modifying or optimizing the mechanical wafer handling procedures for several process steps.

## Validating defect density and yield

Despite these challenges, Littelfuse and Monolith are confident of the quality of the SiC wafers we're producing because of

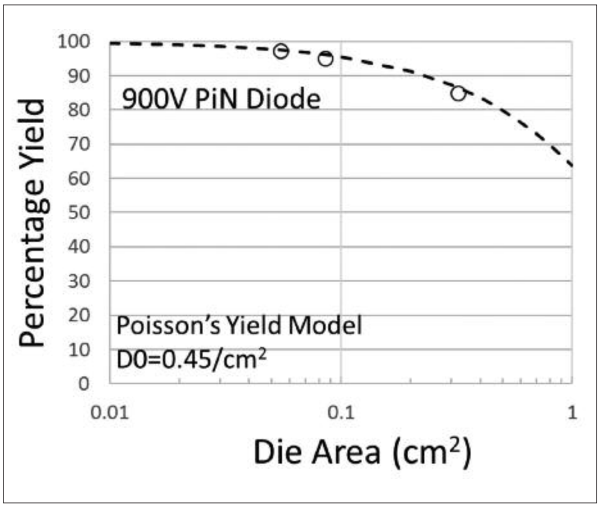



**Figure 1: Percentage yield vs. die area for 900 V PiN diodes (yield is modeled using Poisson's model, assuming defect density of 0.45/cm?)**

specific testing we've conducted to validate defect density and yield. For example, we designed and fabricated a test chip containing SiC Schottky and large-area PiN diodes with die sizes ranging from 0.054 $cm^2$ to 0.45 $cm^2$ on our epitaxial wafers. Wafer level characterization of both the 900 V SiC Schottky diodes and the 900 V PiN diodes was performed on 100 % of the die on all wafers. The yields for the devices of three different die sizes were calculated based on the yields of key electrical parameters: forward voltage ($V_F$) drop, reverse leakage current at full rated voltage ($I_R$), and breakdown voltage ($V_{BR}$).

The percentage yield of the PiN diodes of three different die sizes – 0.32, 0.08, and 0.05 $cm^2$ is plotted in Figure 1 using the Poisson's Yield model and a good fit is obtained for a defect density assumption of 0.45 defects/$cm^2$. The decrease in yield for the larger area PiN diodes is primarily due to the impact of starting material defects and process induced defects on $I_R$ or $V_{BR}$. The Schottky diode yield followed a similar trend, with a slightly larger impact of defects on the yield, particularly for the larger area diodes. This defect level gives approximately a 30 % reduction in yield for an 8x increase in die size.

The high quality of our starting material (epitaxial SiC wafers) and CMOS processing is also reflected in the quality of the 1.2 kV MOSFETs fabricated in the fab. This was demonstrated through long-term reliability testing, in which the devices exhibited no signs of degradation over the entire 1000-hour testing cycle, as shown in Figures 2 and 3.

To illustrate the system-level advantages that power converter designers can achieve using SiC devices rather than Si devices, we have designed and built a 5 kW buck converter, which converts a higher voltage input to a lower voltage output. The operation of the converter with a silicon IGBT and a Littelfuse/Monolith SiC MOSFET was compared head to head. The results, plotted in Figures 4 and 5, illustrate that at 25 kHz, the Si IGBTs were rapidly approaching thermal runaway at the 5 kW power level. Thus, it's safe to assume the Si IGBT could not satisfy any higher power or a higher switching frequency at the 5 kW power level. Additionally, these figures demonstrate superior SiC MOSFET performance in terms of efficiency; even at 25 kHz, which is in the realm of switching frequencies commonly satisfied by Si IGBTs.

These efficiency and temperature characteristic plots demonstrate that SiC MOSFETs are not only capable of offering

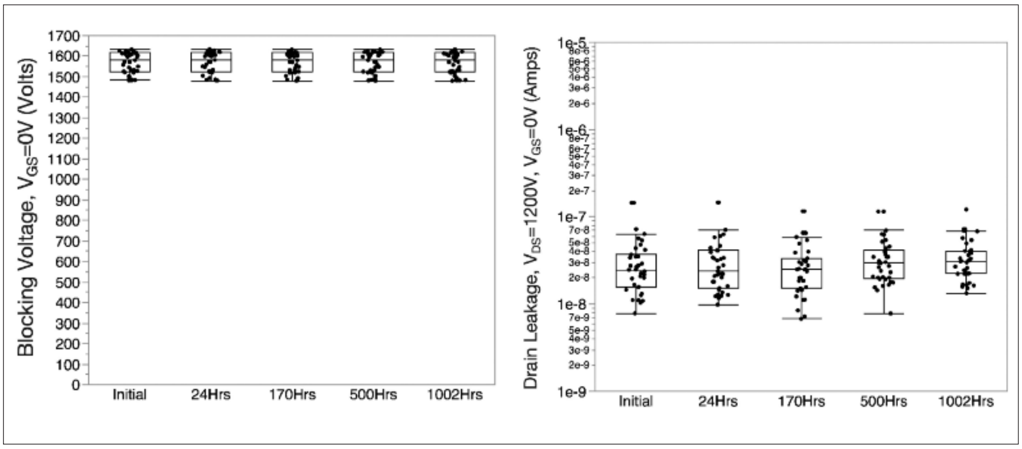



**Figure 2: Results of high temperature reverse bias testing at 175°C (breakdown voltage at $V_{GS}$ = 0 V, leakage current at $V_{DS}$ = 960 V)**

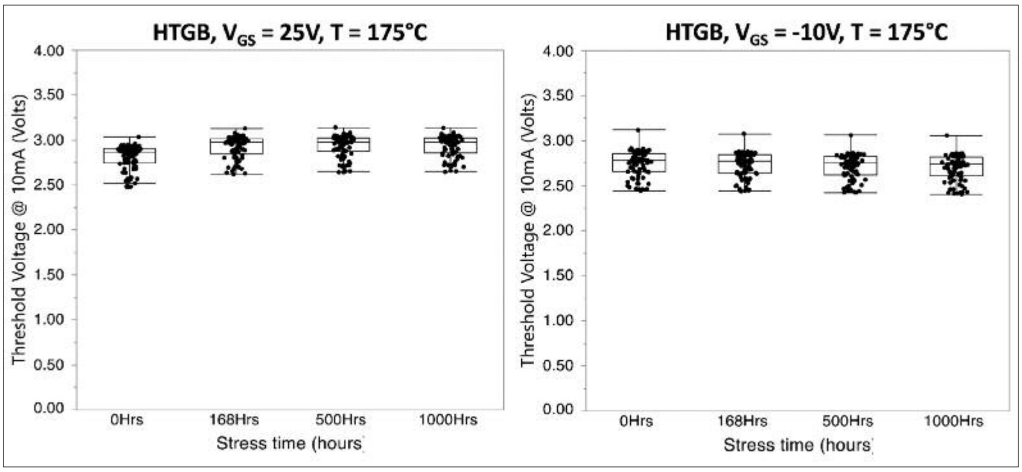



**Figure 3: Results of high temperature gate bias (HTGB) testing at 175°C ($V_{GS}$ = -10V and at $V_{GS}$ = +25 V)**

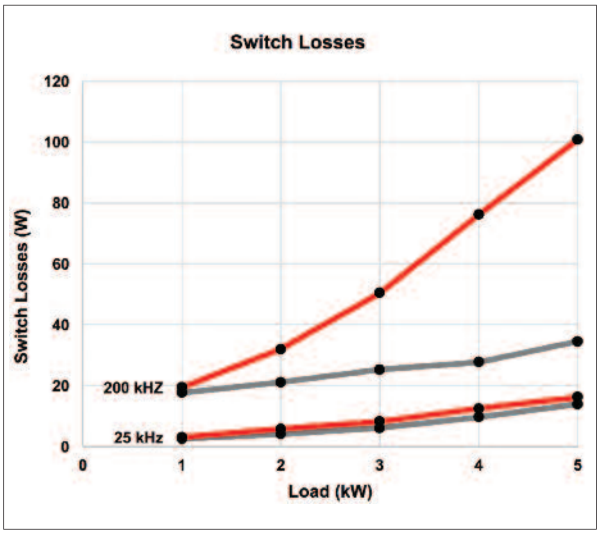



Figure 4: **Efficiency vs. load for 25 kHz operating point**

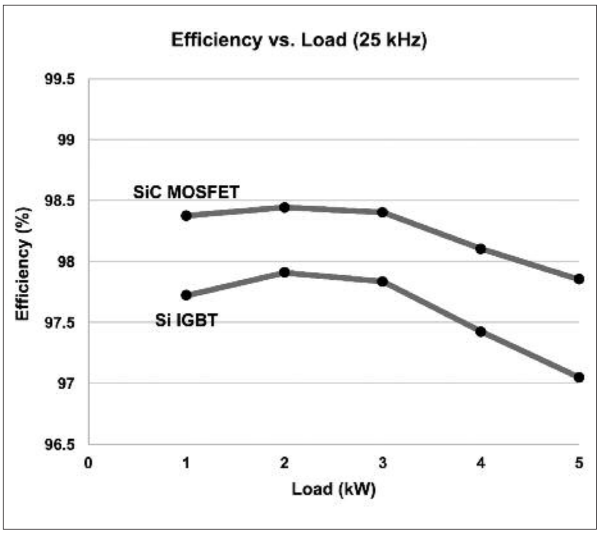
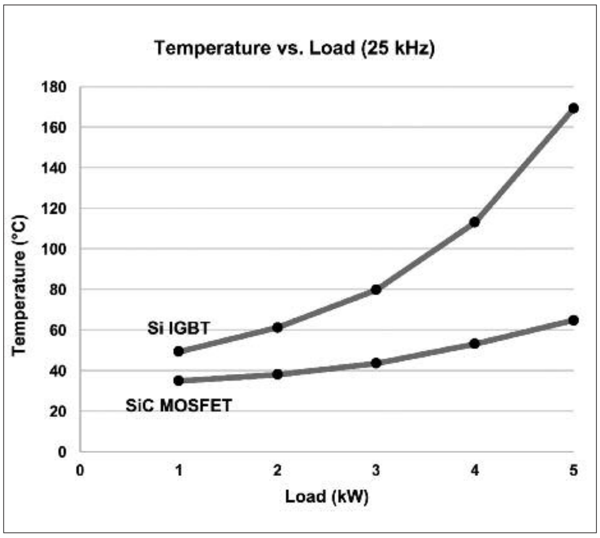



Figure 5: **Temperature vs. load for 25 kHz operating point**




LEFT Figure 6: **Switch losses vs. load of simulated converter, showing Si IGBT in red and SiC MOSFET in gray (Note - bench top testing of Si IGBT based converter at 200 kHz is not possible)**

improved power density by opening the gateway to higher switching frequencies, but they can also compete with Si IGBTs at lower switching frequencies due to their relatively low on-state resistance. Unlike the IGBT-based converter, the SiC-based converter could also comfortably operate at 200 kHz with >98 % efficiency (Figure 6).

The future of power semiconductors will depend on device producers willing to embrace the core principles of providing their customers with devices designed to enhance speed, agility, and flexibility. For SiC MOSFETs to achieve their full potential in power conversion applications, their producers must be willing to work with designers to encourage exploration of the technology's potential. Thus Littelfuse and Monolith Semiconductor have developed a Dynamic Characterization Platform (DCP) to help designers streamline the incorporation of SiC power devices into their systems.

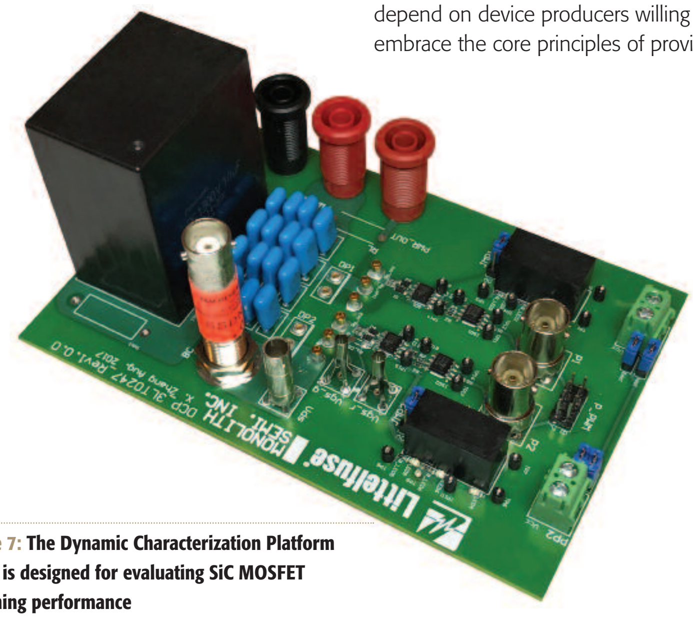


Figure 7: **The Dynamic Characterization Platform (DCP) is designed for evaluating SiC MOSFET switching performance**

## New tools empower power converter designers

The process of designing a SiC-based power converter can be very different than designing with Si power devices. The Dynamic Characterization Platform (DCP) shown in Figure 7 supports evaluating a SiC MOSFET's switching performance with extreme accuracy on a per-cycle basis using a double-pulse, clamped inductive load (CIL) test. The DCP lets designers extract a full suite of switching characteristics associated with a device, including gate charge, switching times, and switching energies. Switching test waveforms provide insight into device behavior and how designers can implement them into their configurations to optimize performance.

## Tomorrow's power semiconductors

Littelfuse has recently introduced 1200 V SiC Schottky diodes and 1200 V, 80 mΩ MOSFETs to the market. In 2018 and beyond, these devices will be scaled to higher current levels, various voltage ratings: 650 V, 900 V and 1700 V, and several discrete package options. We also intend to develop power modules with low parasitic inductance that can take advantage of the faster switching speeds that SiC devices support.