DC Bus Switching Performance as Determined by Commutation Loop Parasitics and Switching Dynamics

In this article a 250 kW all-SiC inverter evaluation kit designed around low-inductance, high-speed power modules is used to demonstrate the DC bus switching performance resulting from the interaction among commutation loop parasitics and the switching dynamics. The interplay among the DC bus structure parasitics and near-RF switching dynamics can be quantified in both the time and frequency domains. The gate driver external turn-on and turn-off gate resistor selections in the gate-source signal path directly impact the system response – and whether it is critically damped or underdamped. The parasitic ESR and ESL of the DC bus film capacitors, laminated bussing, high-frequency (HF) ceramic decoupling capacitors, and power module-DC bussing interconnects contribute to bus switching degradation due to fast SiC MOSFET switching dynamics. The key takeaway is to optimize the DC bus structure rather than trying to compensate for a poor design. **Ty McNutt, Kraig Olejniczak, Daniel Martin and Guy Moxey; Wolfspeed, a Cree Company, USA**

SiC power module designers must pay special attention to module and system parasitic inductance, as these parameters determine the power module current and voltage utilization with respect to the module rating. The gate drivers, capable of switching at hundreds of kHz, must provide high noise immunity to large dv/dt, di/dt, and common-mode disturbances. Even though fast switching devices promise lower switching losses, EMI-related issues become more pronounced and can impact system behavior.

All-SiC power modules - working from the inside out

The high-performance power module of Figure 1 forms the coupling mechanism from the SiC die to the rest of the system beyond the modules' power terminals. An optimal system design begins by working from the inside out; it starts by using: high performance, low on-resistance/high current SiC power devices; a low ESL internal gate-source board to equalize paralleled die performance (up to 13 die); low impedance lead frames (i.e., < 0.1 mΩ parasitic module resistance and 5.5 nH of parasitic inductance); and, high-temperature module material capability in excess of 225°C. To fully capture the benefits of SiC power devices, one cannot be on a "mental holiday" when designing the external bussing; to do so may nullify the power module designer's design intent and optimization efforts within the all-SiC power module.

Gate driver design

Due to extremely high di/dt and dv/dt switching, it is critical that the gate driver have a minimal gate-loop stray inductance to reduce the gate oscillations that are so sensitive to SiC devices. How? Minimize the gate driver-module electrical interconnect length by placing the gate driver PCB on top of the module (i.e., within a few cm). The internal gate-source PCB design and internal gate resistor value selection are critical for achieving optimum module EMI and switching loss reductions.

The driver's external gate resistors control the speed at which the gate

Figure 1: The CAS325M12HM2 All-SiC power module with a 5.5 nH power-loop inductance uses a high-speed internal signal distribution board for equalized die performance

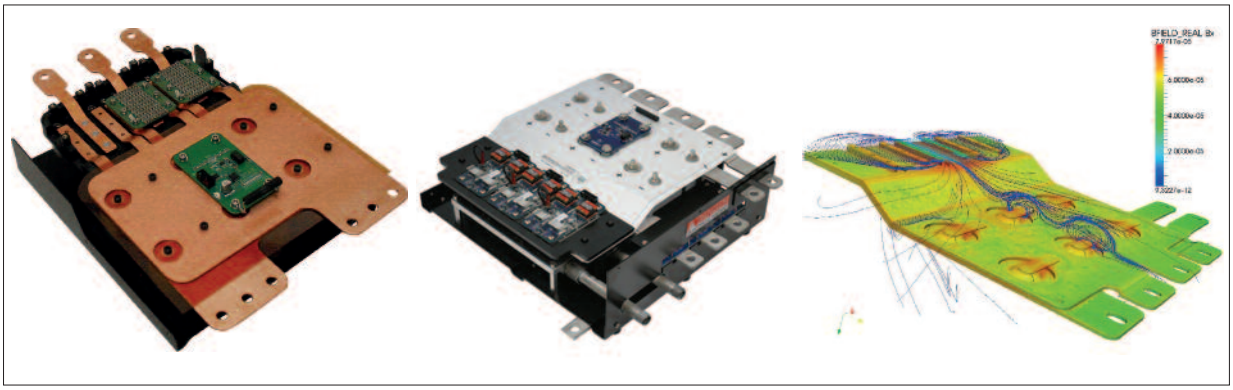

Figure 2: An initial bussing design V1 (left), and optimized design V2 (middle), for a 3-phase inverter using the Wolfspeed CAS325M12HM2 power module. The magnetic flux Bx for the low-inductance (~ 3.5 nH) V2 bussing is shown (right)

capacitance is charged and discharged and therefore determines the system switching losses. The lower the gate resistor value, the faster the switching time, and greater the overshoot. Minimizing the isolation capacitance of the gate driver is critical to improving the system noise immunity from switching the SiC power module. Wolfspeed's gate driver has an isolation capacitance of ~17 pF per channel. Utilizing differential signaling for control and feedback signals further improves system-level noise immunity by rejecting common-mode noise enacted upon the cabling or input pins of the gate driver.

DC bus structure

The commutation loop, which includes the laminated DC bussing and the DC-link capacitor bank, must have a minimal ESL as viewed from the modules' power terminals. The maximum continuous DC bus voltage is constrained by the voltage overshoot resulting from the energy stored in the parasitic inductances seen by the power module's drain and source power terminals. This parasitic inductance, L_σ, combined with higher di/dt, negatively impacts the power module voltage and current utilization. The first is the voltage overshoot, $\Delta V_{overshoot} = - L_\sigma$ di/dt, which adds to the DC bus voltage during turn-off. This constrains V_{bus} to an artificially low value since the peak value of $V_{bus} + v_{ripple} + \Delta V_{Overshadow}$ + the safety margin must be less than the module DC rating.

Here, v_{ripple} is the peak voltage ripple resulting from the AC current interacting with the capacitor bank's ESR. Note the three ways to minimize the voltage overshoot: minimize L_σ, decrease the load current, di, and/or increase the switching time dt. Decreasing the load current results in less power delivered to the load. Slowing down the device during turn-off will result in additional switching losses penalizing the device thermally and affecting the overall system efficiency. Limiting di/dt, by reducing the current or slowing down the power device during turn-off, will result in a reduction in power module current utilization. Thus, minimizing the parasitic inductance is paramount.

DC-link film capacitor selection

The one component which imposes a significant constraint to the overall system performance is the DC-link capacitor. In general, capacitors used in power electronics applications are usually either electrolytic, metallized polypropylene (MPP), or ceramic. The optimum DC-link capacitor selection is important due to the tension that exists among the following three concerns: cost, electro-thermal-mechanical performance at the system maximum ambient temperature, and capacitor reliability based on its maximum hot-spot temperature. The power electronics designer seeks to maximize voltage blocking capability as a function of temperature; capacitance stability as a function of temperature and voltage; RMS ripple current capability; insulation resistance; and reliability and life expectancy. Similarly, the power electronics designer seeks to concurrently minimize footprint, volume, weight, ESR, ESL, and thermal resistance from hot-spot to case.

DC laminated bus

The DC bussing is a multi-physical design problem in the electrical, thermal, and mechanical domains. Electrically, the DC bus needs to be a low ESR (i.e., high conductivity material, "large" cross-sectional conduction area) and ESL (i.e., thin and wide "planes") structure. The main DC bussing design parameters affecting ESR and ESL include: copper thickness (t), width (w), length (l), of the V+ and V- planes and separation distance (d), between the V+ and V- planes. Thermally, a low temperature rise (e.g., < 80 K from room temperature) due to the maximum expected RMS current passing through the structure is required. Mechanically, a high level of robustness against normal shock and vibration during use is required.

The DC bussing that connects the DC-link capacitors to the SiC power module is shown in Figure 2 for two designs: Version 1 (V1), an early stage prototype with inexpensive laminated copper bussing to begin evaluating the module performance, and Version 2 (V2), a design iteration based on theoretical analysis of module/bussing/capacitor interactions. Note, the V1 bussing design does not carry the laminated structure to the module; but instead, shifts to thin "fingers" connecting to the module lead frames thus creating high inductance paths that must be compensated with HF capacitors (see 2 of 3 snubber PCBs installed in Figure 2, left). These HF capacitors, or snubber capacitors, are used to alter the frequency response of the DC bussing, and can result in a reduced turn-off voltage magnitude when placed across the DC bussing as close as physically possible to the module DC terminals.

On the contrary, Figure 2 (middle) shows the improved bussing design where laminated parallel planes are formed from the DC bulk capacitors all the way to the

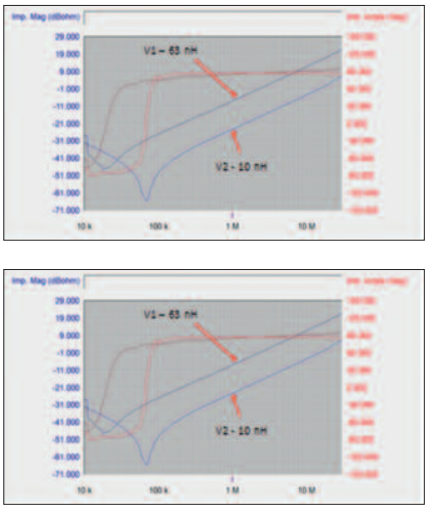

Figure 3: Frequency response of V1 and V2 bussing (top) and V2 bussing with and without snubber PCBs (bottom)

power module terminals. This design eliminates all finger-like bussing features and maintains the smallest current loop from the power module V+ to V- terminals as possible. Implementing this design approach, the DC bus and DC-link capacitor inductance was measured to be 10 nH. Figure 3 shows the magnitude and phase response of the V1 and V2 bussing, respectively, combined with the DC-link capacitor impedance from the SiC power module terminals. Clearly, the source impedance seen by the power module is a combination of the DC bus structure and the equivalent series inductance of the DC-link capacitors. To ensure the lowest source impedance, the designer must utilize either low-inductance capacitors, or parallel many capacitors to reduce the capacitors' effective parasitic inductance.

The snubber capacitor board reduces the effective inductance to 6.8 nH at HF but causes a resonance that can introduce current oscillations between the DC-link capacitors and snubber capacitors. If a snubber is still desirable for the designer, an RC snubber should be implemented to reduce the HF oscillations that can occur with a purely capacitive snubber arrangement. Due to V2 bus structure's low impedance, it was determined that low overshoot and ringing could be achieved with no added snubber circuit. Proper understanding of impedances allows high-speed switching, high efficiency, more bus voltage utilization, and safe utilization of high-speed SiC power modules. This results in an overall higher system power density.

System results

The V2 bussing design was implemented with three CAS325M12HM2 half-bridge power modules to form a three-phase inverter system. In addition to the power modules and DC bussing structures, this design used a liquid- cooled coldplate and three CGD15HB62LP half-bridge gate drivers optimized for SiC. Figure 4 shows clamped inductive load (left) and inverter operation (right) results of the optimized system. Using the V2 laminated bus, test data at a 900 VDC bus and high-speed SiC turn off at 304 A demonstrates an ultra-low overshoot (Figure 4, left). Clean inverter voltage and phase currents feeding a 250 kW three-phase are achieved with f_{sw} = 20 kHz and a 700 VDC bus (Figure 4, right).

Conclusion

A HF power module design philosophy has been extended to the DC bus structure and DC-link capacitors to enable increased DC bus voltage utilization of SiC high-performance power modules by greatly eliminating the overshoot voltage introduced by stray inductance. By optimizing the bus structure and DC-link capacitors the need for external HF snubber capacitors can be eliminated which can lower cost and increase power density. The optimization of bussing inductance, elimination of snubber capacitors, and maintaining current handling capability are concurrently satisfied through an iterative design approach. In addition, the 1200 V SiC power modules were implemented with the new bussing design to demonstrate a 250 kW inverter. The inverter stack-up with the new bussing design showed ultra-low overshoot and clean switching three-phase

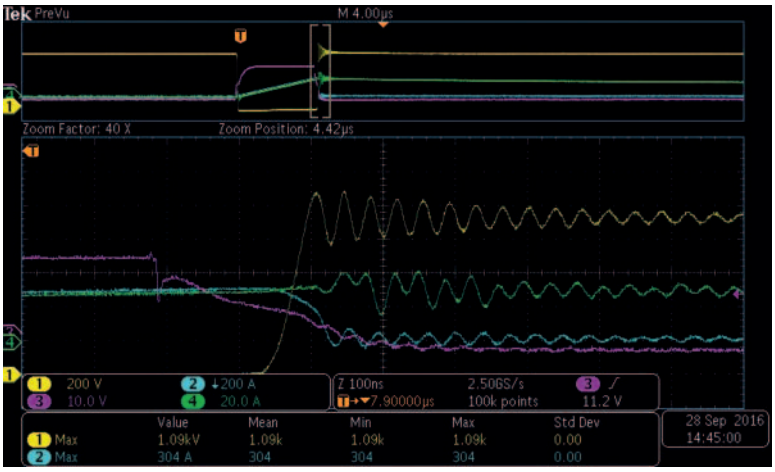

Figure 4: Using a single-phase of the V2 bussing, a 900 V DC bus and turn-off at 304 A demonstrates an ultra-low overshoot (left). A balanced three-phase set of line voltages and one phase current for 250 kW at f_{sw} = 20 kHz & 700 V DC bus (below)