Why and How Isolated Gate Drivers

An IGBT/power MOSFET is a voltage-controlled device which is used as a switching element in power supply circuits or motor drives. 'Gate' is the electrically isolated control terminal for each device. Other terminals of a MOSFET are source and drain; as are emitter and collector for an IGBT. To operate a MOSFET/IGBT, typically a voltage has to be applied to the gate relative to the source/emitter of the device. Dedicated drivers are used to apply voltage and provide drive current to the gate of the power device. This article discusses what these gate drivers are, why they are required and how their fundamental parameters such as timing, drive strength, isolation are defined. **Sanket Sapre, Applications Engineer, Analog Devices, Norwood, USA**

Structure of an IGBT/power MOSFET is such that the gate forms a non-linear capacitor. Charging the gate capacitor turns the power device on and allows current flow between its drain and source terminals while discharging it turns the device off and a large voltage may then be blocked across the drain and source terminals. The minimum voltage when the gate capacitor is charged and the device can just about conduct is the threshold voltage V_{TH}). For operating an IGBT/power MOSFET as a switch, a voltage sufficiently larger than V_{TH} should be applied between the gate and source/emitter terminals.

Consider a digital logic system with a microcontroller which can output a PWM signal of 0-5 V on one of its I/O pins. This PWM would not be enough to fully turn on a power device used in power systems as its overdrive voltage generally exceeds the standard CMOS/TTL logic voltage. Thus, an interface is needed between the logic/control circuitry and the high power device. This can be implemented by driving a logic level n-channel MOSFET which in turn can drive a power MOSFET as seen in Figure 1a.

As in Figure 1a, when IO1 sends out a low signal, $V_{GSQ1} < V_{THQ1}$ and thus MOSFET Q1 remains off. As a result, a positive voltage is applied at the gate of power MOSFET Q2. The gate capacitor of Q2 (C_{GQ2}) charges through pull up resistor R1 and the gate voltage is pulled to the rail voltage of V_{DD}. Given $V_{DD} > V_{THQ2}$, Q2 turns on and can conduct. When IO1 outputs high, Q1 turns on and C_{GQ2} discharges through Q1. $V_{DSQ1} \sim 0V$ such that $V_{GSQ2} < V_{THQ2}$ and hence, Q2 turns off. One issue with this setup is of power dissipation in R1 during on state of Q1. To overcome this, pMOSFET Q3 can be used as a pull up to operate in a complementary fashion with Q1 as seen in Figure 1b. PMOS has a low on state resistance and with its very high resistance in the off state, power dissipation in the drive circuit is greatly reduced. To control edge rates during gate transition, a small resistor is externally added between drain of Q1 and gate of Q2. Another advantage of using a MOSFET is the ease of fabricating it on a die as opposed to fabricating a resistor. This distinct interface to drive the gate of a power switch can be created in the form of a monolithic IC which accepts a logic level voltage and generates a higher power output. This 'gate driver' IC will almost always have additional internal circuits for greater functionality but it primarily works as a power amplifier and a level shifter.

Key parameters of a gate driver

Drive Strength: The issue of providing appropriate gate voltage is addressed by using a gate driver which does the job of a level shifter. The gate capacitor though, cannot change its voltage instantaneously. Thus, a power FET or IGBT has a non-

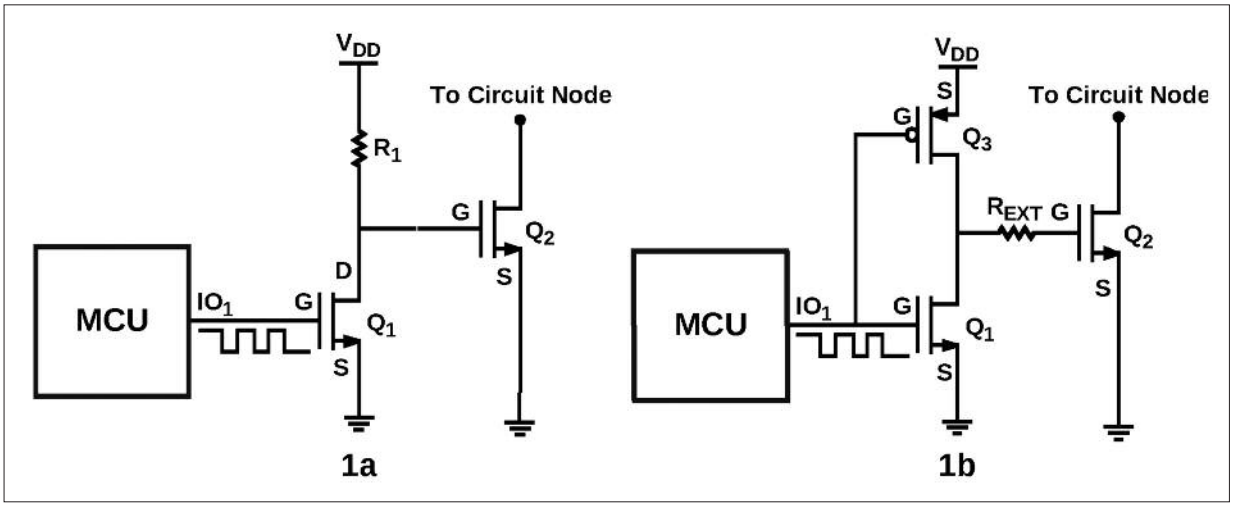


Figure 1: **Power MOSFET driven with inverted logic**

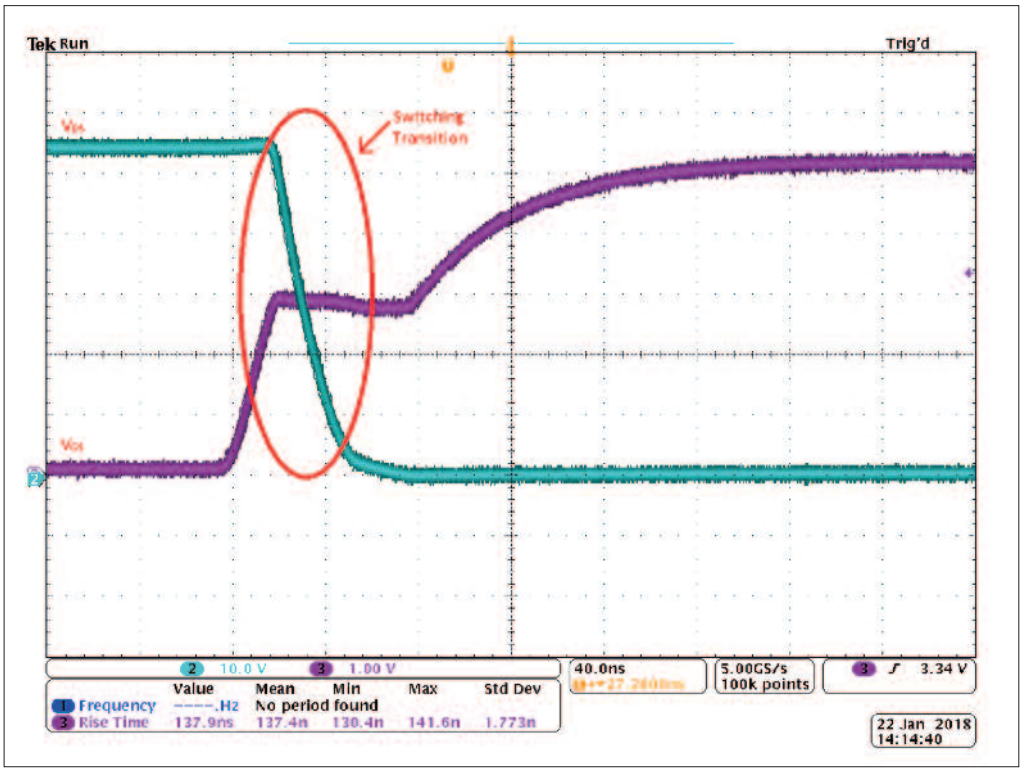


Figure 2: **MOSFET turn on transition without a gate driver**

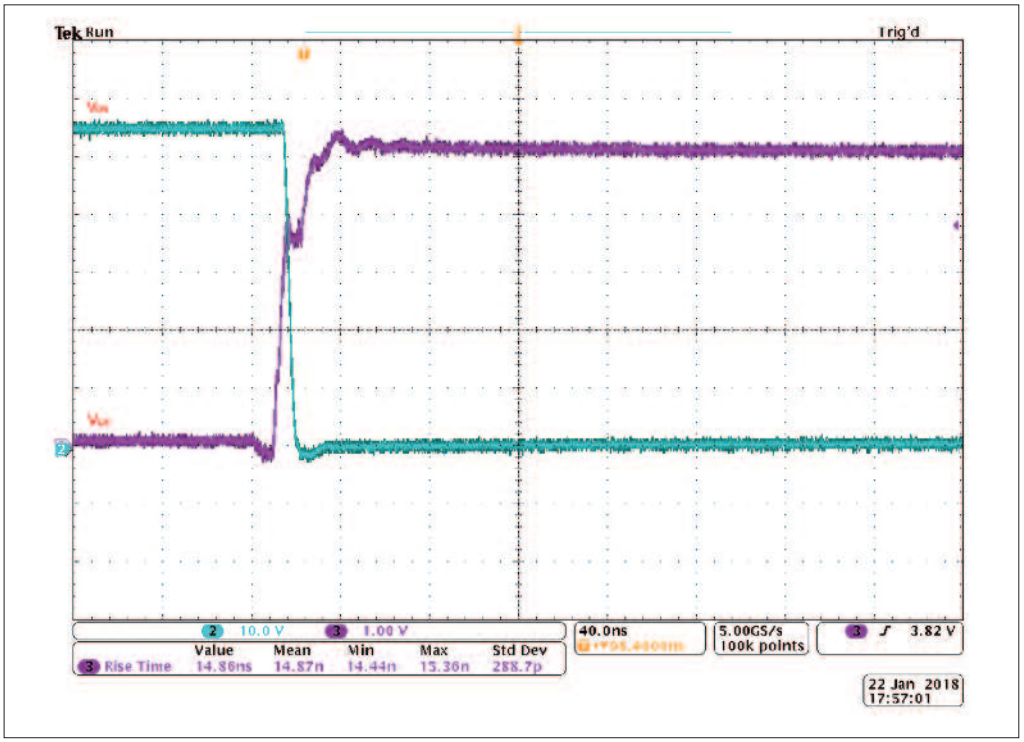


Figure 3: **MOSFET turn on transition with a gate driver**

zero, finite switching interval. During switching, the device may be in high current and high voltage state which results in power dissipation in the form of heat. Thus, transition from one state to another needs to be fast so as to minimize switching time. To achieve this, a high transient current is needed to charge and discharge the gate capacitor quickly.

A driver which can source/sink higher gate current for a longer time span produces lower switching time and thus lower switching power loss within the transistor it drives.

The source and sink current rating for the I/O pins of a microcontroller is typically up to tens of milliamps whereas gate drivers can provide much higher current. In Figure 2, a long switching interval is observed when a power MOSFET is driven by a microcontroller I/O pin at its maximum rated source current. As seen in Figure 3, transition time reduces significantly when ADuM4121 isolated gate driver which provides much higher drive current than a microcontroller I/O pin drives the same power MOSFET. In many cases though, driving a larger power MOSFET/IGBT directly with a microcontroller might overheat and damage the control due to a possible current overdraw in the digital circuit. A gate driver, with higher drive capability, enables fast switching with rise and fall times of a few nanoseconds. This reduces the switching power loss and leads to a more efficient system. Hence, 'drive current' is usually considered to be

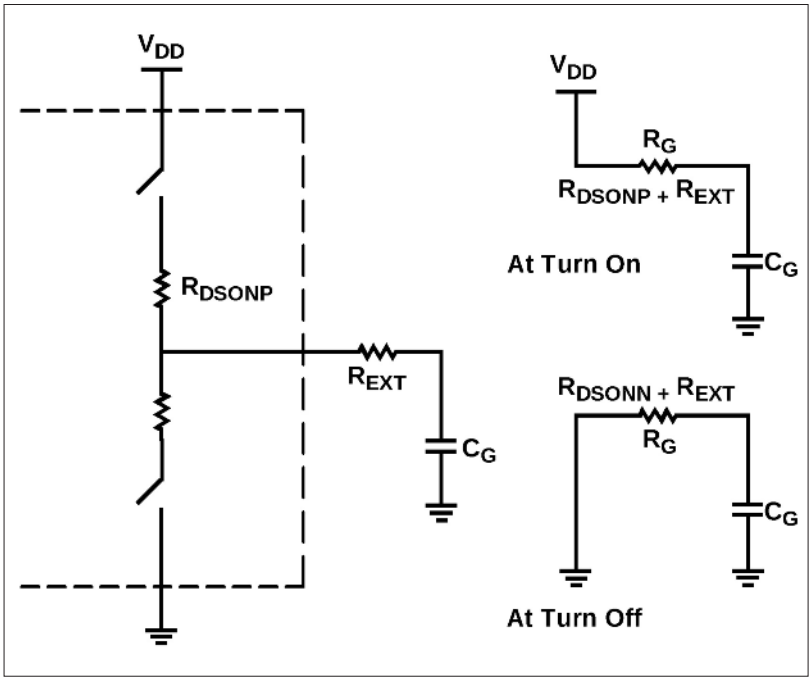


Figure 4: RC circuit model for a gate driver with MOSFET output stage and power device as a capacitor

an important metric in selection of gate drivers.

Corresponding to the drive current rating is the Drain-Source On Resistance termed $R_{DS(ON)}$ metric of a gate driver. While ideally $R_{DS(ON)}$ value should be zero for a MOSFET when fully on, it is generally in the range of a few Ohms due to its physical structure. This takes into account the total series resistance in the current flow path from drain to source.

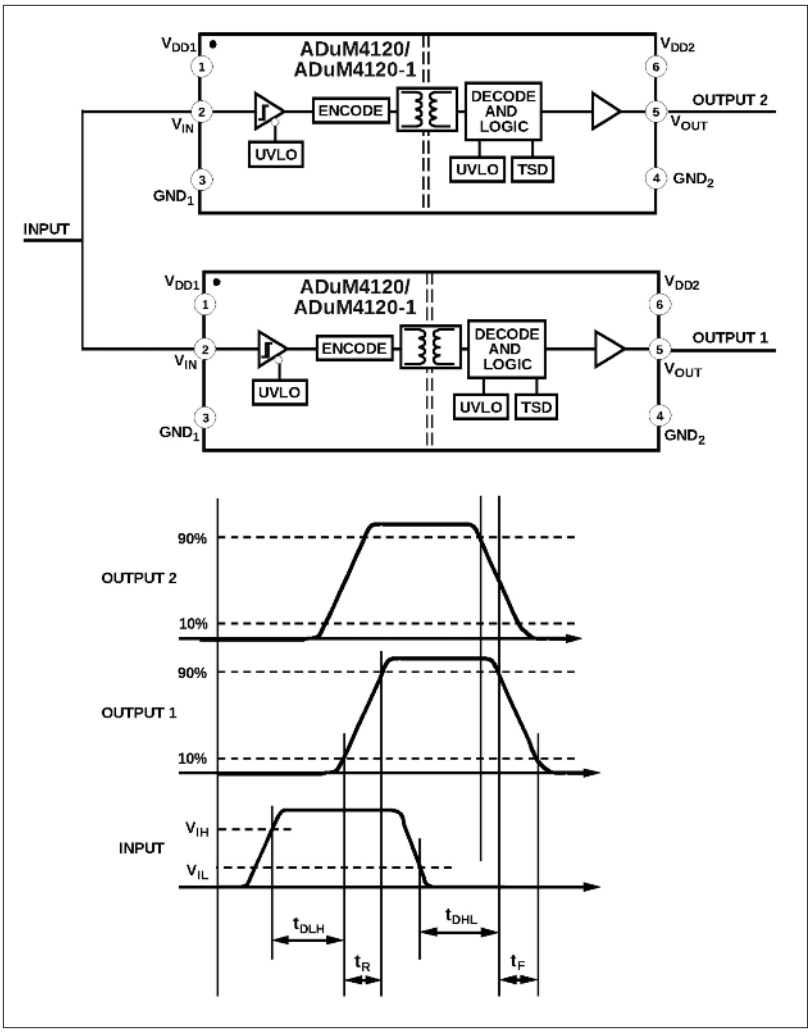
$R_{DS(ON)}$ is the true basis for maximum drive strength rating of a gate driver as it limits the gate current that can be provided by the driver. $R_{DS(ON)}$ of the internal switches determines sink and source current but external series resistors are used to reduce drive current and thus affect edge rates. As seen in Figure 4, high side on resistance and external series resistor R_{EXT} form the gate resistor in the charging path and low side on resistance with R_{EXT} forms the gate resistor in the discharging path.

$R_{DS(ON)}$ also directly affects power dissipation internal to the driver. For a specific drive current, lower value of $R_{DS(ON)}$ allows higher R_{EXT} to be used. As power dissipation is distributed between R_{EXT} and $R_{DS(ON)}$, higher value of R_{EXT} implies more power is dissipated external to the driver. Hence, to improve system efficiency and to relax any thermal regulation requirement within the driver, lower value of $R_{DS(ON)}$ is preferred for the given die area and size of the IC.

Timing: Gate driver timing parameters are essential to evaluate its performance. A common timing specification for all gate drivers including ADuM4120 shown in Figure 5, is the propagation delay (t_D) of the driver which is defined as the time it takes an input edge to propagate to the output. As in Figure 5, rising propagation delay (t_{DLH}) may be defined as the time between input edge rising above input high threshold V_{IH} to the output rising above 10 % of its final value. Similarly, falling propagation delay (t_{DHL}) can be stated as the time from input edge falling below input low threshold V_{IL} to the time output falls below 90 % of its high level. The propagation delay for output transition can be different for a rising edge and a falling edge.

Figure 5 also shows the rise and fall times of the signal. These edge rates are affected by the drive current that a part can deliver but they are also dependent on the load being driven and hence are not accounted for in propagation delay calculation. Another timing parameter is pulse width distortion which is the difference between rising and falling propagation delay on the same part. Thus, pulse width distortion (PWD) = $|t_{DLH} - t_{DHL}|$.

Due to mismatch between transistors within different parts, the propagation delay on two parts will never exactly be same. This results in propagation delay



RIGHT Figure 5: ADuM4120 Gate drivers and timing waveforms

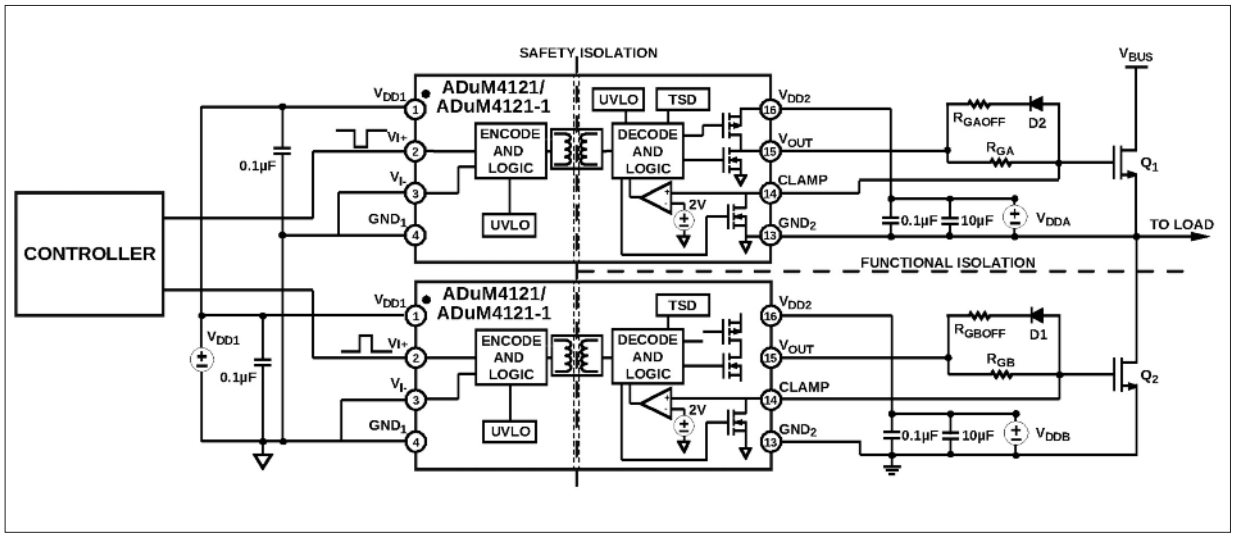


Figure 6: Isolation barriers in a half bridge setup with ADuM4121 isolated gate drivers

skew (tSKEW) which is defined as the time difference between output transitions on two different parts when reacting to the same input in the same operating conditions. As seen in Figure 5, propagation delay skew is defined as part to part. For parts which have more than one output channel, this spec is stated in the same way but is noted as channel to channel skew. Propagation delay skew cannot usually be accounted for in the control circuit.

Figure 6 shows a typical setup of ADuM4121 gate drivers used with power MOSFETs in a half bridge configuration for power supplies and motor drive applications. In such a setup, if both Q1 and Q2 are on at the same time, there is a chance of shoot-through due to the shorting of supply and ground terminals. This can permanently damage the switches and even the drive circuit. To avoid shoot-through, a 'dead-time' must be inserted in the system so that the chance of both switches being on at once is greatly reduced. During dead-time interval, gate signal to both switches is low and thus the switches are ideally in off state.

If propagation delay skew is lower, dead-time required is lower and control becomes more predictable. Having lower skew and lower dead-time results in smoother and more efficient system operation. Thus, timing characteristics are important as they affect speed of operation of the power switch and understanding these parameters leads to an easier and more accurate control circuit design.

Isolation: It is the electrical separation between various functional circuits in a system such that there is no direct conduction path available between them. This allows individual circuits to possess different ground potentials. Signal and/or power can still pass between isolated circuits using inductive, capacitive or optical methods. For a system with gate drivers, isolation may be necessary for functional purposes and it might also be a safety requirement. In Figure 6, we could have VBUS of hundreds of volts with tens of amperes of current passing through Q1 or Q2 at a given time. In case of any fault in this system if the damage is limited to electronic components, then safety isolation may not be necessary, but galvanic isolation is a requirement between the high power side and low voltage control circuit if there is any human involvement on the control side. It provides protection against any fault on the high voltage side as the isolation barrier blocks electrical power from reaching the user in spite of component damage or failure.

Isolation is mandated by regulatory and safety certification agencies in order to prevent shock hazard. It also protects low voltage electronics from any damage due to faults on the high power side. There are various ways to describe safety isolation, but at a fundamental level, they all relate to the voltage at which the isolation barrier breaks down. This voltage rating is generally given across lifetime of the driver as well as for voltage transients of a specific duration and profile. These voltage levels also correspond to the physical dimensions of the driver IC and the minimum distance between pins across the isolation barrier.

Apart from safety reasons, isolation may also be essential for correct system operation. Figure 6 shows a half bridge topology commonly used in motor drive circuits where only one switch is on at a given time. At the high power side, low side transistor Q2 has its source connected to ground. The gate-source voltage of Q2 (V_{GSQ2}) is thus directly referenced to ground and the design of the drive circuit is relatively straightforward. This is not the case with high side transistor Q1 as its source is the switching node which is pulled to either the bus voltage or ground depending on which switch is on. To turn on Q1, a positive gate to source voltage (V_{GSQ1}) which exceeds its threshold voltage should be applied. Thus, gate voltage of Q1 would be higher than V_{BUS} when it is in on state as the source connects to V_{BUS}. If the drive circuit has no isolation for ground reference, a voltage larger than V_{BUS} will be required to drive Q1. This is a cumbersome solution that is not practical for an efficient system. Thus, control signals that are level shifted and referenced to the source of the high side transistor are required. This is known as functional isolation and it can be implemented using an isolated gate driver such as ADuM4223.

Noise Immunity: Gate drivers are used in industrial environment which inherently has a lot of noise sources. Noise can corrupt data and make the system unreliable leading to degraded performance. Thus, gate drivers are required to have good immunity to noise to ensure data integrity. Noise immunity pertains to how well the driver rejects Electromagnetic Interference (EMI) or RF Noise and Common Mode Transients.

EMI is any electrical noise or magnetic interference which disrupts the expected working of the electronic device. EMI which affects gate drivers is a result of high frequency switching circuits and is mainly created due to the magnetic field from large industrial motors. EMI may be

radiated or conducted and can couple into other nearby circuits. Hence, immunity to EMI or RF Immunity is a metric which refers to the ability of a gate driver to reject electromagnetic interference and maintain robust operation without errors. Having high EMI immunity allows drivers to be used in close proximity to large motors without introducing any faults in data transmission.

As seen in Figure 6, the isolation barrier is expected to provide high voltage isolation across grounds at different potentials. But, high frequency switching results in short edges for voltage transitions on the secondary side. These fast transients are coupled from one side to the other due to parasitic capacitance between the isolation boundary which can lead to data corruption. This can be in the form of introducing jitter in the gate drive signal or inverting the signal altogether leading to poor efficiency or even shoot-through in some cases. Thus, a defining metric for gate drivers is Common Mode Transient Immunity (CMTI) which quantitatively describes the ability of an isolated gate driver to reject large common mode transients between its input and output. The immunity of a driver needs to be high if the slew rates in the system are high. Thus, CMTI numbers are particularly significant when operating at high frequencies and large bus voltages.

Conclusion

This article is intended to provide an introduction to gate drivers and thus the parameters discussed so far do not form an exhaustive list with regards to isolated gate driver specifications. There are other driver metrics such as supply voltage, allowable temperature, pinout, etc. which are a common consideration as with every electronic part. Some drivers such as ADuM4135 and ADuM4136 also incorporate protection features or advanced sensing or control mechanism. The variety of isolated gate drivers available in the market make it imperative for a system designer to understand all these specifications and features to make an informed decision about using appropriate drivers in relevant applications.

Literature

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