Direct Cooled Low Inductive SiC Mold Module

To make use of the superior properties of wide bandgap (WBG) semiconductors, power modules are needed with optimized parasitic electromagnetic properties, a high temperature capability and the possibility for a high degree of integration. In this investigation the advantages of a new packaging method for power modules with SiC power MOSFETs on a new multilayer ceramic substrate with transfer molding technology and a direct metallized electrical layer on top surface of the package are emphasized. **Christoph Marczok, Fraunhofer IZM, Berlin; and Andreas Meyer, Rogers Germany GmbH, Eschenbach, Germany**

SiC power modules require a low inductive commutation cell with a low inductive gate path and low inductive input connectors as well as a very low thermal resistance from chip to heatsink. In this development a new approach with another highly insulating material besides prepregs is used to improve power and packaging density in power electronics.

Module design

To achieve highest performance, the multilayer ceramic substrate (MLS, 7 in Figure 1) provides the basis of the power module. It consists of three copper layers separated by two Si3N4 ceramic layers. Compared to standard Direct Bonded copper substrates (DBCs) which provide one electrical layer and the safety insulation (7b) to the heatsink, MLS fulfills two more functions. First, its multilayer setup with through ceramic vias (7a) provides a second electrical layer (midlayer of the MLS), which allows a busbar design to realize a low inductive switching cell. Furthermore that layer is on DC+ potential and shields the switching knot/OUT potential from protected earth (PE), which reduces EMI. Second, the bottom copper contains an etched heat sink structure (7c) for direct fluid cooling.

Four prepackaged SiC power MOSFETs (8), two in parallel are sintered on the top layer of the MLS. The prepackages are electrically connected to the upper copper layer on top of the mold casing (6) with through mold vias (5).

For keeping the advantages of the low inductive module design a primary damped DC-link (2) is implemented, consisting of a resistor and capacitor in series. Furthermore low inductive power connectors DC+/- (1) to the main DC-Link and a low inductive gate path from the semiconductors to the first driver stage/booster (4) need to be considered. This aim is achieved by structuring of the upper copper layer. Therefore the booster SMD components and signal connectors (3) are soldered on the surface and the assembly plastic frame with the spring

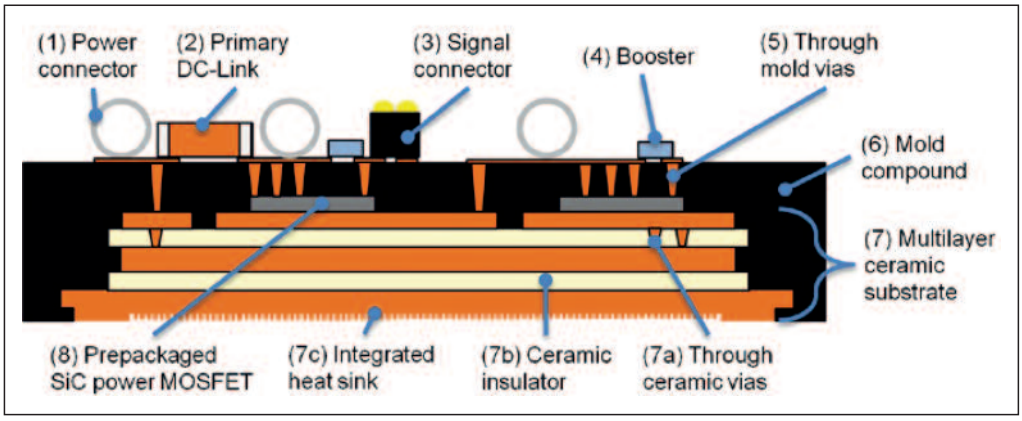

Figure 1: Vertical layer stack of the molded power module with SMD assembly
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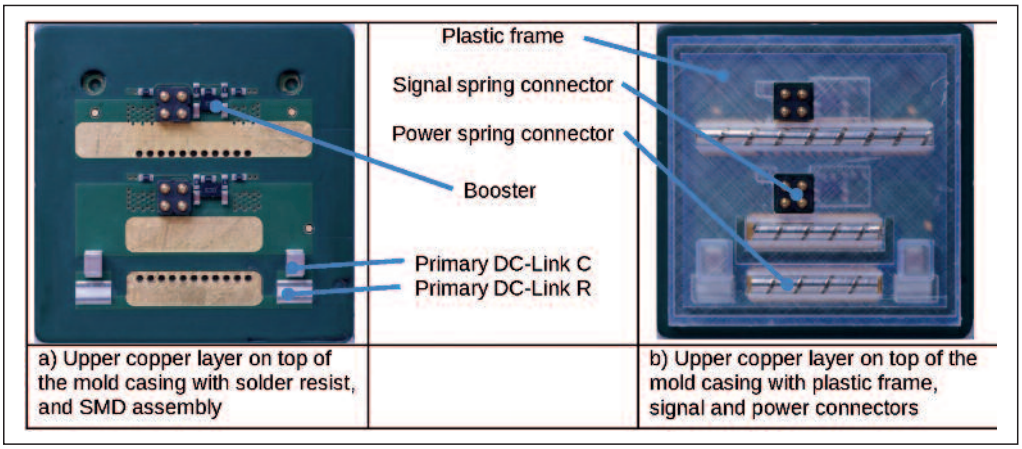

Figure 2: Top view of the molded power module

Material	Thickness in µm	Thermal conductivity in W/(m*K)	Further simulation relevant parameters
MOSFET SiC	330	490	P_{Chip} = 50 W
Ag Sintering layer	60	250	-
Top copper	800	380	-
1st ceramic Si_3N_4	250	90	-
Mid copper	2000	380	-
2nd ceramic Si_3N_4	250	90	-
Bottom copper	1500	380	-
Fluid (water)	-		Flow rate: 6,72 l/min, Δp = 100 mbar, θ = 75 °C

Table 1: material parameters for the thermal simulation

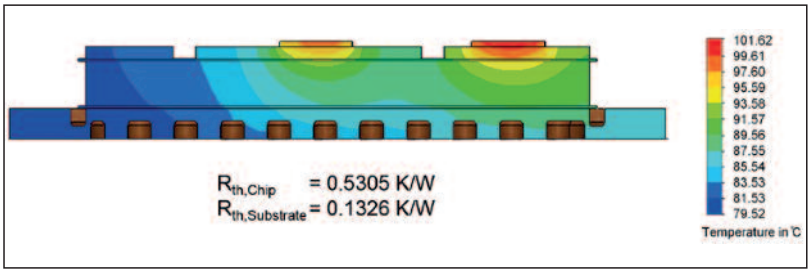

Figure 3: Static temperature distribution in the MLS with four SiC power MOSFETs

power connectors is attached to the power module as shown in Figure 2 a) and b).

In this developmental stage of packaging approach with a diversity of new process elements like a thick MLS with through ceramic vias, a thick substrate transfer molding process, the through mold vias and the upper copper layer on top of the mold casing a robust SiC chip reduces the development risk. Therefore the SiC power MOSFETs were embedded with a PCB process. The bottom side of the bare die is sintered to a copper foil, while the source and gate pads on top are contacted by laser drilled micro vias to the prepackage surface. Thus it was possible to expand and stretch the gate and source pad apart for a larger placing tolerance while keeping its good thermal performance. The copper thickness of the top and bottom layer is around 60 µm for a better robustness towards the through mold via process.

Thermal analysis

The thermal analysis of the power module has been carried out using CFD simulation with SolidWorks flow simulation. The simulation model was symmetrically halved to reduce simulation time. The static temperature distribution on the designed molded power module has been investigated. Table 1 shows the material parameters and the vertical layer stack in the written sequence from top to bottom.

SiC chips are modelled as 6H-SiC, which is the type with the highest thermal conductivity. In this simulation each of all four chips generates power losses of 50 W. The thermal conductivity of the Ag sintering layer is a well experienced value for middle-low porosity. It was modelled as contact resistance with the parameters as shown in Table 1. Figure 3 shows the static temperature distribution in the MLS. The temperature difference can be calculated from the hot spot in Figure 3 on the right chip with 101.62°C and the coolant temperature with 75°C. In general power losses per chip of 188 W can be dissipated.

Packaging technologies and manufacturing

The main manufacuring steps are shown in Figure 4. The power module is manufactured at the Fraunhofer IZM in Berlin. In Figure 4 a) the prepackaged SiC power MOSFETs are sintered on the multilayer Si3N4 substrate manufactured by Rogers in an Active Metal Brazing (AMB) process. In the next step the 4.5 mm thick MLS with a challenging filling geometry is encapsulated in a transfer molding technology, shown in Figure 4 b).

Subsequently the fiducial markings on the MLS are uncovered followed by the laser drilling process to open the 60 ?m thick copper surface of the Prepackages as well as the MLS surface. Afterwards the open surfaces are electrically connected by a sputtered copper seed layer, illustrated in Figure 4 c). In the following it is galvanized up to 60 µm and structured for the electrical functionality. In Figure 4 d) the solder resist is applied, the ENIG surface finish is made and the SMD components are placed and assembled in a reflow soldering process.

In the end the plastic frame is glued to the mold casing surface to keep the creepage distances and to keep the power spring connectors in position for DC+, DC- and OUT.

Conclusion and further steps

An innovative power module packaging is demonstrated consisting of a multi-layer ceramic substrate with through-ceramic vias, built up in a transfer molding process and a post processing electrification of the topside of the mold casing with through-mold vias. Furthermore, a very good thermal performance was shown with a thermal resistance per chip of 0.53 K/W. Finally the outstanding electrical performance is proven with a very low commutation cell inductance of ≤ 1.6 nH.

Ongoing work will improve the power module's thermal design, its electrical interconnects, the integration of more functional, electrical elements as well as the substitution of prepackaged SiC

MOSFETs with bare dies. Furthermore, the manufacturing processes will be optimized for mass production.

Literature

"Low inductive SiC Mold Module with direct cooling", Christoph Marczok, Young Engineer Awardee PCIM Europe 2019, Fraunhofer IZM, PCIM Europe 2019 Proceedings, pages 325 - 329

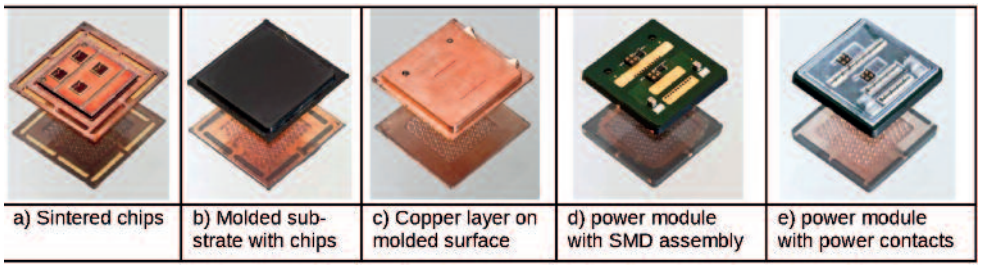

Figure 4: Manufacturing steps of the molded power module