SiC MOSFET Technology with Silicon-Like Reliability

The performance potential of SiC is indisputable. The key challenge to be mastered is to determine which design approach achieves the biggest success in applications. Advanced design activities are focusing on the field of specific on-resistance as the major benchmark parameter for a given technology. However, it is essential to find the right balance between the primary performance indicators like resistance and switching losses and the additional aspects relevant for actual power electronics designs, e.g. sufficient reliability. **Dr. Peter Friedrichs, Infineon Technologies, Neubiberg, Germany**

One of the most important acceptance criteria is the reliability of the device under the operating conditions of its target applications. The major difference to the established silicon device world is the fact that SiC components operate at much higher internal electric fields. Related mechanisms need to be analyzed carefully. What they have in common is that the total resistance of a device is defined by the series connection of contact resistances at drain and source, including the highly doped areas close to the contact, the channel resistance, the resistance of the JFET area, and the drift zone resistance (see Figure 1). In high-voltage Silicon MOSFETs, the drift zone clearly dominates the total resistance; in SiC devices, the part can be designed with a significantly higher conductivity.

Regarding the key MOSFET element, the SiC-SiO interface, the following differences as compared to Silicon have to be considered:

- SiC has a higher surface density of atoms per unit area compared to Si, resulting in a higher density of dangling Si- and C- bonds; defects located in the gate oxide layer near the interface may appear in the energy gap, and act as traps for electrons.
- The thickness of thermally grown oxides strongly depends on the crystal plane.SiC devices operate at much higher drain-induced electric fields in the blocking mode compared to their Si counterparts (MV instead of kV), which requires measures to limit the electric field in the gate oxide to maintain reliability of the oxide in blocking stage. See also Figure 2 for TMOS, the critical point is the trench corner, and for DMOS, the center of a cell.
- SiC MOS structures show for a given electric field a higher Fowler-Nordheim current injection compared to Si devices due to a smaller barrier height. Consequently, the electric field on the SiC side of the interface must be limited.

The above-mentioned interface defects result in a very low channel mobility. Therefore, they cause a high contribution of the channel to the total on-resistance. Thus, the advantage of SiC versus Silicon in the form of a very low drift zone resistance is diminished due to the high channel contribution.

Gate oxide field stress

An observed way to overcome this dilemma is to increase the electric field applied across the oxide in on-state, either higher gate source (V) bias for turn-on or comparably thin gate oxides. The applied electric fields exceed the values usually used in Silicon-based MOSFET devices (4

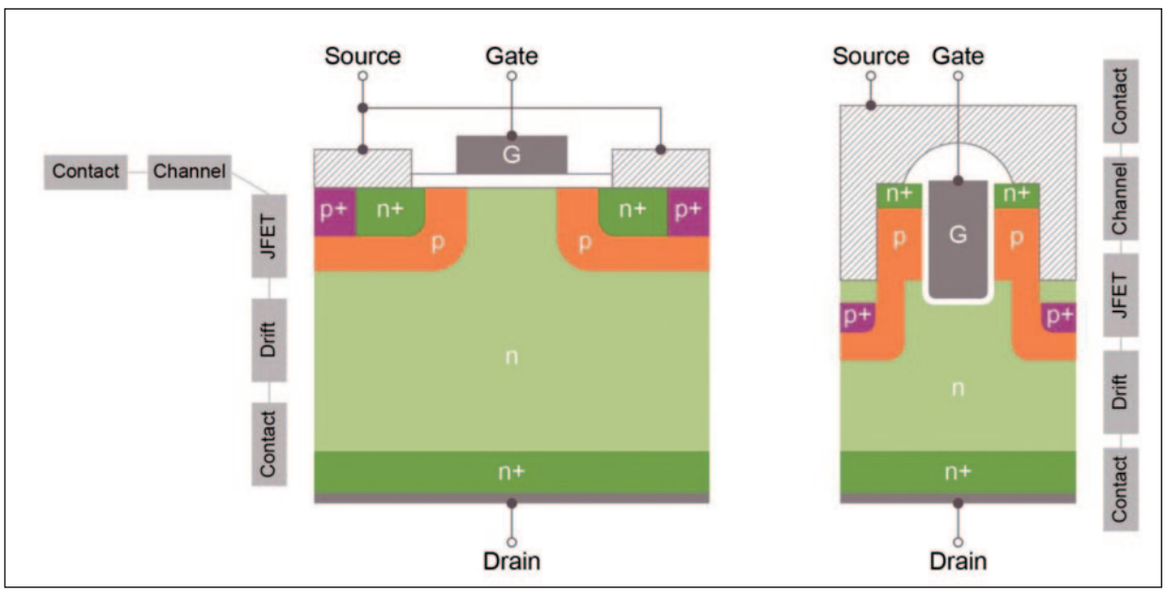


Figure 1: Planar DMOS SiC MOSFET (left), and vertical trench TMOS SiC MOSFET with the corresponding location of resistance-relevant contributions

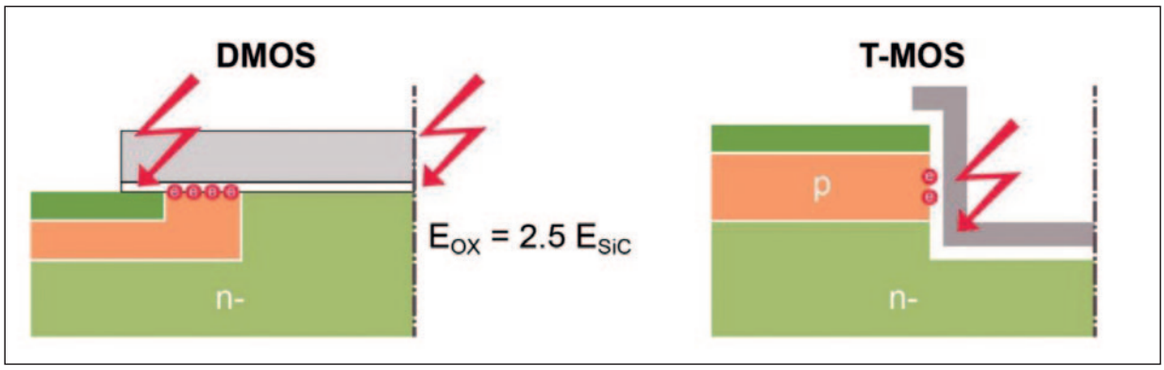


Figure 2: Typical structure of a planar MOSFET (half-cell) revealing two sensitive areas with respect to oxide field stress (left) and typical structure of a trench MOSFET (half-cell), critical issue is the oxide field stress at the trench's corners

to 5 MV/cm vs. 3 MV/cm max. in Silicon). Such high fields in the oxide in the on-state can potentially accelerate wear, and limit the capability of screening remaining extrinsic oxide defects.

Based on these considerations, it is clear that planar MOSFET devices in SiC actually have two sensitive areas with respect to oxide field stress, as sketched in the left part of Figure 2. First, the stress in reverse mode in the highest electric field area close to the interface between drift region and gate oxide, and secondly, the overlap between gate and source which is stressed in on-state.

A high electric field in on-state is seen as more dangerous, since no device design measures are in place which could reduce the field stress during on-state as long as the on-resistance performance has to be guaranteed. Infineon's overall goal is to combine the low $R_{DS(on)}$ offered by SiC with a working mode in which the part operates in the well-known safe oxide field-strength conditions. Hence, it was decided to focus on trench-based devices from the beginning. Moving away from the planar surface with its high-defect density towards other more favorable surface orientations enables a low channel resistance at low oxide fields. These boundary conditions are the baseline for transferring quality assurance methodologies established in the Silicon power semiconductor world in order to guarantee FIT rates expected in industrial and automotive applications.

The CoolSiC MOSFET cell design was developed to limit the electric field in the gate oxide in on-state as well as in off-state (see Figure 3). At the same time, an attractive specific on-resistance for the 1200 V class is provided, achievable even in mass production in a stable and reproducible way. The low on-resistance is ensured driving voltage levels of only V_{GS} = 15 V combined with a sufficiently high gate-source-threshold voltage of 4.5 V typically, being a benchmark in the landscape of SiC transistors.

Special features of the design include the orientation of the channel at a single crystallographic orientation via a self-aligned process. This ensures highest channel mobility and narrow threshold voltage distributions. Another feature is the deep p-trenches intersecting the actual MOS trench in the center in order to allow narrow p+ to p+ pitch sizes for effective screening of the lower oxide corner.

Dynamic performance

Being a unipolar device, the dynamic performance of the SiC-MOSFET is largely governed by its capacitances. The device was designed to have a small gate-drain reverse capacity C_{rss} compared to the input capacity C_{iss}. This is beneficial for suppressing parasitic turn-on, which can prevent the use of sophisticated gate driver circuitry when operated in a half-bridge configuration. Many CoolSiC

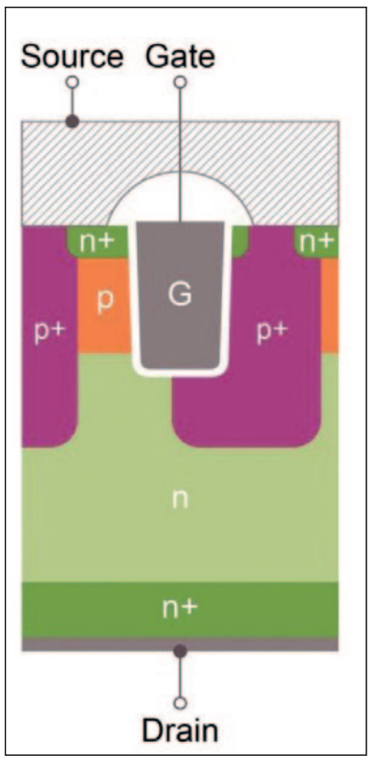


Figure 3: Sketch of the CoolSiC MOSFET cell structure

MOSFET products can be turned off safely even with 0 V at the gate, since in addition to the favorable capacitance ratio the threshold voltage is sufficiently high. The total device capacitances as a function of temperature are summarized in Figure 4 (left).

Figure 4 (right) displays the typical switching losses of a half bridge with single devices mounted in a 4-pin TO-247 housing as a function of drain current. The turn-off energy E_{off} depends only slightly on the load current, since it is dominated by capacities, whereas the turn-on energy E_{on} increases linearly with current, and dominates the total losses E_{tot}. Based on the status from mid-2019, it should be emphasized that the CoolSiC MOSFET shows the lowest Eon among the commercially available 1200 V SiC MOSFETs. E_{on} and E_{off} are practically independent of temperature.

Important to note is the actual housing design that has a significant impact on switching losses, mainly on turn-on losses. Especially effective is the use of Kelvin contacts, which practically separate the load path from the control path in terms of current, and thus, help to prevent di/dt induced feedback loops to the gate signal increasing the dynamic losses.

In general, it is essential to implement fast-switching SiC transistors with low capacitances and gate charges in certain packages only. Major criteria include good thermal performance due to the high-loss power density (absolute losses are reduced with SiC of course, but the remaining ones are concentrated in very small areas). Another criterion is a low stray inductance for managing high di/dt slopes without critical voltage peaks. Finally, especially in the case of multichip packages with more die in parallel, a

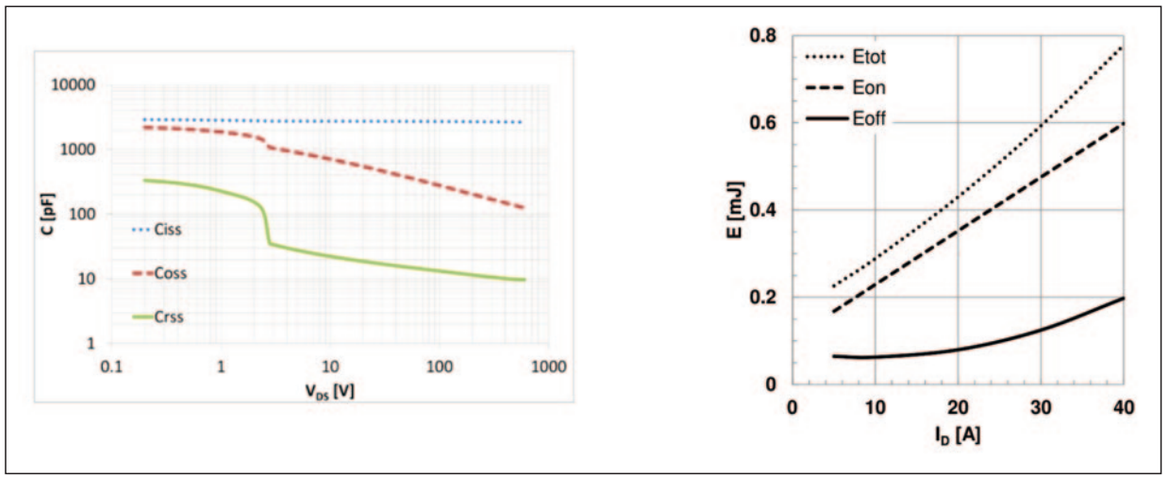


Figure 4: Typical device capacitance vs. drain-source voltage for a 45 mΩ CoolSiC (left) and related switching energies (right) as a function of drain current (for V_{GS} = 15/-5 V, R_{Gext} = 4.5 Ω, V_{DS} = 800 V, T_{vj} = 175°C)

symmetric inner module design based on the strip line concept is mandatory. Current module packages offering such features are the EASY platform for modules, or the TO247 family, respectively TO263-7, for discrete housing.

Gate-oxide reliability

Besides performance, reliability and ruggedness are the most discussed topics for SiC MOSFETs.

Ruggedness is defined as the capability of a device to withstand certain extraordinary stress events, for example, short-circuit performance or pulse-current handling capability. Reliability covers the stability of the device under nominal operating conditions over the targeted application lifetime.

The effects relevant to reliability include the drift of certain electrical parameters or catastrophic failures. For hard failures, the quantification is usually done in the form of FIT rates, which actually state how many devices of a certain type are allowed to fail over a certain period. FIT rates in high-power silicon devices are mostly governed today by cosmic ray effects.

In the case of SiC, an additional influence from gate-oxide reliability needs to be considered due to the oxide field stress. Thus, the total FIT rate is the sum of cosmic ray FIT rates and oxide FIT rates. For cosmic ray stability, a similar approach can be applied such as the one typical in the Silicon sector. Here, FIT rates are obtained experimentally for a certain type of technology, and based on the results, in combination with the application targets, a design can be implemented that meets the FIT rates, usually achieved by optimizing the electric field distribution in the drift zone. For the oxides FIT rates, a screening process needs to be applied to reduce the FIT rates, as defect densities in SiC are still quite high compared to Silicon (in the case of Infineon's Si power devices, the screening of gate oxides still takes place as a quality assurance measure).

The challenge of the gate-oxide reliability of SiC MOS devices is for example to guarantee a maximum failure rate of less than 1 FIT under given operation conditions in industrial applications (as is available today for IGBTs). Since the intrinsic quality and properties of SiO2 on SiC and on Si are almost identical, Si MOSFETs and SiC MOSFETs of the same area and oxide thickness can withstand roughly the same oxide field for the same time (same intrinsic lifetime). Of course, this is only valid if the devices do not contain defect-related impurities, i.e., extrinsic defects. In contrast to Si MOSFETs, SiC MOSFETs exhibit a much higher extrinsic defect density in the gate oxide.

Infineon has invested a significant amount of time and material samples to develop a complete picture regarding the MOS reliability for SiC MOSFETs. We have tested the on-state reliability of electrically screened SiC MOSFETs for 100 days at 150°C using three individual stress runs at different positive and negative gate-stress biases. Each sample group consisted of 1000 pieces.

Using the initial processing conditions, at twice the recommended gate bias of 30 V, less than 10 out of 1000 devices failed. The implemented technology progress reduced this number to only one fail at 30 V, and zero fails at 25 V and -15 V. This one remaining failure is still an extrinsic failure, but it is not critical, as it will occur far beyond the specified product lifetime under the nominal gate-bias use conditions.

To verify the off-state reliability of the CoolSiC MOSFETs, we have stress-tested over 5000 1200 V devices for 100 days at 150°C, V_{GS} = -5 V and V_{DS} = 1000 V. These conditions correspond to the most critical point of the mission profile for industrial applications. A further acceleration is very difficult due to restrictions in the applied drain voltage with respect to the breakdown voltage of the device. Running the tests at even higher drain voltages will falsify the results, as other failure mechanisms such as cosmic-ray induced failures would become more likely. The result was that none of the tested devices failed during this off-state reliability test. As the 650 V device follows the same design criteria as the 1200 V device, the same reliability is expected.

Conclusion

The CoolSiC MOSFET features superior performance in terms of switching behavior and total losses. One of the highlights is the possibility to turn off the device with zero gate bias, which makes the transistor concept the only true "normally-off" device at the moment. We are in an advanced stage of rolling out the 2nd CoolSiC generation which will increase the power handling capability by 25 – 30 % and enhance the safe operating area (SOA) without compromising quality.

Literature

Infineon Technologies White Paper "High-performance CoolSiC MOSFET technology with silicon-like reliability", January 2020

SiC Wafer Cost Reduction

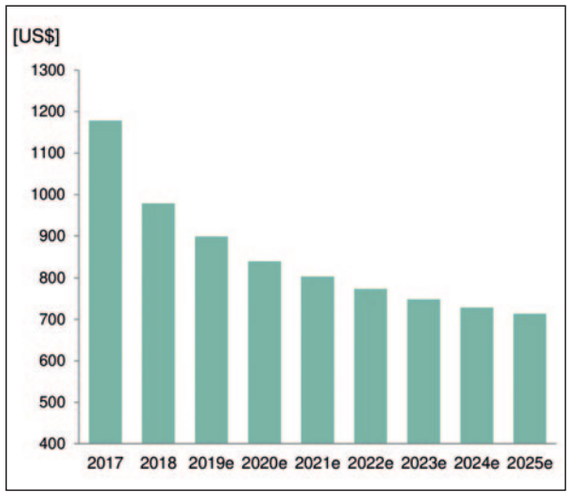
According to a SiC update in May 2020 by Peter Friedrichs SiC raw wafers remain the major cost driver, though the price curve is declining. A special technology saves a lot of the valuable material during processing.

In November 2018 Infineon acquired Siltectra for124 million Euros, a start-up based company in Dresden. They have developed an innovative technology (Cold Split) to process crystal material efficiently and with minimal loss of material. Infineon will use the Cold Split technology to split SiC wafers, thus doubling the number of chips out of one wafer.

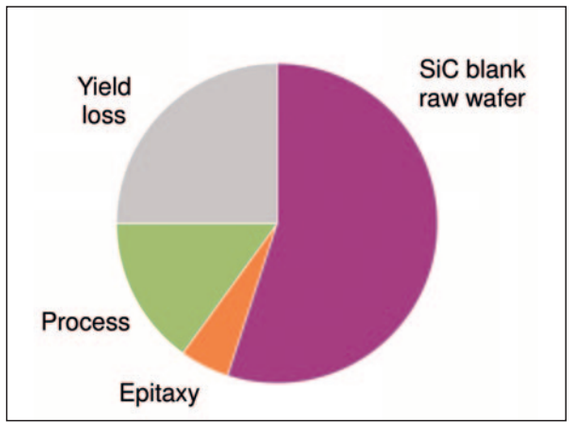
Focus of Cold Split is to split crystalline materials with minimal loss of material compared to common sawing technologies. This technology can also be applied with SiC, for which rapidly rising demand is expected in the coming years. SiC products are already used today in very efficient and compact solar inverters. In the future, SiC will play a more and more important role in electro-mobility. The Cold Split technology will be industrialized at the existing Siltectra site in Dresden and at the Infineon site in Villach, Austria.

Silectra's proprietary process is a high-output, low-cost wafering and thinning technology for substrates like SiC and GaAs, as well as GaN, Sapphire and Silicon. The laser-based technique employs a chemical-physical process that uses thermal stress to generate a force that splits the material with exquisite precision along the desired plane, and produces virtually no kerf loss. The "no kerf loss" capability delivers breakthrough advantages. First, it extracts more wafers per boule than conventional wafering technologies. This drives up output. Second, it dramatically reduces consumables costs.

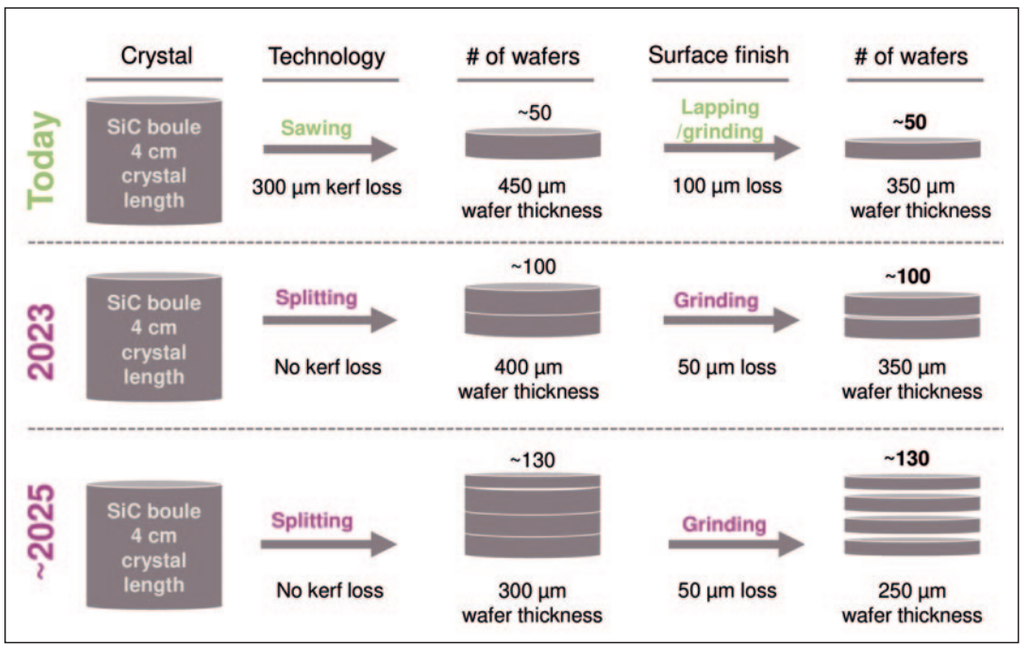
According to Friedrichs design and production of semi-automated process tool park is completed in Dresden, and the clean room is ready for manufacturing by end of calendar year 2020. Wafers for splitting are already available to increase the number of usable wafers by a factor of 2. Boule splitting is planned for 2023 increasing wafers by a factor of 2.0 in a first step, with potential for a factor of 2.6. "Combining boule splitting and wafer splitting will make the most efficient process," Friedrichs pointed out. And the manufacturing lines in Villach are already capable of processing 200 mm diameter SiC wafers! **AS**



SiC 150 mm raw wafer price development **Source: Omdia/Infineon**

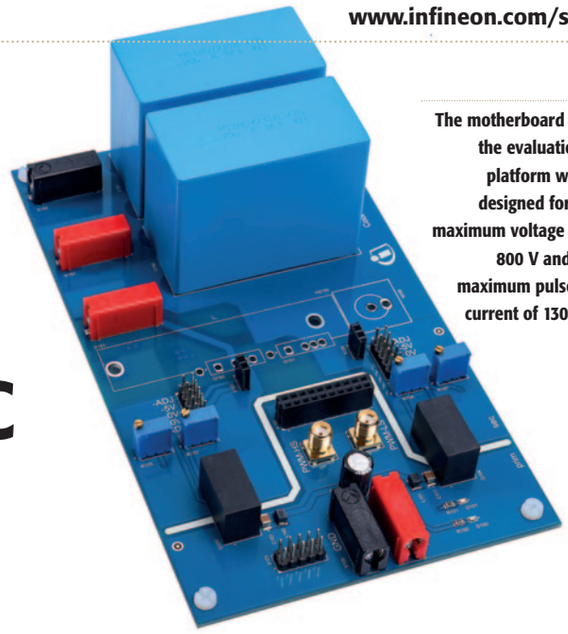


Average SiC MOSFET frontend cost breakdown **Source: Yole/Infineon**



RIGHT: From wafer splitting to boule splitting with Cold Split

Modular Evaluation Platform for Discrete CoolSiC MOSFETs



The motherboard of the evaluation platform was designed for a maximum voltage of 800 V and a maximum pulsed current of 130 A

Double pulse testing is a standard procedure for designers to learn about the switching behavior of power devices. To facilitate the testing of drive options for the 1200 V CoolSiC MOSFET in TO247 3-pin and 4-pin packages, Infineon introduced a modular evaluation platform.

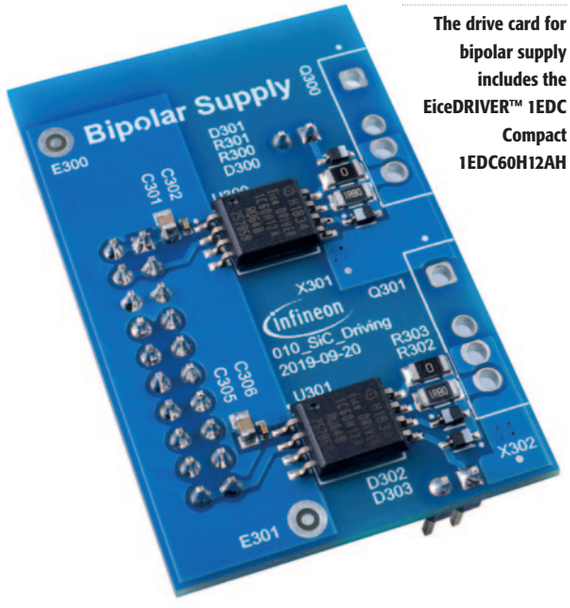
The modular SiC evaluation platform comprises a motherboard with interchangeable drive cards. The drive options include a Miller clamp and a bipolar supply card; additional variants will be launched in the near future. In shortening time-to market for a variety of applications, this portfolio will help paving the way for Silicon Carbide to become mainstream.

The motherboard of the evaluation platform is split into two sections, the primary supply side and the secondary side. On the primary side, the 12 V supply and the PWM will be connected. On the secondary side is the secondary supply of the driver, the half bridge with connections for the shunt for current measurement and the external inductance. The positive operating voltage of the drivers can be adjusted between +7.5 and +20 V, while the negative voltage can be regulated between +1 V and -4.5 V. The motherboard was designed for a maximum voltage of 800 V and a maximum pulsed current of 130 A. For measuring at higher temperatures of up to 175°C, the heatsink can be used together with a heating element.

The Miller clamp card contains the EiceDRIVER™ 1EDC Compact 1EDC20I12MH, the Miller clamp is typically activated below 2V

Serving as a reference design for two drive options, the cards feature driver ICs from the EiceDRIVER™ family suitable for high frequency switching of SiC power devices. The first modular card contains the 1EDC Compact 1EDC20I12MH with an integrated active Miller clamp, which is typically activated below 2 V. The second drive card includes the 1EDC Compact 1EDC60H12AH allowing a bipolar supply, where VCC2 is +15 V and GND2 is negative. With these two driver cards, the portfolio already covers a large part of the options preferred by designers for driving SiC MOSFETs.

All three components of the modular evaluation platform – motherboard, Miller clamp and bipolar drive cards – can be ordered now. An additional drive card for short circuit detection will be added to the portfolio during summer 2020, a card for SMD package testing will follow during the second half of this year. www.infineon.com/tools



The drive card for bipolar supply includes the EiceDRIVER™ 1EDC Compact 1EDC60H12AH